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Pulse Width Modulator Design Using 90nm CMOS Technology

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ABSTRACT: In this paper the design of single chip PWM using a CMOS transistor at 100MHz frequency is designed. The proposed architecture is much simpler as it comprises of the 555 timer. PWM is an important in applications of analog communication and in power control, so PWM is designed to keep in mind about using small area for chip and low power consumption of the device. The PWM is designed in Microwind tool using 90nm technology. The area required for the design is $474\mu m^2$ and the power consumption of the design is 0241mW.

KEYWORDS: Pulse Width Modulator, CMOS, Timer, Astable Mode, VLSI

I.INTRODUCTION

The VLSI technology is used where we can design complex circuits on a single chip. The portable devices such as mobile phones, laptops, smart watches, need a small area for the design and less power consumption, so for a VLSI designer it is very important to keep these two things in mind while designing a chip. The PWM has also designed by keeping small area requirement and low chip size as discussed in this paper. The principle of Pulse Width Modulator was proposed a long time ago, but due to slow development of power electronics it has not been realized till 1980's. The PWM can be easily adapted by microprocessor for controlling the operation of analog circuits. PWM is widely used for applications such as communication, Power conversion or control, measurement. The PWM was earlier developed for analog design and then shifted to digital for reduction of both power consumption and system cost[1].
In the past when partial power was required a rheostat is used to adjust the amount of current flowing through the motor. PWM can be used now a days to reduce the total amount of current increased when a power source is united by resistive means. The power delivered to the source is limited by the modulation duty cycle. The pulses are made in such a way that the average value of high and low is proportional to the duty cycle of the PWM input [2].

II.PULSE WIDTH MODULATOR

PWM is also known as pulse duration modulation. PWM is a modulation technique which is used to encode a message into a pulse. PWM provides control for power supplied to electrical devices. PWM is widely used in measurement and communications to power control and conversion. By changing the pulse width of the PWM its average voltage can be changed. The most easy way to generate PWM is by using function generator [3].
The PWM circuit can also be designed using old 555 timer, which is used for generation of pulses and pulse width or frequency modulation. The 555 timer consists of a high speed, voltage comparator and gates and hence 555 timer performs in the MHz range [4].
The 555 timer chip is a medium size and the multi purpose chip which combines circuit of mimics and digital circuits. If 555 timer is connected with resistor and capacitor, the basic unit circuits such as multivibrator, monostable flip and schmidt trigger can be designed. The 555 timer is popular as waveform generation, detection, monitoring, medical facilities, household appliances and alarm etc. There are four types of basic modes of the 555 timer namely monostable, bistable, astable and timed[5].

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The working of mode depends upon high and low level on the output of trigger level. A brief description of internal configuration of pulse width modulator using 555 timer is given in this paper [6]. The paper is organized as section II describes the basic concept of 555 timer and its circuitry to make the pulse width modulator. The section III describes the block diagram and its circuit diagram using 555 timer as a building block, section IV describes the simulation results and its discussion. The conclusion is described in section V.

III.DESIGN OF PWM

The basic building block of a PWM is a comparator and flipflop. The block diagram of PWM, shown in figure (1), consists of a 555 timer used for designing of PWM.

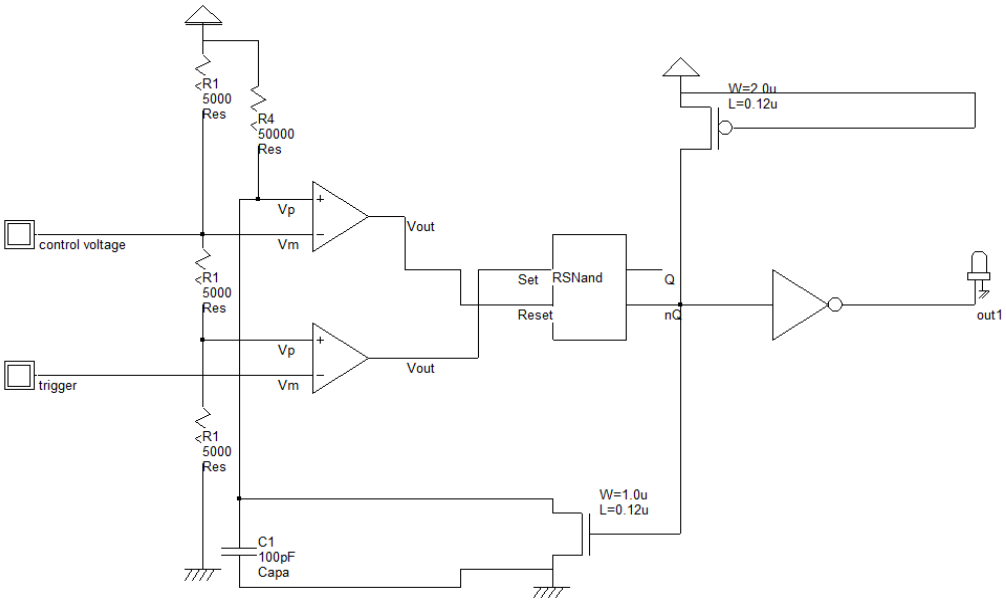

Fig (1) Block diagram of PWM using 555 timer

There are two inputs to the circuit such as control voltage and trigger. The trigger input is used to trigger the PWM pulse. The PWM pulse will get modulated according to the control voltage applied. Figure (2) shows the detailed circuit diagram of PWM using CMOS transistor and resistors. It consists of two comparators and one RS flipflop. The output of the comparator is sent to the flipflop. The voltage comparators are of ideal arithmetic amplifier with identical structure. The comparator is designed with two input terminals and one output terminal. The upper comparator compares the 2V/3 voltage and lower comparator compare a voltage level of V/3. The basic RS flipflop posses set reset functions. The inverted output of the flipflop is fed to an inverter. The output will be inverted of flipflop output.
All the components of the circuit are of digital nature except of resistor and capacitor. The circuit is designed in micro-wind software.

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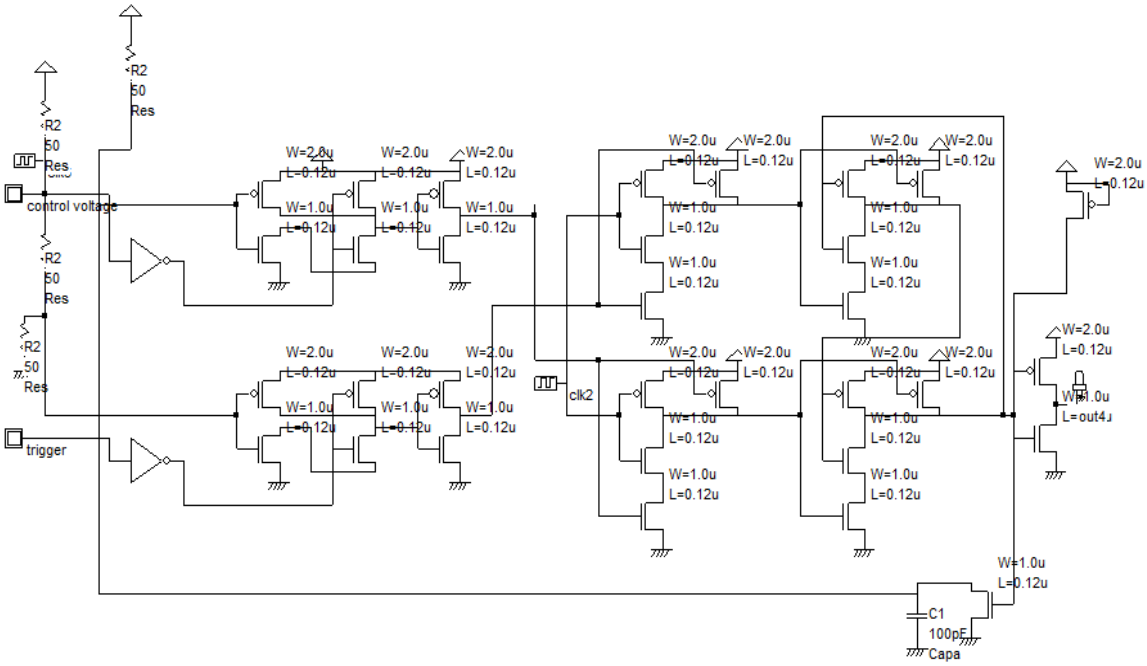

Fig (2) Schematic of PWM

Figure (3) shows the layout of the PWM design. The design was of semi customed nature i.e. NMOS and PMOS transistors are used to make the circuit. The input to the layout is a low level triggered pulse used to trigger the circuit. The input to the design is sinusoidal signal to control the width of the output. The width of output pulse is varied as the amplitude of control signal changes. The width of the pulse would be narrow and congested if the amplitude of the control signal is maximum and the widh of the output signal would be maximum and the pulse would be wide when the amplitude of signal is low.

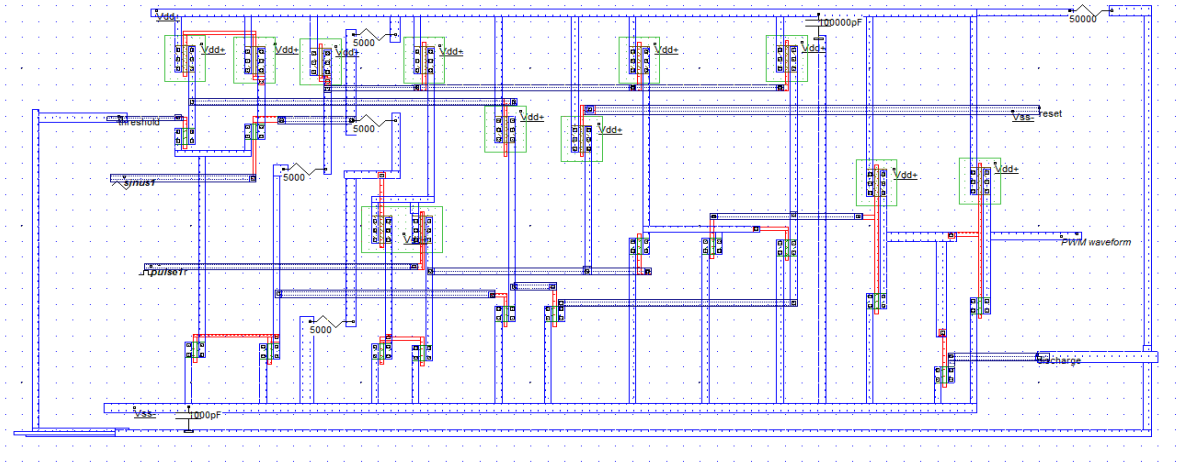

Fig (3) Layout of PWM

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IV.RESULTS AND DISCUSSION

In this section, the simulated result of design using CMOS technology in Microwind software is discussed. In figure (4) the trigger pulse is shown which is used to trigger the PWM. The trigger pulse is a low level pulse.

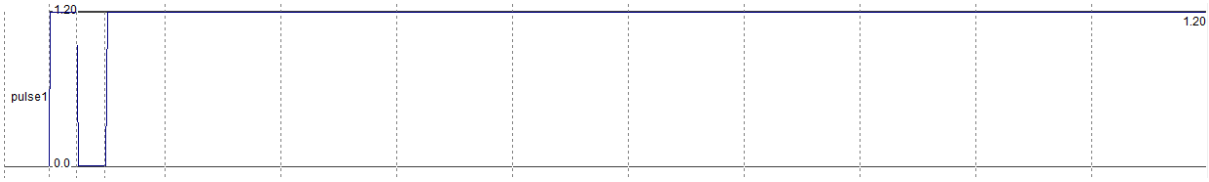

Fig (4) Trigger Pulse

In figure (5) the sinusoidal input signal is shown which is used to modulate the output pulse. The output pulse will be Pulse modulatd according to the sinusoidal input signal.

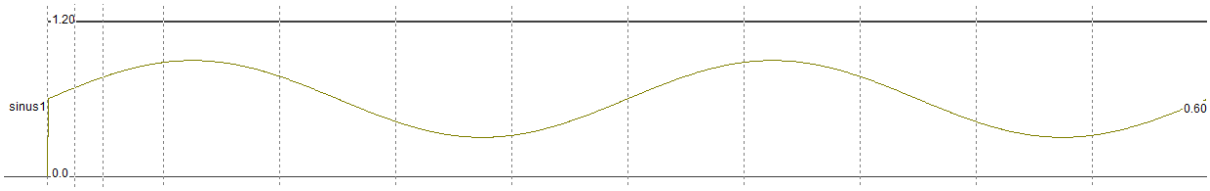

Fig (5) Sinusoidal Input Signal

The approach of designing the circuit in Microwind would reduce the area used for the design and also the power consumption. Figure (6) shows the output of PWM signal.

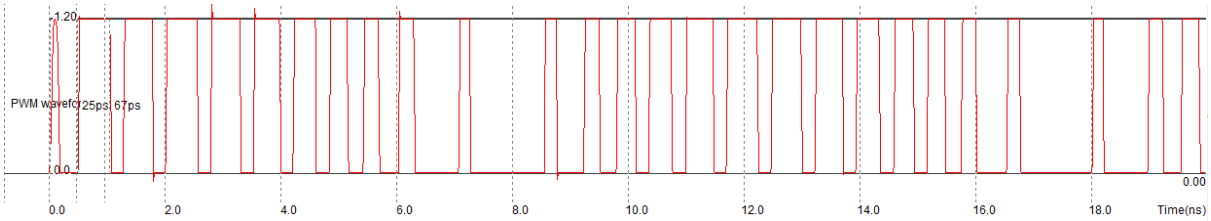

Fig (6) Pulse Width Modulated Output signal

V.CONCLUSION

As compared to earlier designs used for the PWM using 555 timer, a fixed frequency and very low power consumption is required. In this paper a digital PWM has been designed using CMOS technology. The tool used for the designing is Micro-wind. The PWM was designed in 90nm technology. The power consumption for the PWM is 0.241mW and the area required for designing is $474\mu m^2$.

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