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Design and Implementation of FIR Filter Structure using High Adders and Wallace Tree Multiplier

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ABSTRACT: Approximate computing is an come up trend fordigital processing computation atnanoscale and due to which the power management has become a great concern for increase in usage of multimedia devices.The compressors are the basic components used in many different applications like partial product summation in multipliers and so on. In this paper, various types of compressors have been designed. The different logic technique of XOR-XNOR gates and multiplexers has been compared with the existing CMOS logic. The pass transistor utilization of XOR-XNOR gates and multiplexer circuits achieves low power with less number of transistor counts. The act of basic compressor architectures with these low power XOR-XNOR gates and MUX blocks results in terms of area and power. So the proposed 8x8-bit Wallace tree multiplier was designed using this proposed compressors including the power results are compared with the conventional Wallace tree multiplier design.

KEYWORDS: Compressor, multipliers, XOR-XNOR, Wallace Tree multiplier.

I.INTRODUCTION

Multiplication is a mathematical operation which is both simplest and an abbreviated process like adding an integer a specified number of times. Multiplication is the fundamental operation relevant in several processors and systems. Multiplication of two k bit numberare essential in multi operand addition process that can be executed in k cycles of shifting and addition along with hardware, firmware or else software. Operation based on multiplication such as multiply, accumulate and inner product are some of the frequently used an accelerated arithmetic functions executed in many digital signal processing (DSP) applications like convolution, Fast Fourier transform, filtering and microprocessors in its arithmetic and logic unit.The multimedia and digital signal processing system regularly require low power consumption, short design cycle, and flexible processing strength, have become progressively popular over the past few years. The multimedia and DSP applications are highly multiplication intensive to prevent the performance and power consumption of these systems that are dominated by multipliers.

This paperfocused on the development in three stages. In these high speed design, the Wallace tree construction method is used to add the partial products in a tree-like pattern in order to produce two rows of partial products which can be added in the last stage.

II.MULTIPLIER

A basic multiplier subsist of three parts (i) partial product generation (ii) partial product addition (iii) final addition. A multiplier essentially consist of two operands, a multiplicand 'Y' and a multiplier 'X' together with produces a product. In the first stage the multiplicand and the multiplier are multiplied bit by bit to reproduce the partial products. The second stage is the important stage where the most complicated in certain speed of comprehensive multiplier to add these partial products and to generate the Product 'P'.

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III.WALLACE TREE MULTIPLIER

Wallace multiplier is an efficient parallel multiplier. In the conventional Wallace tree multiplier, the first step is to form partial product array. In the second step, groups of three adjacent rows each, is collected. Each group of three rows is reduced by using full adders and half adders. Full adders are used in each column where there are three bits whereas half adders are used in each column where there are two bits. Any single bit in a column is passed to the next stage in the same column without processing. This reduction procedure is repeated in each successive stage until only two rows remain. In the final step, the remaining two rows are added using a carry propagating adder. An example of a representation of the conventional 8-bit by 8-bit Wallace tree multiplier is shown in Figure 1. The three row groupings are shown by light lines.

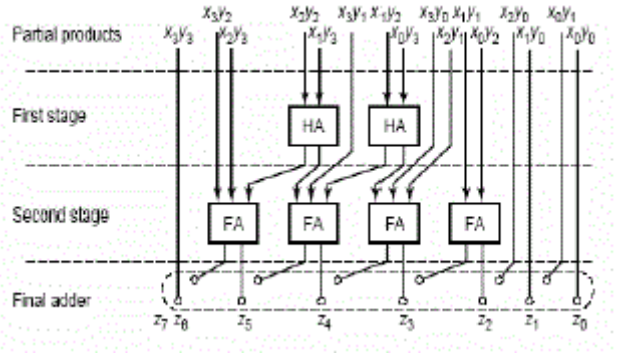

Fig.1: Wallace Tree Multiplier.

Different Compressor logic established upon the concept of counter of full adder. Compressor can be describe as a single bit adder circuit that has more than three inputs as in full adder and having a less number of outputs. In the proposed architecture, it is depend on the factthat both the XOR and XNOR computed are efficiently worn to reduce the delay by replacing the second XOR with the MUX. This is due to the possibility of the select bit through the MUX block before the inputs are applied.Hence time taken for switching the transistors in the critical path is highly reduced.

The summing of the partial product bits are in parallel using a tree of carry-save adders became generally known as the Wallace Tree. The three step processes which are used to multiply two numbers.

a) Formation of bit products.

b) Devaluation of the bit product matrix into two row matrix by means of a carry save adder.

c) Summation of remaining two rows using a rapid Carry Look Ahead-Adder (CLA).

A. 4:2 Compressor

The 4:2 compressor which has 4 inputs x1, x2, x3, x4 and 2 outputs sum & carry along with a Cin and a Cout as shown in Fig 3. The input Cin is the output from the close lower significant compressor. The outputCout is the output for the next knowing stage. It consists of two 3:2 compressors in series and affect a critical path of 4 XOR delays as shown in Fig.4.The alternative implementation is shown in Fig.5. This implementation involves a critical path delay of three XOR's, thus reducing the critical path by 1 XOR delay.

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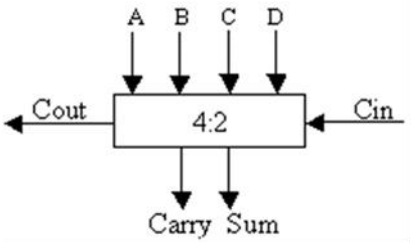

Fig.2: 4:2 compressor

B.5:2 Compressor

The 5:2 compressor generally uses building block for high precision and speed multipliers. The main block diagram of a 5:2 compressor is shown in Fig.9.In which it has seven inputs and four outputs.

In these Five inputs are the primary inputs and the other two inputs cin1, cin2 receive their values from the next compressor from one binary bit order lower in significance.

In 5:2 compressor all the seven inputs have equivalent weight. This compressor develop an output of the same weight as the inputs and three outputs. The output of the above 5:2 compressor is given beneath, X1+X2+X3+X4+X5+Cin1+Cin2=sum+2.(carry+Cout1+Cout2)

In the proposed architecture the mentioned outputs are utilized efficiently by accepting multiplexers at select stages in the circuit. Here the additional inverter stages are also eliminated which results in devaluation of delay, power consumed and number of transistors.

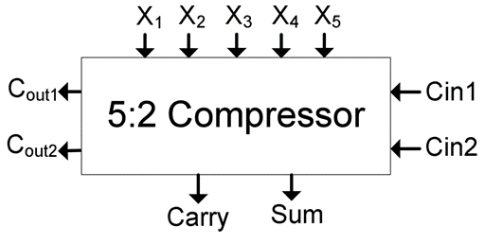

Fig.3: 5:2 Compressor

IV. PROPOSED METHOD

A filter modifies an input signal for signal processing by being a frequency selective network. Analog filter and Digital filter are the two types of filter. Digital filters are preferred in signal processing circuits because of its better SNR ratio as compared to analog signal. Noiseless mathematical operations are performed by the digital filter at each step in the transform. Digital filters have precise and accurate reproduction of the input signal and thus this allows achievement of better filter performance over analog filters. Digital filters are based on binary data rather than analog that works on input voltages. There are different types of digital filters present. FIR Finite Impulse Response and IIR Infinite Impulse Response filters are the most common filters. Again FIR filters have an added advantage over the closed form IIR filter designs in terms of precision, linearity, bandwidth etc.

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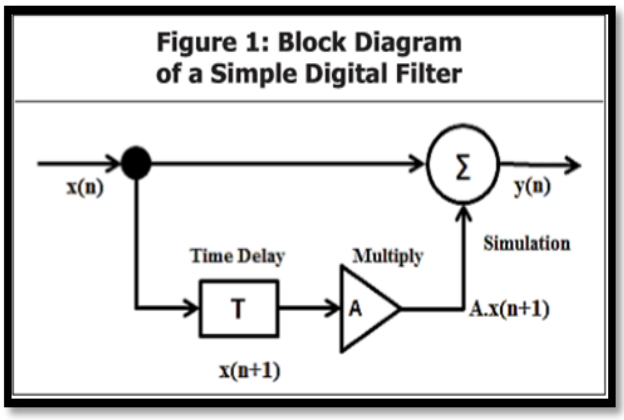

Fig.4:Shows block layout of simple Digital Filter

Fig .4.shows the block layout of a simple digital filter. The 3 basic operations of a digital filter are Time delay, multiplication and addition, decide the behavior of filter. In figure shown above x(n) is the input sequence which is sampled delayed or multiplied according to the impulse response , sampling rate etc.

V. RESULT AND DISCUSSION

XILINX STIMULATION RESULTS

Simulation results are carried out by Xilinx ISE design 13.2. The Results are seized individually for all the tasks in the process of binary multiplication.

1) Device Utilization Report

Project File:	compress.ise	**Current State:**	Synthesized
Module Name:	mull	**• Errors:**	No Errors
Target Device:	xc3s200-4tq144	**• Warnings:**	2 Warnings
Product Version:	ISE 10.1 - Foundation Simulator	**• Routing Results:**	
Design Goal:	Balanced	**• Timing Constraints:**	
Design Strategy:	Xilinx Default (unlocked)	**• Final Timing Score:**	

compress Partition Summary [-]

No partition information was found.

Device Utilization Summary [estimated values] [-]

Logic Utilization	Used	Available	Utilization
Number of Slices	390	1920	20%
Number of 4 input LUTs	679	3840	17%
Number of bonded IOBs	64	97	65%

Detailed Reports [-]

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Mon Apr 13 16:40:36 2015	0	2 Warnings	0
Translation Report					
Map Report					
Place and Route Report					
Static Timing Report					
Bitgen Report					

Delay: The delay of the reduction circuitry of a multiplier is dependent on the number of reduction stages and the delay of each stage.
Transistor Count: The transistor count is used in this paper as metric of circuit complexity. In this paper the transistor count is measured in terms of 4 input LUTs. Comparison of the Parameters between the FIR Forms.

A. TABLE I: Wallace tree Multiplier

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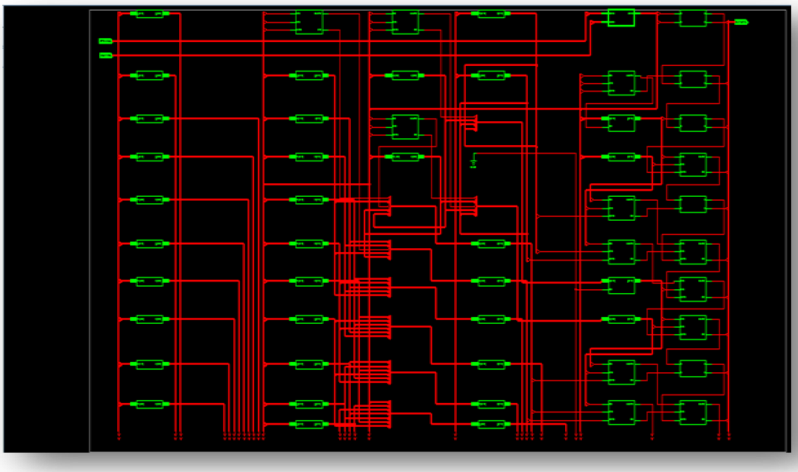
Direct form	Delay(ns)	Power(mw)
8 bit	4.13	5.633
4 bit	10.86	0.144

B. TABLE I: Wallace tree Multiplier Used In FIR Filter

Direct form	Delay(ns)	Power(mw)
8 bit	4.04	2.144
4 bit	4.02	0.862

The table 1 compares the delay of 2 types of direct forms. The delay for the proposed Wallace tree multiplier using FIR is less as compared to Wallace tree, which means Wallace tree multiplier using FIR is faster and more efficient. The area and power consumption for the proposed Wallace tree multiplier is less as compared to FIR filter, which means Wallace multiplier is area efficient, less complex and thus cheap in terms of manufacturing cost.

2) 16*16 with compressors RTL view of proposed multiplier:



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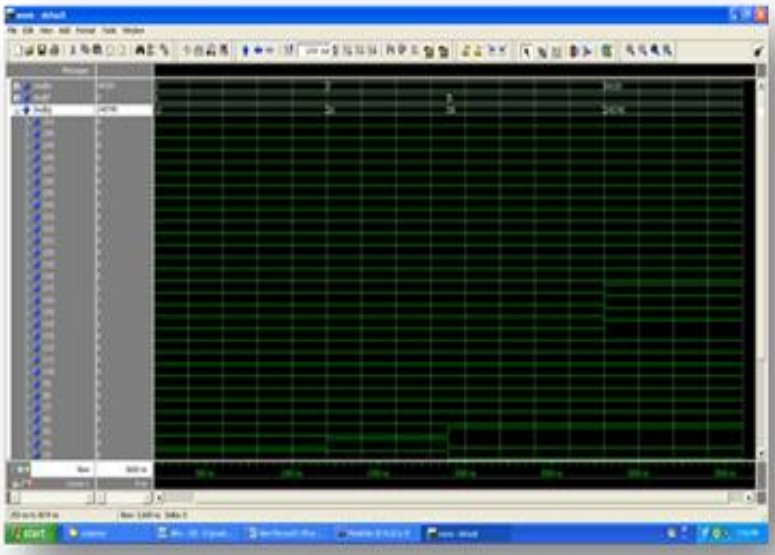
3) Output Waveform



VI.CONCLUSION

Design improvements are made everyday in the existing devices for the best performance and efficiency. In this we have seen that FIR filter when incorporated with the Wallace multiplier gives better filter performance in delay, area and power as compared to existing designs. Wallace multiplier effectively improves the efficiency of the FIR filter by making the performance faster, reducing the delay and area consumed. This proposed design has efficient use in DSP applications, audio signal processing etc.

In this project , 8x8 bit multipliers are designed using 4:2, 5:2 and 6:2 compressors. The conventional Wallace tree design 14 transistor adder cell is compared with the proposed 4:2, 5:2 and 6:2 compressor design with different logic styles. In proposed method the power consumption and the number of transistor was highly reduced. Due to this compressor, the area and speed of the Wallace tree multiplier is increased upto 24%.

The results prove that the proposed architecture is more efficient than the existing onein terms of delay. This approach may be well suited for multiplication of numbers with morethan 16 bit size for high speed applications. The power of the proposed multiplier canbe explored to implement high performance multiplier in VLSI applications.

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