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Pulse Width Modulator Design Technologies: A Review

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ABSTRACT:In this review paper, various techniques of pulse width modulator have been discussed. This paper is a review for the design of the Pulse Width Modulator. Different types of technologies have been discussed in this to optimize the results in terms of area and power consumption.

KEYWORDS: Pulse Width Modulator, CMOS, VLSI, Digital PWM.

I.INTRODUCTION

Pulse width modulator also known as pulse duration modulator, is a modulation technique used to encode a message into a pulse. PWM provides control for power supplied to electrical devices specially to inertial loads like motors. PWM has various applications in measurement and communications to power control and conversion. The internal part of PWM is 555 timer IC chip. One characteristic of PWM is duty cycle which is defined by percentage of on and off time.

The 555 timer IC has various applications for the generation of clock waveforms single pulse and pulse width or frequency modulation. The 555 timer circuit works in astable mode and monostable mode. The pin no. 5 of 555 timer IC modulates the generated pulse width or frequency.[1]

Now a days size of devices is very much reduces and to meet this requirement digitally controlled wide range PWM with small area size is developed which is suitable for dynamic voltage scaling system. Because of small on chip area and high accuracy PWM possess fast control circuitry, high accuracy and reduces the response time from millisecond to nanosecond .[2]

In high bandwidth application such as microprocessor voltage regulator or dynamic power supplier for RF power amplifier multi phased double edge PWM scheme used. The multi phased PWM implements in CMOS technology to meet various advantages such as high precision, better linearity, good noise immunity and wide range of duty cycle.[3]

PWM has one of the application in digitally controlled power convertor which get more attention over the past no of years. This convertor has various advantages in the area of performance, manufacturing and design methodology. It has high throughput and low latency. This convertor possesses very fast switching speed due to use of PWM. In digitally controlled power convertor one of the most critical block is digital PWM which is designed using CMOS IC technique which produce switching frequency up to 15 MHZ. This circuit has also application in digitally controlled switched mode power convertor (SMPC).[4]

One of the other digitally controlled power convertor is based on field programmable gate array (FPGA) which possess high performance digital PWM. Main factor of this design is fine time resolution to meet required voltage regulation accuracy and to limit undesired limit cycling. FPGA based convertor contains two different approach. One is phase locked loop (PLL) or digital clock manager (DCM) which has advantage of very high resolution. Second is use of standard internal logic element which eliminates the need for specialised PLL or DCM. [6]

One of the other application of PWM is in smart sensors which is based on quasi digitalization concept. Because of frequency modulation that produce ratiometric output which reduces error due to change in oscillation time constant, PWM has application in smart sensors operates in harsh environment over wide temperature region. [9]

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II.LITERATURE REVIEW

Kostopoulos et al. in [1] proposed the configuration of the 555 timer from PWM and frequency modulation view point. Since limitation of commercially available 555 timer is speed , parameter tolerance and concept is very much complex. To overcome the limitation of commercial 555 timer employing discrete component in the implementation along with high speed voltage comparator and gates. Since 555 timer is universally accepted device for generation of clock waveforms, single pulse or pulse width or frequency modulation. The presented practical nomograms for the design of modulated monostable and astable circuits.This nomograms simplify the analysis of timing circuit and pulse width and frequency modulator using 555 timer. Because of 555 timer with flexible concept and with the availability of high speed voltage comparator and gates, the configuration is easily constructed which results frequency range in MHZ.

Kose et al. in [2] proposed a digitally controlled current starved pulse width modulator.The accuracy and performence of the proposed digitally controlled PWM evaluvated with 22 nanometer CMOS predictive technology models under PVT variations. The proposed PWM is appropriated for dynamic voltage scaling system due to small on chip area and high accuracy under process, voltage and temperature variation. This design overcome the limitation of previously proposed PWM which is frequency variation. This design is successful to achieve negligible frequency variation, small on chip area, fast control circuitry, high accuracy and dynamic duty cycle control under PVT variation.

Zhang et al. in [3] proposed an analog CMOS double edge multiphase low latency PWM. This design improves the previous conventional design of PWM in many characteristics like high precision, good linearity, better noise immunity and wide duty ratio range. The design is flexible reconfigured for multiphase PWM operation with no restriction on duty cycle range. Multiphase double edge PWM with low latency is important for achieving fast controller response for high bandwidth application such as microprocessor voltage regulator modules.

Malley et al. in [4] proposed programmable digital PWM. The most critical component in any digitally controlled switching power convertors is digital PWM. This design composed of delay locked loop and programmable PWM module which allows generation of high resolution and high switching frequency PWM signal. The design specify various characteristics over convertors which is controlled by analog circuitry such as high data throughput, low latency and processing speed.

Jacobina et al. in [5] introduced microprocessor based scheme which uses standard timer circuit and a simple software algorithm to implement the digital scalar PWM technique. The proposed work establishes the correlation between space vector PWM and digital scalar PWM. It also shows how to make DSPWM strategy equivalent to the SVPWM technique without loosing its simplicity of implementation. Due to flexibility of manipulation, the SVPWM technique is widely employed. The proposed scheme evaluvated mathamatically and tested via computer simulation and experimental tests. The proposed method provides a direct method to deal with non- sinusoidal modulating waveform. This corresponds to generative any attractive non sinusoidal modulating signal in the carrier based modulation technique.

Piazza et al. in [6] proposed all digital PWM which is improvement of general PWM. ADGPWM allows over modulation, negative carrier and reference signal to be managed. This is suited to both serial data processing platform and to integrate circuit implementation to realize several control algorithms for switching power convertor. Now a days use of switching power convertor is wide spread and constant frequency PWM is most frequently used method so ADGPWM IS best suited for this. GPWM has various limitations like incorrect output signal generated for reference duty ratio which is greater than one so it is unable to allow over modulation. On the other hand ADGPWM has several advantages such as it does require external passive components and provides intrinsic noise suppression. It allows easier configuration, more reliable, more compact and easier to integrated with other digital component on IC.

Chen et al. in [7] proposed DPWM with pulse shrinking mechanism technique. Since PWM can be easily adopted by microprocessor for controlling the operation of analog circuit, it is widely utilized by many useful application. PWM has firstly realized with analog design and was shifted to digital domain for reduction of both power consumption and system cost. So for reduction of power consumption and chip area pulse shrinking mechanism technique is very much useful for generation of pulses of PWM. Proposed method results excellent linearity of DPWM.

Ghosh et al. in [8] proposed the design of single chip RF PWM and driver aimed at exciting a 80 watt class E GaN high power stage at 435 MHz. Since next generation space born synthetic aperture radar application requires highly efficient solid state power amplifier at higher output power, switch mode power amplifier able to offer high peak efficiency when driven by constant envelope rectangular input signal. Spectrum analyser used to evaluvate dynamic

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range and to enhance dynamic range proposed work is very much useful which combines output power of several transmit chains.

III.DISCUSSION

Various techniques have been studied which includes a pulse width modulator design for communication and measurement applications. It has a small area and low power consumption. The result obtained from this paper were compared with other technologies of PWM design. Another method in [3] is discussed to generate low latency pulse width modulator and compared with conventional PWM which has good noise immunity and wide range of duty cycle.

IV.CONCLUSION

In this review paper pulse width modulator using CMOS technology has been proposed using various technique which makes proposed design suitable for various applications from measurement and communications to power control and conversion. It also suitable for switched mode power amplifiers, on chip power supplies, smart sensors and synthetic aperture radar. The proposed PWM technique should contain small area and low power consumption.

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