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State Space Model for 3-Phase 4-Wire DSTATCOM under Unbalanced Distorted Supply Voltages

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ABSTRACT: This paper presents the DSTATCOM topology for compensation of AC loads including unbalanced nonlinear loads and DC load component from its DC link in a three phase four wire system. In this the algorithm instantaneous symmetrical components used to extract positive sequence of supply voltage to generate reference compensator current to compensate AC, DC components under unbalance and non stiff supply voltage. Its state space model has derived and presented. Its state matrix components have been developed considering unbalanced non stiff source. The voltage source inverter has operated in current controlled mode and the switching pulses for filter have been developed using a two level and three level hysteresis controller. In the three level hysteresis controllers, inverter Switching strategies uses inverter zero output condition to make DC capacitor voltage constant. The simulations have done in MAT LAB.

KEYWORDS: Active power filter, AC loads, Non linear Loads, Distribution static compensator, Theory of instantaneous symmetrical components.

I.INTRODUCTION

In the last few decades, the revolt of using power electronics devises has increased very a large amount. The extensive use of power electronics based loads causes power pollution rigorously effecting in distribution systems, especially in single phase load are tapped from three phase four wire distribution systems. Because of these uneven power distributions, clean power supply to customers has challenge for power engineers. Active power filters have been developed to solve some of power quality problem which are current harmonics, low power factor and unbalanced load ect. [1-2] one of the main sections of active power filter (APF) is the voltage source inverter (VSI), operated in current controlled mode [3]. The shunt connected custom power device called the distribution static compensator (DSTATCOM), injects harmonic currents equal but opposite magnitude at a point where source, load and filter has connected called the point of common coupling (PCC) so that harmonic filtering, power factor correction, and load balancing can be achieved [4]. The operation of VSI is supported by a dc storage capacitor with proper dc voltage across the VSI (whose DC value is maintained constant) [5-6]. Control methods of the active power filter is an important criterion. There are large numbers of control methods are available to operated active power filters for.

compensation of unbalance and non linear loads. The synchronous detection method to compensate loads, under unbalanced and balanced source voltage conditions but three phase voltage synchronization for each scheme of compensation is essential [6]. Equal resistance method is not possible for three phase three wire system with compensation target for the supply currents to in proportion and phase with their respective supply voltages. The three phase synchronization makes the control circuit complicated when the supply voltages are unbalanced. Control algorithm based on the pq theory is most accepted, also known as instantaneous reactive power theory [7]. Since the algorithm aims to compensate the total instantaneous reactive power of the load but the supply current is unbalanced and distorted even after compensation. The instantaneous active and reactive power can be computed in terms of transformed voltage and current signals [8]. From the instantaneous active and reactive powers theory, harmonic active and reactive powers are extracted using low pass and high pass filters. From harmonic active and reactive powers using reverse alpha and beta transformation, compensating commands in terms of either current or voltages are derived. However to satisfy the constraints of supplying constant active from the source at unbalanced voltages the compensated

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currents are distorted [9]. This is not desirable characteristic of the algorithm. The algorithm works very well if we can find positive sequence voltages for unbalance supply voltages and substitute these voltages in control algorithm based on the instantaneous symmetrical components theory both under stiff and non stiff sources

II. NEUTRAL CLAMPED INVERTER TOPOLOGY

There are various voltage source inverter are presented eminent researchers, but among those the neutral clamped inverter topology has gained considerable attention to load balancing, harmonics reduction and power factor correction. A three phase four wire neutral clamed inverter circuit has shown in Fig. 2.1. It is well published in [12-14]. In this circuit the junction (n') of the two capacitors is connected to the neutral of the load and source. A path for zero sequence current flows through this neutral wire. Therefore the three injected currents of voltage source inverter can be independently controlled. In this configuration there is no isolation transformer and each leg of the VSI is connected to the point of common coupling through an interface inductor with small resistance which is equivalent inductor resistance.

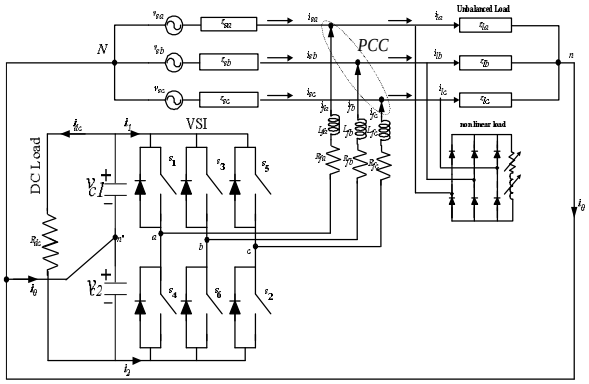

Fig. 2.1 Neutral clamped inverter topology

The topology consists of six switches and there are no isolation transformers. The problem of saturation due to dc current does not arise due to absence of transformers. This topology employs two dc storage capacitors (C_1 and C_2) of same rating. The topology provides the independent tracking of the three reference currents and compensates the zero sequence load current. However it has serious disadvantage that due dc component of load current the voltages of the capacitors do not remain constant shown in [15-16]. Because of the unequal leakage currents, unequal delay in the semiconductor switch, asymmetric charging of the capacitors during transient conditions, the state space model will be developed. This model will be used for ac load compensation, which may be unbalanced and contain harmonics. To equate the unequal capacitor voltage PI controller will be used, explained in the following section.

III. EXTRACTION OF REFERENCE COMPENSATOR CURRENTS UNDER NON STIFF AND UNBALANCED SOURCE VOLTAGES

A three phase, four wire compensated system [15] is shown in Fig.1. The three phase load considered is unbalanced and non linear, the three phase supply voltages and currents also considered unbalanced [16-17]. The compensator , linear and non linear loads are connected at a point called the point of common coupling (PCC), accordingly the compensator has to inject currents in to the line equal and opposite to load currents, then the source currents are free harmonics. The compensator is considered is idle and it is comprised of idle three phase voltage source inverter [18-19].

The basic scheme is shown in Fig. 3.1. In this scheme the compensator is represented by current sources. The aim of the scheme is to generate the three reference current waveforms for i_{fa} , i_{fb} and i_{fc}, denoted by i^*_{fa} , i^*_{fb} , and i^*_{fc} ,respectively, from the measurements of source voltages and load currents such that the supply sees a balanced load. No

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assumption on the nature of the load is required. The compensator will produce desired results as long as its bandwidth is sufficient to follow the fluctuations in the load. The reference currents are generated using the theory of the instantaneous symmetrical components.

Let any three phase instantaneous currents be defined by, i_{fb}, i_{fc} and . The power invariant instantaneous symmetrical components are then defined by.

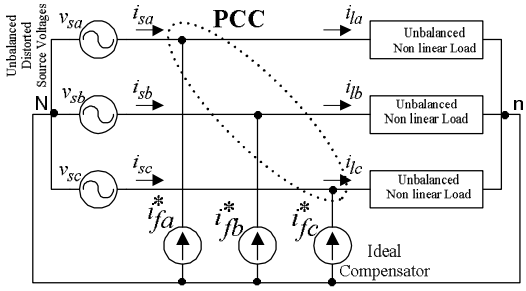

Fig.3.1 Line diagram of 3-phase, 4-wire compensated system

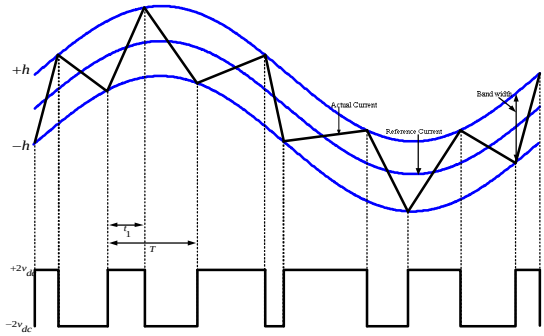

Fig. 4.1 Two level hysteresis current controller.

IV. PWM HYSTERESIS CURRENT CONTROLLER

The linear current controller generates required variable voltage which is then fed into single or multiple pulsed width modulation (PWM) to generate the gate drives switching pulses for voltage source inverter (VSI). The non linear current controller's works on pre defined hysteresis band, in which the actual currents are compared with the reference compensator currents which are generated based on instantaneous symmetrical components theory under unbalanced and distorted source voltages, discussed in previous section.

4.1 Two-Level Hysteresis Current Controller

In conventional hysteresis current controller, the inverter output current is made to follow the reference current generated by the algorithm strictly with certain hysteresis band. Hysteresis current controller operates PWM voltage source inverter by comparing reference current with actual filter current in a pre defined hysteresis bands (upper and lower) shown in Fig. 4.1. The current error is difference between the desired (reference) current and the actual current generated by the inverter. The basic logic is as given below.

If the actual current in certain leg is greater than reference current plus hysteresis band (h/2) then it has to be decreased so the bottom switch has to be turned ON and top switch of the same leg has to be turned OFF at the same time. If the actual current is less than reference current minus hysteresis band (h/2) then it has to be increased so the bottom switch has to be turned OFF and top switch of same leg has to be turned ON at the same time. In this two level switching strategies does not use the inverter zero condition, it uses $+2V_{dc}$ and $-2V_{dc}$ only.

The variation of the switching frequency depends on the value of interface inductance, this variation of switching frequency influence the performance of current controlled VSI in terms of maximum switching frequency and harmonics.

4.2 Three-Level Hysteresis Current Controller [2]

The implementations of a three level hysteresis current controller are set as upper and lower band. The reference current for this three level hysteresis controller are derived from positive sequence of supply voltage based on instantaneous symmetrical component theory discussed in the above section. When the actual current reaches to an outer hysteresis band, at that particular instant of time the inverter output is set to an active positive or negative output to force the reversal of actual current. Accordingly the actual current reaches to an inner hysteresis boundary (this inner hysteresis boundary is nothing but the reference current generated from theory of positive sequence extraction of

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instantaneous symmetrical component), at this time the inverter output is set to a zero condition and the actual current will be forced to reverse direction without reaching the next outer boundary. If the selection of a zero inverter output does not reverse the actual current, it will continue though the inner boundary to the next outer hysteresis boundary, at that time an opposite inverter output will be commanded and the current will reverse.

The switching process of three level hysteresis current controller as shown in Fig.4.2. The MATLAB program for phase-a switching is as follows.

```
if ierra>0
    if ierra>=(h)
    swa=1;
    end
elseif ierra<=del
    swa=0;
end

if ierra<0
    if ierra<=(-h)
    swa=2;
    end
elseif ierra>=(-del)
    swa=0;
end
```

If swa=1implies that the switch state is $+2V_{dc}$

elseif swa=0 implies the switch state is zero

elseif swa=2 implies the switch state is $-2V_{dc}$

Similarly for phase-b and phase-c switching functions can be performed for proper operation of three phase four wire VSI in current controlled mode. The three level hysteresis current controller frequency can be derived while considering three level switching

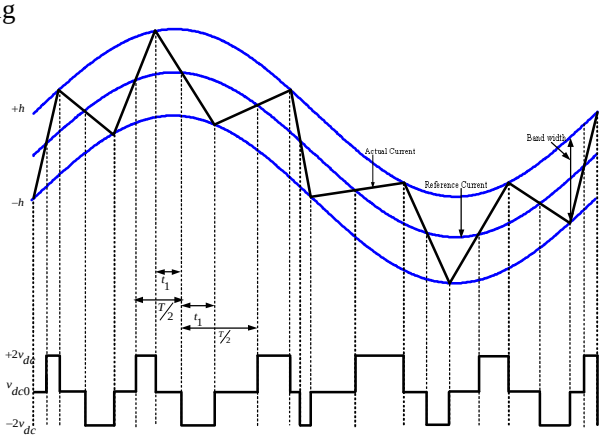

Fig. 4.2 Three-Level Hysteresis Current Controller

4.3 State Space Model for VSI

The gating signal for switch S_1 in Fig. 2.1 is represented by a binary variable S_a. If $S_a = 1$, S_1 is closed, and if $S_a = 0$, S_1 is open. A gating signal for S_4 is the complementary signal that is if $\bar{S}_a = 0$, S_4 is open, and if $\bar{S}_a = 1$, S_4 is close. Similarly $S_b, \bar{S}_b$, S_c , $\bar{S}_c$, and represent gating signals for switches S_3 , S_6, S_5 and S_2 respectively. The switches of the inverter will be operated by generating switching signals to most positive group and

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most negative group in complementary form such that in each leg one of the switches is always gated. Accordingly by operating the switches the input currents to the inverter i_1 and i_2 are derived from Fig. 3.3.

$$i_1 = S_a\, i_{fa} + S_b\, i_{fb} + S_c\, i_{fc} \tag{4.1}$$

$$i_2 = \bar{S}_a\, i_{fa} + \bar{S}_b\, i_{fb} + \bar{S}_c\, i_{fc} \tag{4.2}$$

The voltage source inverter configuration of switches S_1 to S_6 is operated in the three level hysteresis current control mode. When the filter current i_{fa} touches the pre-calculated lower limit of hysteresis band, switch S_1 is closed. When the filter curent reaches to the inner band which is reference current generated usig contol theory, the swithc S_1 is opens and zero state will be applied. If the selection of a zero inverter output does not reverse the actual current, it will continue though the inner boundary to the next outer hysteresis boundary which S_4, will closes, at that time an opposite inverter output will be commanded and the current will reverse.
The equivalent circuit for this mode is shown in Fig 4.3.

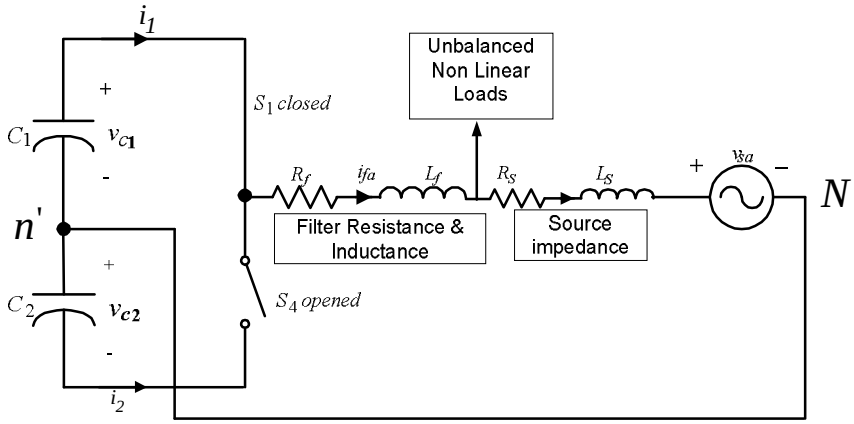

Fig. 4.3 Equivalent circuit for phase a when is on and is off.

Applying KVL around the loop we get

$$\frac{di_{fa}}{dt} = -\frac{R_f + R_S}{L_f + L_S} i_{fa} + \frac{v_{c_1}}{L_f + L_S} - \frac{v_{sa}}{L_f + L_S} \tag{4.3}$$

Similarly if the current hits a pre-calculated upper limit, switch is opened and is closed. From an equivalent circuit similar to Fig. 4.2, we can write,

$$\frac{di_{fa}}{dt} = -\frac{R_f + R_S}{L_f + L_S} i_{fa} - \frac{v_{c_2}}{L_f + L_S} - \frac{v_{sa}}{L_f + L_S} \tag{4.4}$$

From equation (4.3) and (4.4) combined to get the following equation.

$$\frac{di_{fa}}{dt} = -\frac{R_f + R_S}{L_f + L_S} i_{fa} + S_a \frac{v_{c_1}}{L_f + L_S} - \bar{S}_a \frac{v_{c_2}}{L_f + L_S} - \frac{v_{sa}}{L_f + L_S} \tag{4.5}$$

Similarly for phase's b and c, we have,

$$\frac{di_{fb}}{dt} = -\frac{R_f + R_S}{L_f + L_S} i_{fb} + S_b \frac{v_{c_1}}{L_f + L_S} - \bar{S}_b \frac{v_{c_2}}{L_f + L_S} - \frac{v_{sb}}{L_f + L_S} \tag{4.6}$$

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$$\frac{di_{fc}}{dt} = -\frac{R_f + R_S}{L_f + L_S} i_{fc} + S_c \frac{v_{c_1}}{L_f + L_S} - \overline{S}_c \frac{v_{c_2}}{L_f + L_S} - \frac{v_{sc}}{L_f + L_S} \quad (4.7)$$

In Fig. 4.3 the switch can be closed and opened or vice versa. In each case KCL can be applied at nodes 1 and 2, and KVL can be applied around the loop of the closed switch. The resulting equations can be combined with the help of (4.1) and (4.2) and binary variables and to obtain the following, assuming

$$\frac{dv_{c_1}}{dt} = -S_a \frac{i_{fa}}{C} - S_b \frac{i_{fb}}{C} - S_c \frac{i_{fc}}{C}$$

$$\frac{dv_{C2}}{dt} = -\overline{S}_a \frac{i_{fa}}{C} - \overline{S}_b \frac{i_{fb}}{C} - \overline{S}_c \frac{i_{fc}}{C} \quad (4.8)$$

$$\frac{d_{vdc0}}{dt} = 0 \quad (4.9)$$

We obtain the following state space model

$$\dot{x} = Ax + Bu \quad (4.10)$$

Where $\frac{d}{dt}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} u$ $x_1 = \begin{bmatrix} i_{fa} & i_{fb} & i_{fc} \end{bmatrix}^{\Gamma}$, $x_2 = \begin{bmatrix} v_{c1} & v_{c2} & v_{dc0} \end{bmatrix}^{\Gamma}$

$u = [v_{sa} \quad v_{sb} \quad v_{sc}]^t$

$$A_{11} = \begin{bmatrix} -\frac{R_f + R_S}{L_f + L_S} & 0 & 0 \\ 0 & -\frac{R_f + R_S}{L_f + L_S} & 0 \\ 0 & 0 & -\frac{R_f + R_S}{L_f + L_S} \end{bmatrix} \quad A_{12} = \begin{bmatrix} \frac{S_a}{L_f + L_S} & \frac{-\overline{S}a}{L_f + L_S} & 0 \\ \frac{S_b}{L_f + L_S} & \frac{-\overline{S}b}{L_f + L_S} & 0 \\ \frac{S_c}{L_f + L_S} & \frac{-\overline{S}c}{L_f + L_S} & 0 \end{bmatrix}$$

$$A_{21} = \begin{bmatrix} \frac{-S_a}{C} & \frac{-S_b}{C} & \frac{-S_c}{C} \\ \frac{\overline{S}a}{C} & \frac{\overline{S}b}{C} & \frac{\overline{S}c}{C} \\ 0 & 0 & 0 \end{bmatrix},$$

$$B_1 = \begin{bmatrix} -\frac{1}{L_f} & 0 & 0 \\ 0 & -\frac{1}{L_f} & 0 \\ 0 & 0 & -\frac{1}{L_f} \end{bmatrix} \quad A_{22} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

V. SIMULATION RESULTS AND ANALYSIS

To understand the actual compensator, a neutral clamped 3-phase, 4-wire voltage source inverter is chosen and simulated in MAT Lab environment [14], shown in Fig.2.1. The load and the compensator are connected at the point of common coupling (PCC). The voltage source inverter is consisting of six IGBT switches each with anti parallel diodes which allow the flow of current in both the directions. The middle point of the two capacitors is connected to the neutral of the load. The midpoint of the inverter legs are connected to the PCC through interface inductor. A small resistance is considered which interface inductor resistance.

The system parameters for the simulation studies are given in Table 1.

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TABLE I System Parameters for Simulation Studies

System parameters	Value
Source voltage	$V_{sa} = 340\sin(100\pi t)V$ $V_{sb} = 391\sin(100\pi t - 120^0) + 117.3\sin(300\pi t + 30^0)V$ $V_{sc} = 272\sin(100\pi t + 120^0) + 81\sin(300\pi t - 30^0)V$
System frequency	50 Hz
DC capacitors	2000 micro farads
Inter face inductors	$L_f = 15mH$
Inter face resistance	$R_f = 2\Omega$
PI controller gain	Kp=15, Ki= 2
Reference voltage	$V_{dcref} = 500V$
Unbalanced load parameters	$Z_a = 17.32 + j10,$ $Z_b = 15 + j25.98$ $Z_c = 43.46 + j11.64\Omega$
Non linear load	Three phase diode rectifier with R= 600ohms, L= 0.1 H

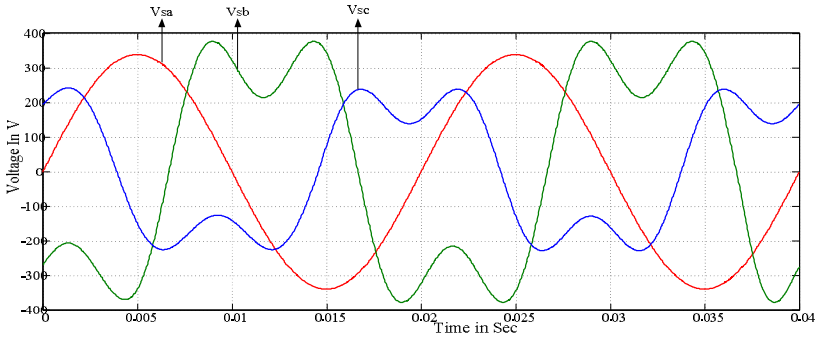

Fig. 5.1 Unbalanced and distorted three phase supply voltages

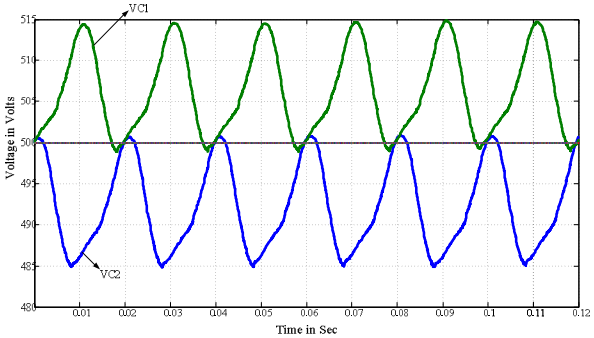

Fig. 5.2 DC Capacitors voltage variations in two level HC

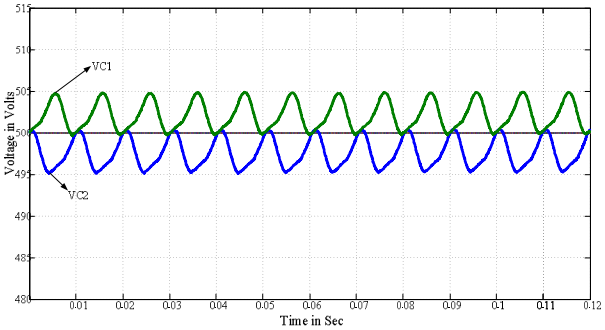

Fig. 5.3 DC Capacitors voltage variation in Three level HCC

In section 4 explained state space model of three level hysteresis current controllers. According to the Fig. 4.1 and 4.2, in the three levels HCC the compensator can use positive, negative and zero level of the inverter output. Due to

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this zero level switching, the variation of voltage across two capacitors is reduces which is shown in Fig. 5.3. The voltage variation across two capacitors in two level shown in Fig. 5.2. In this it is clearly shown that, under two level HCC voltage variations is more, whereas in three level voltages variation reduces considerably.

4.4 Transient performance of DC link Voltage controller in two levels HCC

The Eqn. (19) is used to generate DC load power including losses in the inverter. While maintaining this dc load power constant using PI controller under two level HCC, it is possible to maintain the capacitor voltage also constant. From the Fig. 5.4 it is observed that, initially the compensator is operated under steady state conditions. At $t = 0.03\,\text{sec}$, load is suddenly reduced to half of it is original. Due to this sudden reduction of load, power consumed by the load reduces and the capacitor absorbs surplus power supplied by the source. Because of this surplus power the capacitor voltages will increase above the reference value. Using PI controller gain the variation in the capacitor voltages will come back to it is reference value at $t = 0.045\,\text{sec}$. After few cycles at $t = 0.065\,\text{sec}$, the load switches back to it is full load. At this point of time, load requires high amount of power and this power will be supplied from the capacitors due to which the capacitor voltage will fall down. Again the PI controller action starts and brings the voltage variation in the capacitor to it is reference value within few cycles. From Fig. 5.5, it is observed that the source current changes with respect to the load and dc link voltage changes. At $t = 0.03\,\text{sec}$, the source current magnitude reduces due to reduction of load and the source current magnitude increases to it is original value at $t = 0.065\,\text{sec}$

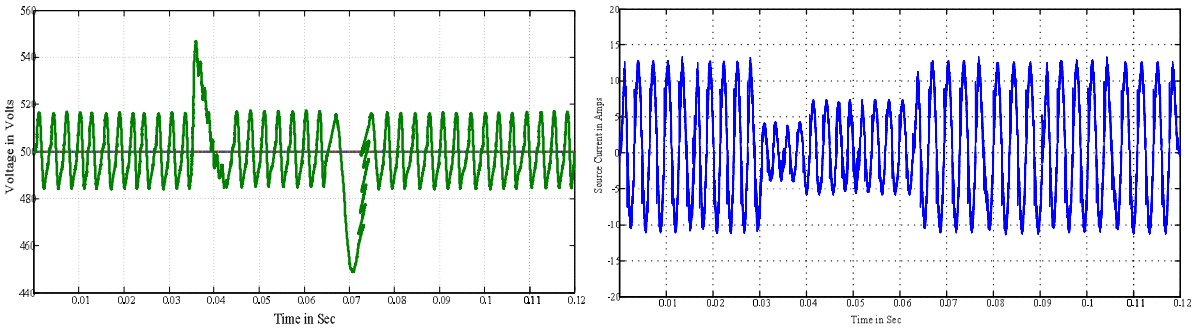

Fig. 5.4 DC link voltage variation in two level HCC , Fig. 5.5 Source current after compensation in two levels HCC under transient condition.

5.2 Transient performance of DC link Voltage controller in three levels HCC

The Eqn. (19) is used to generate DC load power including losses in the inverter. While maintaining this dc load power constant using PI controller under three level HCC, it is possible to maintain the capacitor voltage also constant. From the Fig. 5.6 it is observed that, initially the compensator is operated under steady state conditions. At $t = 0.03\,\text{sec}$, load is suddenly reduced to half of it is original. Due to sudden reduction of load, power consumed by the load reduces and the capacitors absorb surplus power supplied by the source. Because of this surplus power the capacitor voltages will increases above the reference value. Using PI controller gain, the variation in the capacitor voltages will come back to it is reference value at $t = 0.04\,\text{sec}$. After few cycles at $t = 0.65\,\text{sec}$ the load switches back to it is full load. At this point of time, load requires high amount of power and this power will be supplied from the capacitors due to which capacitor voltage will fall down. Again the PI controller action starts and brings the voltage variation in the capacitor to it is reference value within few cycles. From fig. 5.7 it is observed that the source current changes with respect to the load and dc link voltage changes. At $t = 0.03\,\text{sec}$ the source current magnitude reduces due to reduction of load and the source current magnitude increases to it is original value at $t = 0.065\,\text{sec}$

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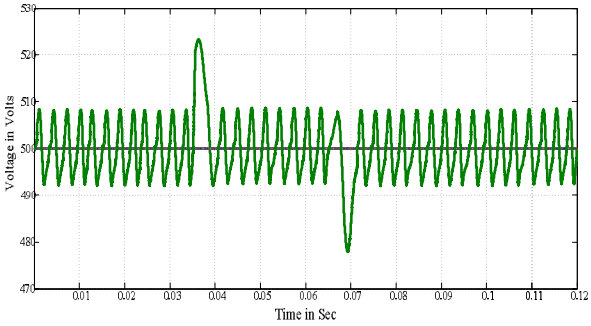

Fig. 5.6 DC link voltage variation in three level HCC levels

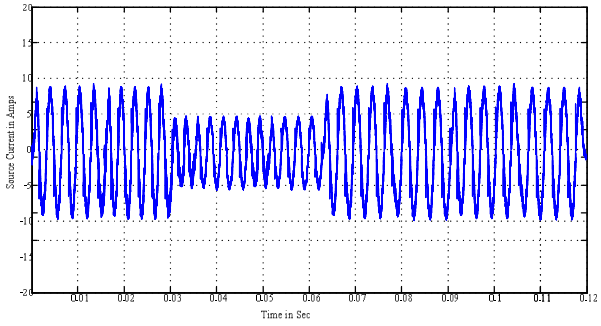

Fig. 5.7 Source current after compensation in three HCC under transient condition.

Source current paramet er	Simulation			Hardware		
	Phase -A	Phase -B	Phase -C	Phase -A	Phase -B	Phase -C
Peak value	17.02	13.42	14.03	3.48	2.68	3.02
% THD	7.48	8.82	8.62	6.54	7.63	7.48

Table 6.1 %THD comparison in simulation and Experimental studies

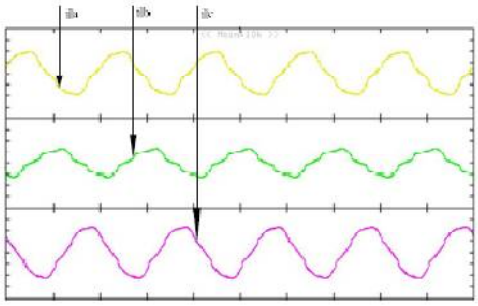

Fig. 5.8 Three phase unbalanced load or source currents before compensation

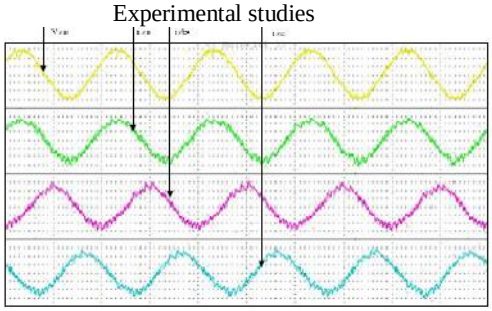

Fig. 5.9 Three phase actual filter currents

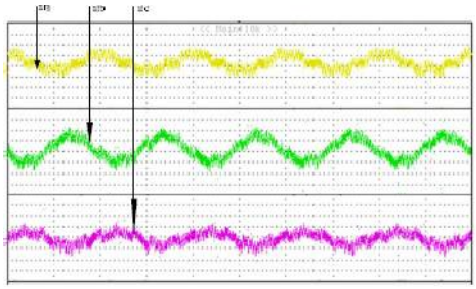

Fig. 5.10 Three phase source currents after compensation with phase-A source voltage

In Fig. 5.5 shows the unbalanced load or source currents before compensation due to unbalanced non liner load. After compensation the source current found unbalanced and distorted because of generation of compensator currents are not independent as shown in Fig. 5.6. The %THD variation shown in table 6.3 is found that the distortion is above the normal limits of IEEE standards.

Fig. 5.8 shows the unbalanced non linear load currents, the compensator has to inject harmonics currents with equal magnitudes of load current and opposite phase angle at PCC. The filter injected currents are shown in Fig. 5.9 .In this it is observed that the filter currents are equal in magnitudes but opposite in phase angle. Fig. 5.10 shows the compensated source currents in three phases with respect to compensated source voltage in phase-A which are almost sinusoidal in nature and in phase with their respective source voltages after compensation

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VII. CONCLUSION

This paper presents a state space model for three phase four wire systems with non stiff source. A control algorithm has proposed to compensate AC and DC components under unbalanced non linear load conditions. Initially a fixed unbalanced load will be considered in three phases along with non linear load. It is observed that after compensation the source currents are balanced and in phase with source voltage. The source currents observed balanced even after increasing the load in all three phases. A three level hysteresis current controller has been used to generate switching commands for inverter switches.

BIOGRAPHY

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