ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 6, June 2017

Adiabatic Array Logic Design of 4x1 MUX and 8x1 MUX without Redundancy

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ABSTRACT: Adiabatic array logic allows designing low power digital circuits with more power saving despite having an equal number of transistors with the conventional CMOS logic style and 2PASCL In this paper, 4x1 MUX and 8x1 MUX is designed using Adiabatic Array Logic and by removing redundant transmission gates from Adiabatic Array Logic. The proposed designed shows the reduced power dissipation and also transistor count in comparison with basic Adiabatic Array Logic design. The comparison of power dissipation is also carried out with sinusoidal power supply over a frequency range of 100MHz-600MHz. The simulations are carried out in Cadence Virtuoso at 180nm technology, 1.8V CMOS standard process technology.

KEYWORDS: Adiabatic logic; Adiabatic Array Logic; charge recovery; power consumption; redundancy; power saving

I.INTRODUCTION

The increasing demand of mobile devices and the need to limit power consumption in VLSI chips led to rapid and innovative developments in low power circuit design during recent years [6]. The main motive behind these developments is mobile devices requiring low power consumption and high throughput. In low power design techniques, adiabatic logic circuits break the lower limit of the energy dissipation in static CMOS which equals to C $V_{DD}^2/2$ by using AC power supply instead of the DC power supply. There are several adiabatic logics [4][7][8] have been developed in several years. Adiabatic Array Logic [1][2][3] is new adiabatic technique which is recently proposed. It employs an AND plane of transmission gates to realize ANDed terms and a wired OR-plane to OR them. Before the actual work is discussed, a brief theory of adiabatic and CMOS logic along with Adiabatic Array Logic is shown.

Consider a CMOS inverter with DC supply voltage V_{DD} . The energy dissipation during charging/discharging cycle of load capacitance is given by

$$E_{CMOS} = \frac{1}{2}\alpha C_L V_{DD}^2 \tag{1}$$

where α is the switching probability.

In adiabatic inverter circuit, the energy dissipation during charging/discharging is given by:

$$E_{adia\_diss} = 2\frac{RC}{T}CV_{DD}^2 \tag{2}$$

The above equation shows that this energy loss is inversely proportional to the charging time, T. This implies that slower the capacitor is charged, lesser energy will be dissipated. Also energy dissipation governed by the resistance R which is not in case of the CMOS logic.

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As adiabatic logic aims to minimize the energy dissipation, we have to:

$$E_{AL} < E_{CMOS}$$

Or

$$2\frac{RC}{T}CV_{DD}^{2} < \alpha\frac{1}{2}CV_{DD}^{2}$$

Or

$$T > 4\frac{RC}{\alpha} \tag{3}$$

This condition is required for adiabatic logic to better than the static CMOS logic. The physical significance of equation (3) is that the charging time T of the capacitor should be high i.e., the charging process should be slow. This is achieved by using a AC supply such as ramp or sinusoidal voltage instead of the DC voltage.

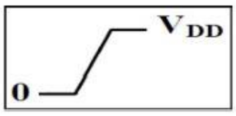

Figure 1. Ramp voltage

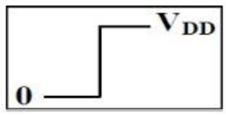

Figure 2. DC voltage

Ramp voltage used in adiabatic logic is called the power clock. It has four intervals: evaluate (E), hold (H), recover (R) and wait (W), as shown in Fig.3.

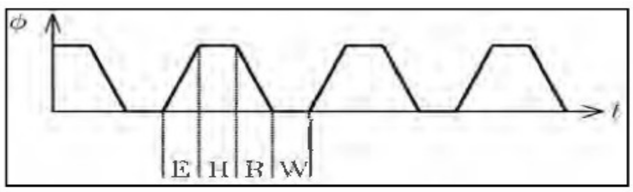

Fig.3. Phase in an Adiabatic Power Supply

The adiabatic array logic is driven by a sinusoidal power supply, the power clock. The logic is shown below:

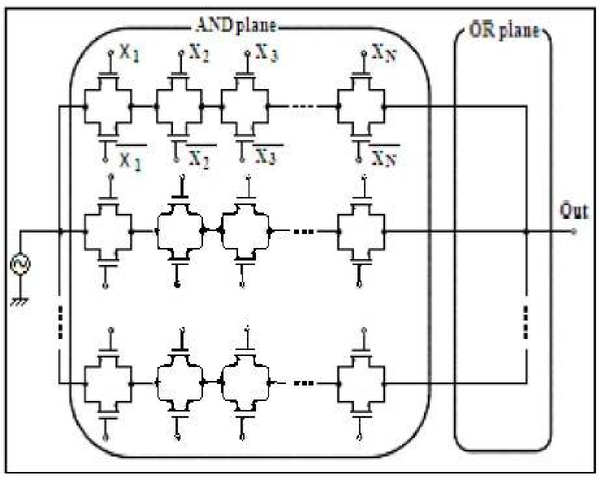

Fig.4. Adiabatic Array Logic

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Vol. 6, Issue 6, June 2017

It consists of an array of transmission gates to form AND plane and wired OR plane. This circuit can be analyzed by transmission gate in the ON state represented with a linear model made up of a resistance R and a capacitance C [5] at the output node as shown in Fig.4.

$$R = \frac{1}{V_{DD}} \left[\begin{array}{l} \dfrac{1}{\mu_n C_{ox} \dfrac{W_n}{L_n}} \ln\left(\dfrac{V_{DD} - V_{tn}}{V_{DD} - V_{tn} - |V_{tp}|}\right) + \\ \dfrac{1}{\mu_p C_{ox} \dfrac{W_p}{L_p}} \ln\left(\dfrac{V_{DD} - |V_{tp}|}{V_{DD} - V_{tn} - |V_{tp}|}\right) + \\ \dfrac{1}{\mu_p C_{ox} \dfrac{W_p}{L_p} - \mu_n C_{ox} \dfrac{W_n}{L_n}} \ln\left(\dfrac{\mu_p \dfrac{W_p}{L_p}}{\mu_n \dfrac{W_n}{L_n}}\right) \end{array} \right] \tag{4}$$

Assuming the triode region for both PMOS and NMOS transistors, the capacitance C is given by:

$$C_{ON} = W(\frac{1}{2}L + \Delta L)C_{ox} + C_{jB} \tag{5}$$

where, ΔL is the overlap and capacitance C_{jB} is due to the junction between the diffusion and the bulk.

II.PROPOSED WORK

The Adiabatic Array Logic designs have some repeated transmission gates which consumes area as well as power. Therefore it is necessary to make the adiabatic array logic redundant. Here, we have taken two circuits 4x1 MUX and 8x1 MUX to compare basic Adiabatic Array Logic and Redundant Adiabatic Array Logic.

A multiplexer [10][15] (or MUX) is a device that selects one of several input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has *n* select lines, which are used to select which input line to send to the output.

4x1 Multiplexer has 4 inputs, 2 select lines and 1 output line. The select lines select one of the data and give it to the output. The expression for the 4x1 MUX is shown below:

$$Y = \overline{S1}\,\overline{S0}I0 + \overline{S1}S0I1 + S1\overline{S0}I2 + S1S0I3 \tag{6}$$

8x1 Multiplexer has 8 inputs, 3 select lines and 1 output line. The select lines select one of the data and give it to the output. The expression for the 8x1 MUX is shown below:

$$\begin{aligned} Y = {} & \overline{S3}\,\overline{S1}\,\overline{S0}I0 + \overline{S3}\,\overline{S1}S0I1 + \overline{S3}S1\overline{S0}I2 + \overline{S3}S1S0I3 + \\ & S3\overline{S1}\,\overline{S0}I4 + S3\overline{S1}S0I1 + S3S1\overline{S0}I2 + S3S1S0I3 \end{aligned} \tag{7}$$

Their proposed circuits are shown in figures which are designed using Cadence Virtuoso at 180nm, 1.8V CMOS standard process technology with W/L=0.6µm/0.18µm for both PMOS and NMOS, $V_{clk} = 1.8V$ (peak-to-peak), and

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ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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Website: www.ijareeie.com

Vol. 6, Issue 6, June 2017

load capacitance 0.01pF. Simulating these circuits provided the output waveforms, below their respective circuits. Four terminal MOS transistors have been used whose substrate is connected to V_{DD} and ground for PMOS and NMOS respectively.

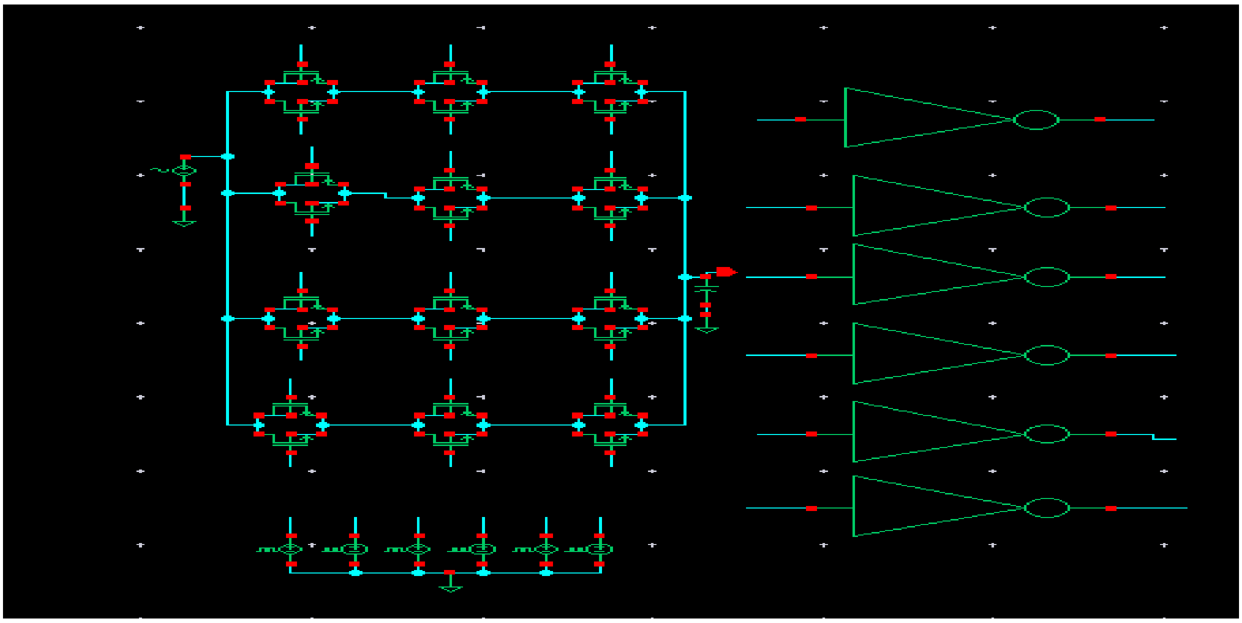

Fig.5(a).4x1 MUX using Adiabatic Array Logic

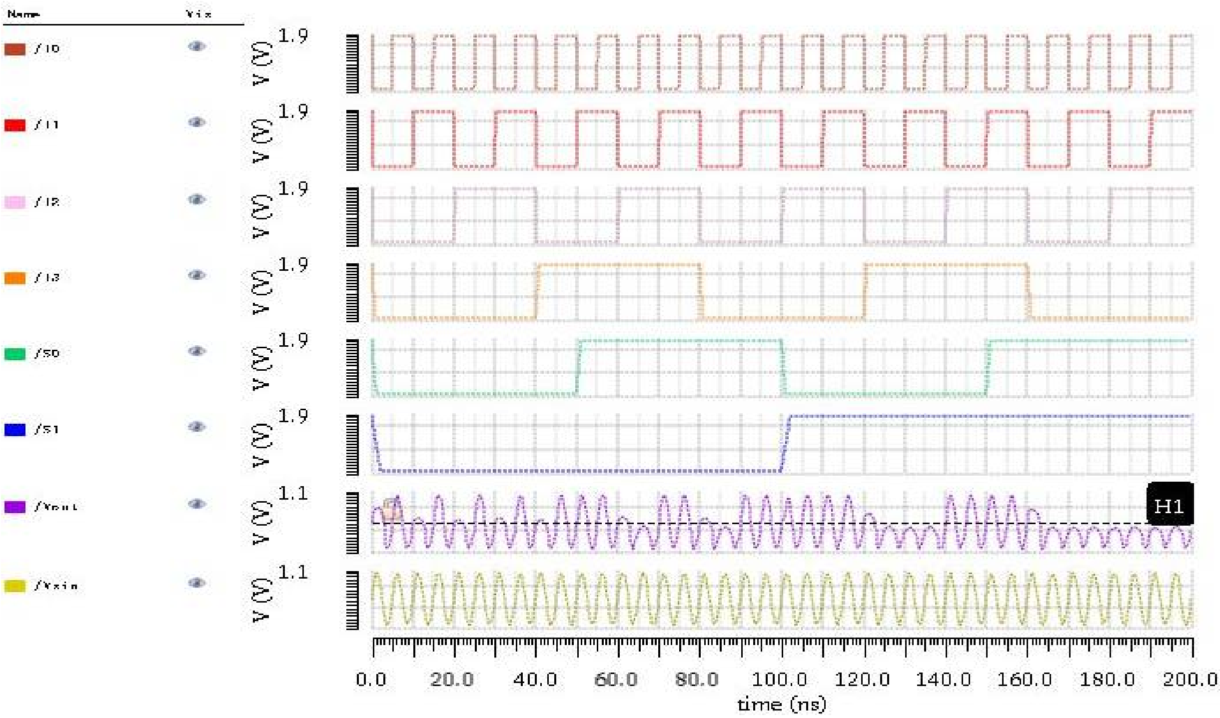

Fig.5(b).Output Waveform Of 4x1 MUX Adiabatic Array Logic

ISSN (Print) : 2320 – 3765
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Vol. 6, Issue 6, June 2017

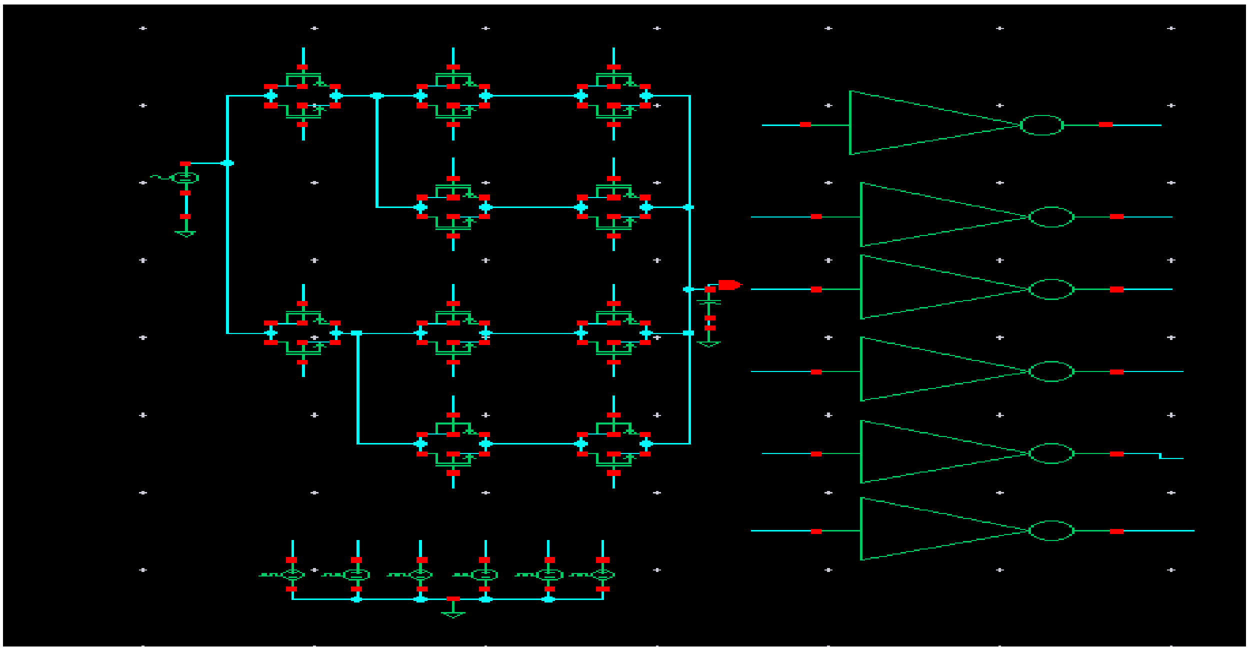

Fig.6(a). Proposed 4x1 MUX Adiabatic Array Logic without redundancy

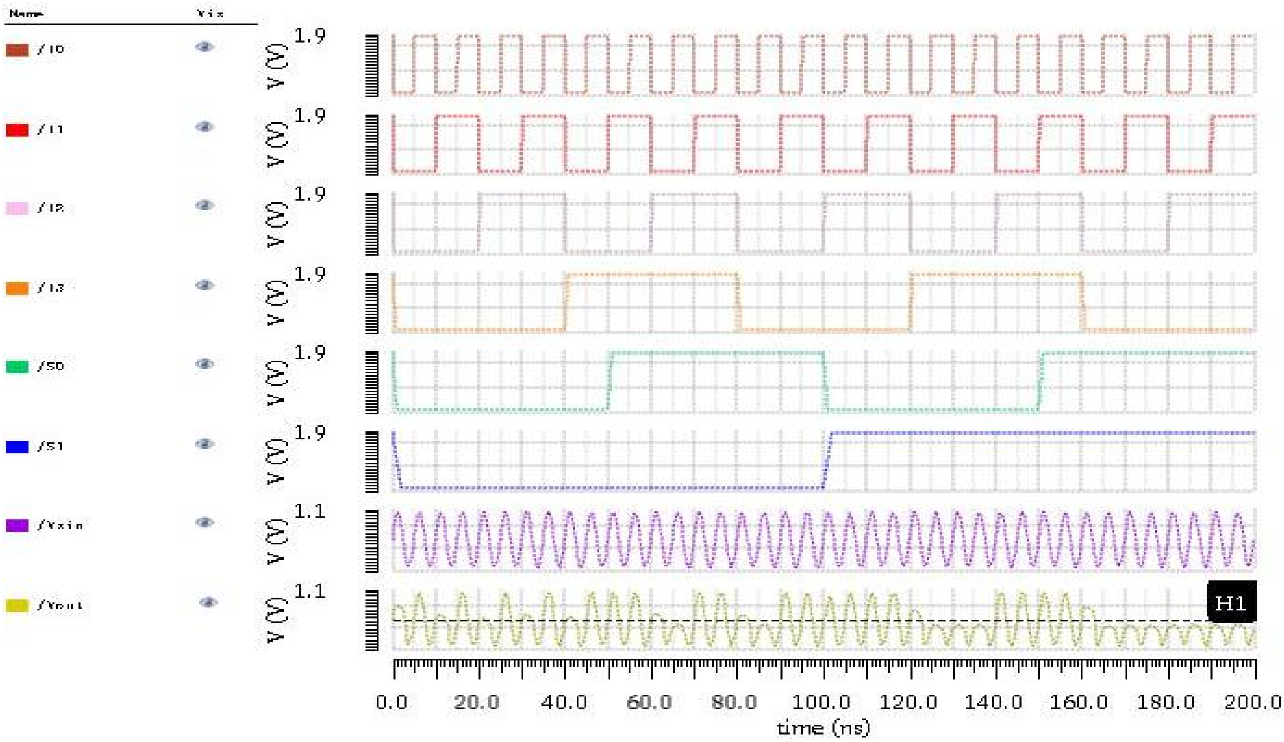

Fig.6(b).Output Waveform Of 4x1 MUX Adiabatic Array Logic without redundancy

ISSN (Print) : 2320 – 3765
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Vol. 6, Issue 6, June 2017

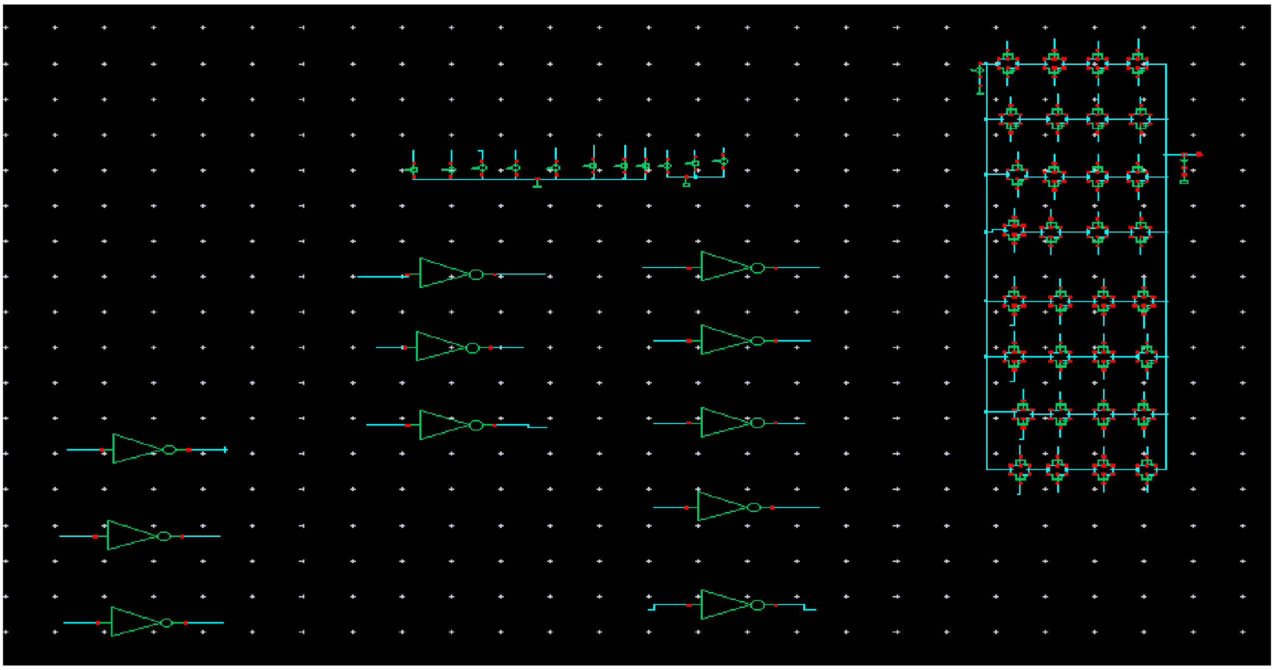

Fig.7(a).8x1 MUX using Adiabatic Array Logic

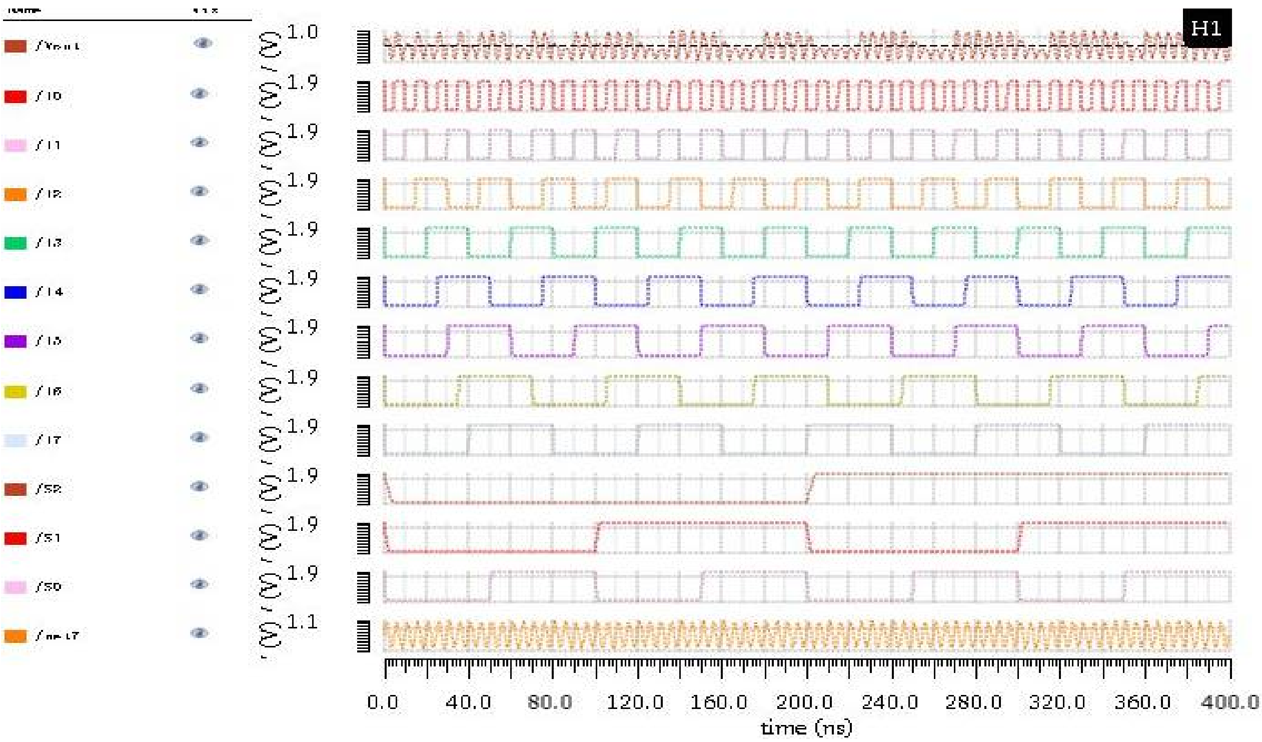

Fig.7(b). Output Waveform of 8x1 MUX using Adiabatic Array Logic

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Vol. 6, Issue 6, June 2017

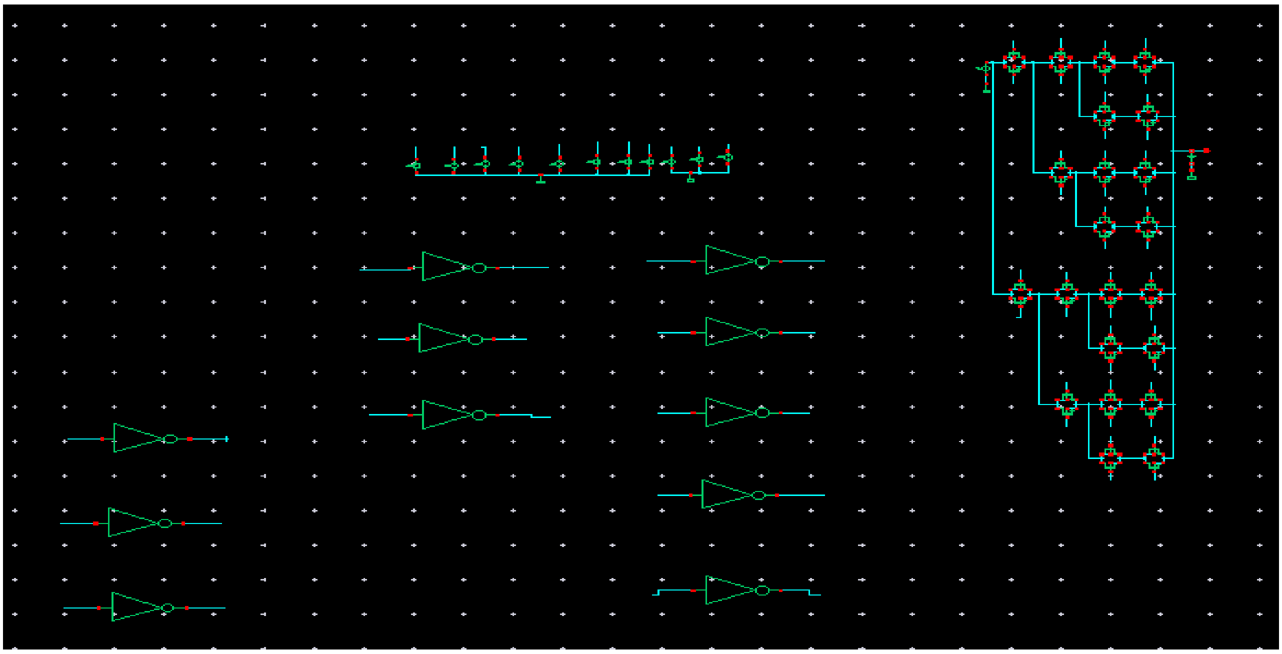

Fig.8(a). Proposed 8x1 MUX Adiabatic Array Logic without redundancy

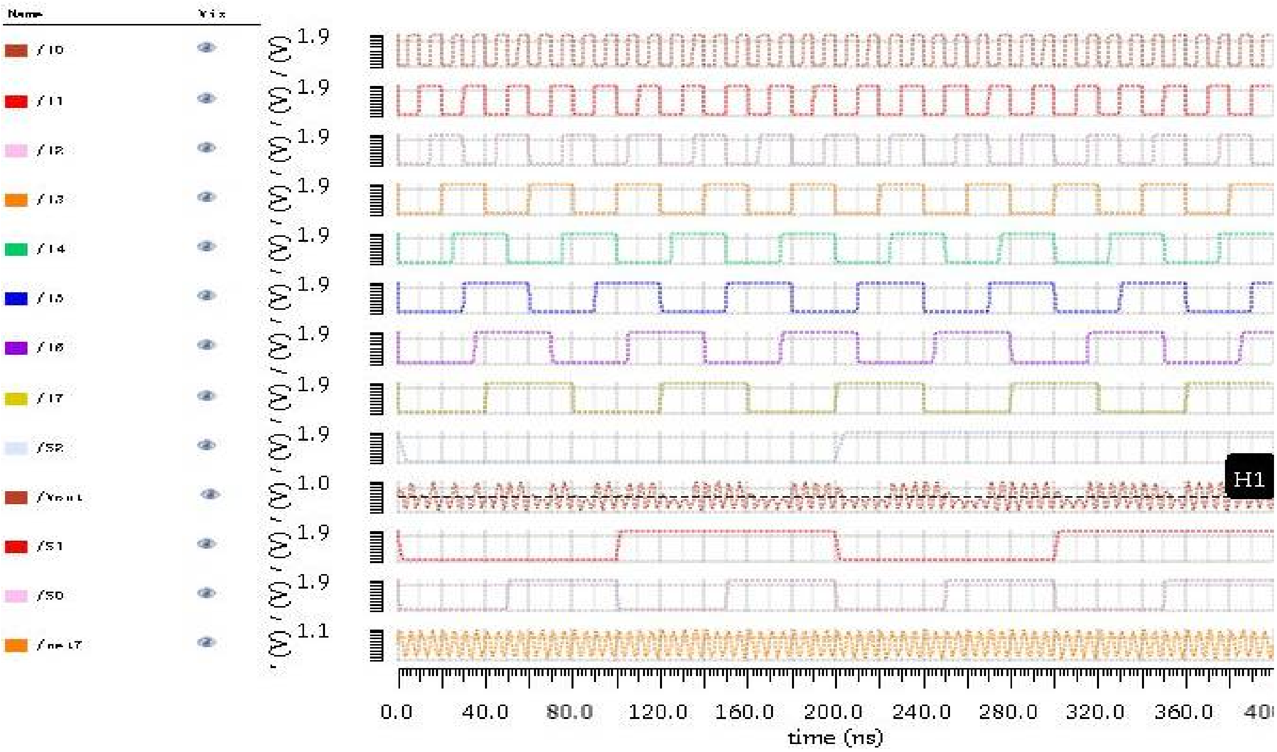

Fig.8(b).8x1 MUX using Adiabatic Array Logic without redundancy

ISSN (Print) : 2320 – 3765
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International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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Vol. 6, Issue 6, June 2017

III. RESULTS AND DISCUSSION

The total power dissipation of any circuit can be defined as the sum of the products of the voltage and current of all power sources present within the circuit. To calculate the power savings in the circuits, the energy consumption E is computed as below:

$$E = \int_0^{T_s} \left(\sum_{i=1}^{n} V_{pi} I_{pi} \right) dt \qquad (8)$$

Where $T_s(=1/f_s)$ = the period of the primary input signal; V_p = the power supply voltage, I_p = the power supply current, and i = number of power supply. Therefore, energy dissipation E is equal to the net energy flowing into the circuit from the power supply.

The propagation delay [5] of the circuit should be considered to measure performance of the circuit. The transmission gate can be modelled as an ohmic series resistance R bounded by capacitance by two grounded capacitance C. The step response delay t_D^{RC} of chain of RC element is given by

$$t_D^{RC} = \sum_{i=0}^{n} R_i C_i \quad \text{where i is no of node.} \qquad (10)$$

The total power dissipation and propagation delay of the proposed circuit and basic Adiabatic Array Logic circuits are evaluated by doing transient analysis at different frequency ranging from 100 MHz to 600 MHz of sinusoidal power supply. Area per chip is calculated by formula W*L*Transistor count.

TABLE I. PERFORMANCE ANALYSIS OF ADIABATIC ARRAY LOGIC STYLE AND CMOS LOGIC STYLE FOR 4X1 MUX AND ADIABATIC ARRAY LOGIC WITHOUT REDUNDANCY

Parameter	*Adiabatic Array Logic*	*CMOS logic*	*Adiabatic Array Logic without redundancy*
Transistor count	24	24	20
Area per chip(μm^2)	2.594	2.594	2.16
Total Power Dissipation(μW) at 200 MHz	5.316	7.452	5.121
Delay at 200MHz	6.023	5.359	5.976

TABLE II. POWER DISSIPATION OF ADIABATIC ARRAY LOGIC STYLE AND PROPOSED ADIABATIC ARRAY LOGIC 4X1 MUX AT DIFFRENT FREQUENCY OF SINUSOIDAL POWER SUPPLY

Frequency of Sinusoidal Power Supply (MHz)	*Total Power Dissipation(μW) of Adiabatic Array Logic Style*	*Total Power Dissipation (μW) of Adiabatic Array Logic Style Without redundancy*	*Propagation Delay(ns) of Adiabatic Array Logic*	*Propagation Delay(ns) of Adiabatic Array Logic Without redundancy*
100	4.475	4.317	51.910	51.860

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ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 6, June 2017

Frequency of Sinusoidal Power Supply (MHz)	*Total Power Dissipation(µW) of Adiabatic Array Logic Style*	*Total Power Dissipation (µW) of Adiabatic Array Logic Style Without redundancy*	*Propagation Delay(ns) of Adiabatic Array Logic*	*Propagation Delay(ns) of Adiabatic Array Logic Without redundancy*
200	5.316	5.121	6.023	5.976
300	8.484	5.943	7.385	7.331
400	9.770	7.422	5.586	5.545
500	12.640	8.667	5.512	5.465
600	16.070	10.730	5.418	5.412

TABLE III. PERCENTAGE CHANGE OF PARAMETERS OF PROPOSED DESIGN WITH RESPECT TO VARIOUS LOGIC STYLE FOR 4X1 MUX

Parameter	*Adiabatic Array Logic*	*CMOS logic*
Transistor count	20% Less	20% Less
Area per chip(μm^2)	20.09% Less	20.09% Less
Total Power Dissipation(µW) at 200 MHz	3.81% Less	45.51% Less
Delay at 200MHz	0.78% Less	10.32% More

TABLE IV. PERFORMANCE ANALYSIS OF ADIABATIC ARRAY LOGIC STYLE AND CMOS LOGIC STYLE FOR 8X1 MUX AND ADIABATIC ARRAY LOGIC WITHOUT REDUNDANCY

Parameter	*Adiabatic Array Logic*	*CMOS Logic*	*Adiabatic Array Logic without Redundancy*
Transistor count	64	64	44
Area per chip(μm^2)	6.912	6.912	4.752
Total Power Dissipation(µW) at 200 MHz	10.720	11.81	10.720

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(An ISO 3297: 2007 Certified Organization)

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Vol. 6, Issue 6, June 2017

Parameter	*Adiabatic Array Logic*	*CMOS Logic*	*Adiabatic Array Logic without Redundancy*
Delay at 200MHz	5.422	5.359	5.423

TABLE V. POWER DISSIPATION OF ADIABATIC ARRAY LOGIC STYLE AND PROPOSED ADIABATIC ARRAY LOGIC 8X1 MUX AT DIFFRENT FREQUENCY OF SINUSOIDAL POWER SUPPLY

Frequency of Sinusoidal Power Supply (MHz)	*Total Power Dissipation(µW) of Adiabatic Array Logic Style*	*Total Power Dissipation(µW) of Adiabatic Array Logic Style Without redundancy*	*Propagation Delay(ns) of Adiabatic Array Logic*	*Propagation Delay(ns) of Adiabatic Array Logic Without redundancy*
100	7.467	7.440	52.070	52.07
200	10.720	10.720	6.198	6.023
300	14.170	13.260	8.930	8.432
400	19.360	17.740	6.712	6.128
500	23.840	21.590	7.453	6.789
600	29.650	26.800	6.753	6.389

TABLE VI. PERCENTAGE CHANGE OF PARAMETERS OF PROPOSED DESIGN WITH RESPECT TO VARIOUS LOGIC STYLE FOR 8X1 MUX

Parameter	*Adiabatic Array Logic*	*CMOS logic*
Transistor count	45.45% Less	45.45%Less
Area per chip(μm^2)	45.45% Less	45.45% Less
Total Power Dissipation(µW) at 200 MHz	0 %	10.17% Less
Delay at 200MHz	0.01% Less	1.19% More

VI.CONCLUSION

In this paper, redundancy of the Adiabatic Array Logic is removed to achieve reduced power consumption and propagation delay. The proposed Adiabatic Array Logic has reduced no of transistor count in comparison with Adiabatic Array Logic and conventional CMOS Logic which has same number no of transistor count. At higher

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International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

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Vol. 6, Issue 6, June 2017

frequency, these circuits dissipate larger power. Though the propagation delays of these circuits are higher up to small content, these circuits are reliable with low frequency.

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