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Low Power Design of Johnson Counter using MTCMOS

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ABSTRACT: Semiconductor devices are aggressively scaled with every technology generation to accomplish high performance and high integration density. This leads to increase in power dissipation and increased delay. Low power and faster operation of a circuit has become inevitable for analogue as well as digital circuits. The digital circuit used for counting pulses is known as counter. The binary counter is a fundamental unit of computer or digital circuit operation. Counter is the widest application of flip-flops. A counter is one of the most useful digital circuits. Counters are used in many applications which are frequency dividers and frequency counters**.** In this paper, a power efficient design of Johnson counter is proposed. The design utilizes MTCMOS technique. All the simulations are carried out in Cadence Virtuoso Design Environment using 90nm TSMC technology. The analysis has been carried out on parameters like power, delay, energy and power-delay-product at different clock frequencies. Power dissipation is reduced by 77% for the proposed system.

I.INTRODUCTION

Due to VLSI minituarisation and scaling of devices have led to the increase in power consumption and leakage . The increase in density of integrated circuits and continuous reduction of the dimensions of devices and interconnections have increased complexity . In the nano-meter regime, a noteworthy segment of the total power consumption in high performance circuits is because of leakage currents. Since high performance systems are compelled to a predefined power budget, the leakage power diminishes the available power, affecting performance . Thus we need to develop the devices with higher performance Thus, techniques are important to reduce leakage power while keeping up the high performance. Also, as different components of leakage are getting important with technology scaling, every leakage reduction system needs re-evaluation in scaled advancements where sub-threshold conduction is not the only leakage mechanism. New low power circuit techniques are required to decrease total leakage in high performance nano-scale circuits. A range of circuit techniques including clock gating, transistor sizing, various dynamic supply voltage are there to lessen the dynamic power. For low-leakage design ,different circuit strategies including, multi threshold complimentary MOS, dynamic threshold complementary MOS , sleep transistor, natural stacking .

The fundamental unit of digital circuit operation is binary counter . The low voltage operation of a counter is helpful in the most part now in everyday chips basically. The goal of this paper is to develop a counter which saves power and energy of circuit by reducing the switching activity during inactive states of clock . Switching power constitutes about 70%-80% of energy dissipation . In this paper, we have reduced switching activity in circuits by clock gating technique and MTCMOS .

II. WORKING OF JOHNSON COUNTER

The johnson counter we are using here is only used for toggling the value of the data sequence provided to it .So ,the J-K port of j-k flip flop is always connected to 1, so that whenever there is a clock edge (positive or negative) flip- flop will change its value . We have designed a negative edge triggered system to avoid signal glitch. Positive triggering in our system produces signal glitches. That is why negative edge triggering is used to avoid any possibility of signal glitch.

Thus we have proposed the toggle based operation using Johnson counter or master slave flip-flop.We have considered here master slave structure of Johnson counter becoz the race around condition of Johnson counter due to toggle is

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removed . This type of strategy ensures low power operation eliminating all other conditions and keeping it active only for toggle operation . Thus system provides clock for flip-flop only for toggling and eliminate unnecessary clock operations ensuring least power dissipation . As we can see from the table that flip-flop Q_0 changes value only for clock pulses 2 and 6 . Similarly , flip-flop Q_1 changes value for clock pulses 3 and 7 . So, we can generate the logic considering only toggle time of each flip-flop .

$$Clk_{q0} = (\overline{Q_0 \ xor \ Q_3}).Clkmaster$$
$$Clk_{q1} = (Q_1 \ xor \ Q_0).Clkmaster$$
$$Clk_{q2} = (Q_2 \ xor \ Q_1).Clkmaster$$
$$Clk_{q2} = (Q_2 \ xor \ Q_1).Clkmaster$$

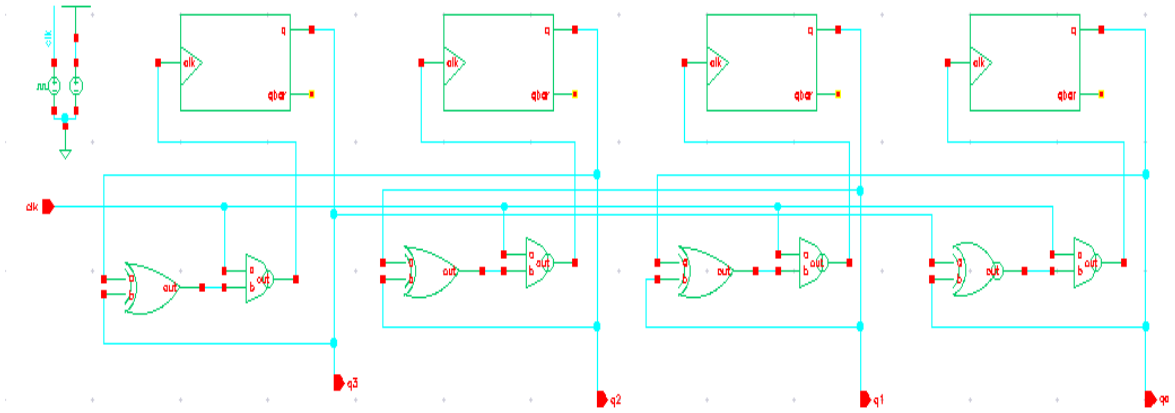
clock	Q_3	Q_2	Q_1	Q_0
1	1	1	1	1
2	1	1	1	0
3	1	1	0	0
4	1	0	0	0
5	0	0	0	0
6	0	0	0	1
7	0	0	1	1
8	0	1	1	1
9	1	1	1	1

Table I : pattern followed by Johnson counter

II. PROPOSED WORK

We have proposed a system using combinational circuitary (XOR gates , NAND gates and inverter) implemented by MTCMOS technique . In this paper , we have designed a Johnson counter using four master – slave flip flop . All flip flops are operated with clock gating system . Thus our design exhibit both clock gating technique and MTCMOS technique ensuring huge reduction in power and energy . The circuit is being operated at various frequencies and result have been tabulated .

The schematic of 4-bit Johnson counter is shown below :



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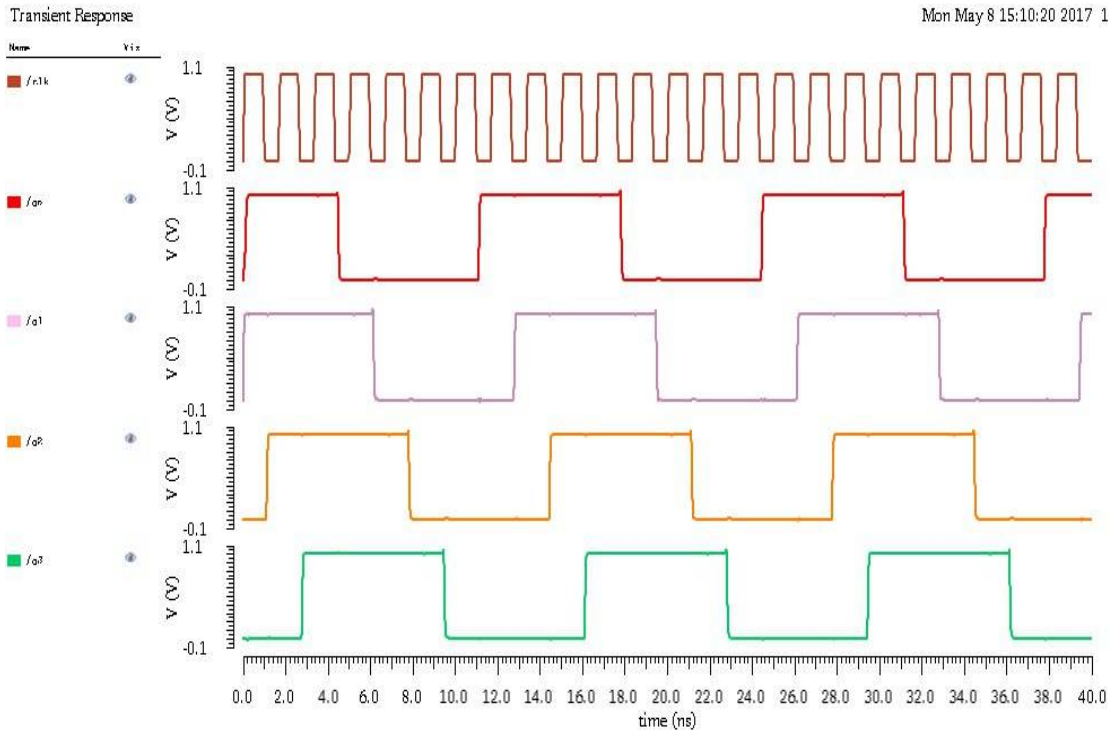
The output waveform is shown below :



III. RESULTS

Power dissipation has been minimized by 76.7% in our proposed system . and energy dissipation had been minimised by 76.80% . PDP is decreased by 59.40% in our proposed technique .

Conventional technique

Frequency	Power	Delay	PDP	Energy
600 MHz	63.97 u	109.7 p	7.016 f	2.559 p
700 MHz	73.61 u	109.7 p	8.073 f	2.945 p
800 MHz	83.06 u	109.7 p	9.109 f	3.332 p
900 MHz	92.69 u	109.7 p	10.16 f	3.708 p
1000 MHz	102.1 u	109.6 p	11.2 f	4.085 p

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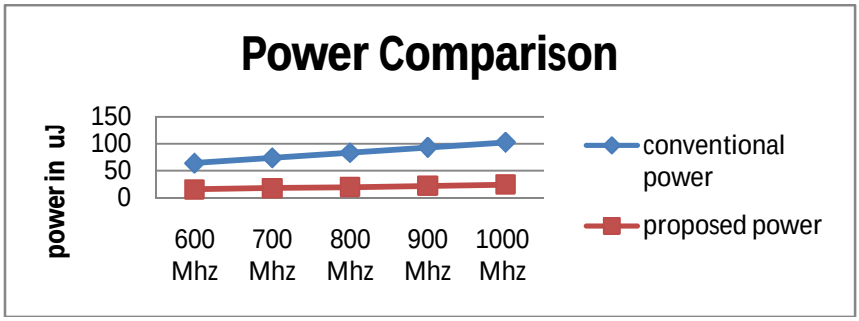
Modified technique

Frequency	Power	Delay	PDP	Energy
600 MHz	14.7 u	191.8 p	2.82 f	588 f
700 MHz	17.02 u	191.8 p	3.265 f	681 f
800 MHz	19.28 u	191.8 p	3.698 f	771.3 f
900 MHz	21.61 u	191.8 p	4.144 f	864.3 f
1000 MHz	23.87 u	191.7 p	4.576 f	954.8 f

IV. CONCLUSION

We have designed our system in several segments and all these segments are interconnected. In conventional design, there are some interconnections which may develop placement and routing issues being part of a bigger system as the conventional system is not segmented. The consecutive flip-flops are connected with each other in that system . But in our proposed system, there is no interconnections between different flip-flop blocks. All the outputs of the flip-flops are fed to the clock gating system where they are processed and necessary clock pulses are provided to the clock ports of different flip-flops. Thus, simpler and organized interconnection system is ensured in our proposed design.



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