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High Resolution Wide Dynamic Range for Programmable Delay Generator for Applications in Timing Spectroscopy

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ABSTRACT: Timing spectroscopy requires the measurement of the time interval between two physical events. Timing spectroscopy used in various applications in the field of nuclear instrumentation, time correlated single photon counting, time of flight, positron annihilation spectroscopy, coincidence detection and discrimination of neutron gamma discrimination. Such timing spectroscopy systems require calibration units for their testing. These calibration units can measure the timing error existing in the timing spectroscopy system.High Resolution Wide Dynamic Range Programmable Delay Generator of 1ns to 1us with resolution 1ns is used to calibrate timing spectroscopy systems. This paper introduces study, Design and implementation of High Resolution Wide Dynamic Range system which gives variable delay logic pulse to calibrate timing spectroscopy systems. Aim is to develop system which produced variable delay logic pulse from 1nanosecond to 1microsecond with 1 nanosecond resolution & 1 nanosecond accuracy.

KEYWORDS: Timing Spectroscopy, Programmable delay generator, time-to-amplitude converter

I .INTRODUCTION

Timing spectroscopy involves the measurement of the time relationship between two events. a time-pickoff circuit is employed to produce a logic output pulse that is consistently related in time to the beginning of each input signal. Ideally the time of occurrence of the logic pulse from the time-pickoff element is insensitive to the shape and amplitude of the input signals.a time-to-amplitude converter (TAC) can be used to measure the time relationship between correlated or coincident events seen by two different detectors that are irradiated by the same source. Figure.1is a simplified block diagram of a typical time spectrometer used for making this type of timing measurement.

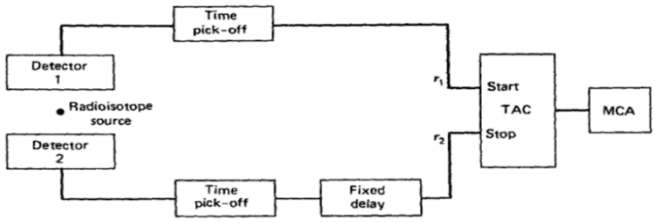

Fig.1 Block diagram of timing spectroscopy

a time-pickoff unit is associated with each detector, with the logic pulse from one time pickoff used to start the TAC and the delayed logic pulse from the other time pickoff used to stop the TAC. The TAC is usually implemented by charging a capacitor with a constant-current source during the time interval between a start input signal and the next stop input signal. The amplitude of the voltage on the capacitor at the end of the charging interval is proportional to

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the time difference between the two signals. .Most important characteristic of TAC is its linearity over entire the conversion ranges. Walk, jitter this types of error introduced non-linearity in the measurement. The amplitude information from the TAC is often applied to an MCA for accumulation of the data and display of the probability density of start-to-stop time intervals, commonly called a timing spectrum. Timing spectroscopy systems accuracy needs to be measured and hence calibration units are required.

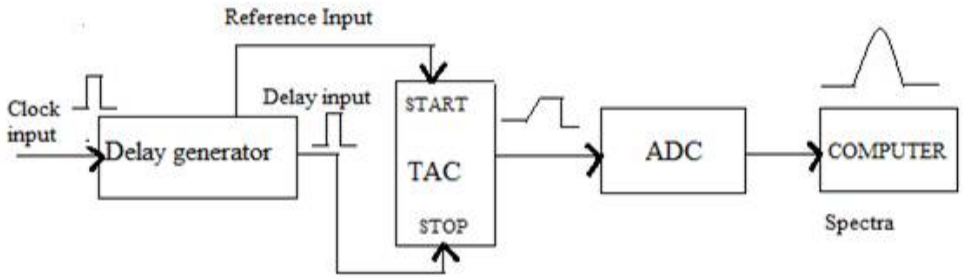

Fig 2. Block Diagram of System

Fig .2 shows design of calibration system of timing spectroscopy Systems.
In this Paper Introduced Programmable delay generator which produced variable delay logic pulse. The precise delay pulse applied to TAC.TAC was used to measure the delay time. The TAC was started by the Reference delay pulse signal of delay generator IC and stopped by its delayed pulse signal, the TAC result was digitized by an analog-to-digital (ADC) and after then a spectrum was created in a computer. Programmable delay generator system is used to calibrate timing spectroscopy system.

II. LITEARTURE SURVEY

A digitally-programmable method for linearly controlling signal delay over a wide frequency and delay range has been developed.Emitter degeneration or pre- or post-distortion techniques usually are needed to linearizethe relationship between voltage and delay. [1]
High Speed Multiple Pre-set Counter & Pulsed Crystal Oscillator Which Synchronized in constant phase with respect to random time Reference pulse, comprised a new precision Delay Generator.[7]
It described the system's composition in hardware and software view.This system is composed ofProgrammable gate arrays deserializer MAX3885, high-speed clock generator AD9517-1, DDR2 SDRAM, serializer and USB2.0 Controller.[9]
High timing-fidelity delay circuit because of engineering requirement and practical necessity. This high resolution delay circuit can also be used in other coincidence electronics designs that use the “timing-AND-logic” concept employed by some commercial PET systems because such systems also require a long delay to synchronize the timing trigger and the energy/position signals.[10]
The developed system is required to generate high-side (HS) and low-side (LS) signal in frequency range from 1 MHz to 15 MHz and duty cycle values from 5% to 50%. The most notable characteristic of the developed generator is the ability to adjust dead-times between the generated signals as precise as possible in order to use the signal generator for testing the semiconductor devices for synchronous DC-DC converter applications.[11]
The proposed delay generation system periodically measures and corrects the error and maintains it at the minimum value without requiring any special calibration phase. Up to 40 improvements in accuracy is demonstrated for a commercial programmable delay generator chip.[12]

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II. PROGRAMMABLE DELAY GENERATOR STRUCTURE & DESIGN

The operating principle of Programmable delay generator is as follows: A programmable delay generator delays pulse by a programmed amount of time. The delay through the device is controlled by an n-bit digital word. This is the programmed delay. Programmable delay generator internally makes use of ramp/comparator/DAC architecture as shown in figure 3. One input of a high-speed comparator is driven by a digital to-analog converter (DAC). The DAC is used to set a reference voltage at this comparator input. The other input is connected to a ramp generator. The ramp generator is started by applying a pulse to the trigger input of the delay generator. When the ramp voltage crosses the comparator, threshold set by the DAC, the output of the comparator switches. This output is delayed from the trigger pulse by an amount of time that is proportional to the DAC digital input code and the slope of the ramp. Altering the digital delay value changes the DAC output voltage, which alters the delay through the circuit.

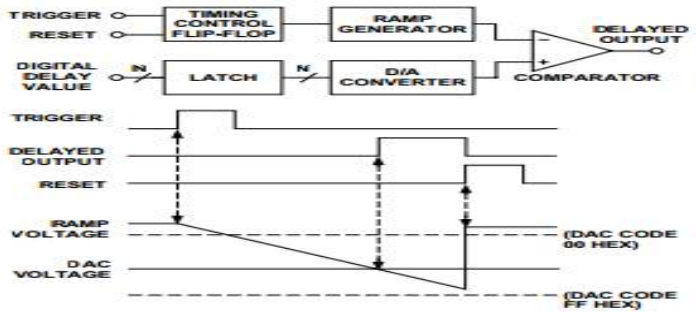

Fig 3. Working principle of programmable delay generator IC

a) Block Diagram

Fig 4 show programmable delay generator system. Design included two delay generator ICs & DIP Switches. Programmable delay generator generates delay logic pulse which varies from nanosecond to microsecond with 1ns step size. The entire range is not covered by using a single programmable delay generator IC. Thereby, two programmable delay generator ICs are used to generate variable delay from nanosecond to microsecond**.** DS1023-100 which delay pulse from 16ns to 255ns with 1ns step size and DS1023-500 which delay pulse from 16ns to 1275microsecond with 5ns step size. Input signal is TTL pulse. Output pulse is delayed by an amount of time that is proportional to the digital input code, Digital inputs are produced by DIP switch's, pulse then delay up to nanosecond to microsecond. To get 1 nanosecond resolution and 1 nanosecond accuracy cascade both the IC.as shown in figure 4.

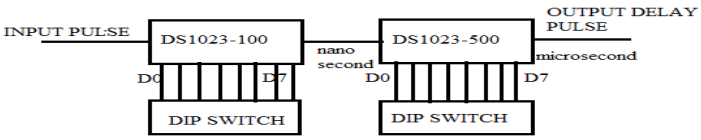

Fig 4. Structure of programmable delay generator system

b) Operating Principle

Programmable delay generator involve two Programmable delay generator ICs & DIP Switches To get 1 nanosecond resolution and 1 nanosecond accuracy cascade both the ICs as shown in above figure. DS1023-100 is calibrate by DS1023-500.Function Generator is used to provide input TTL Pulse in circuit. In first step DS1023-100, D1023-500 Have 00000000 addressed & hence input TTL pulse is delay by 32ns because of inherent delay of both ICs. To get minimum delay from 16ns output delay taken with respect to DS1023-100 Reference delay. So in first step required delay is from 16ns to 249 ns that is done with DS1023-100 with 1 ns step size at that time DS1023-500 is with

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00000000 Addressed. because of DS1023-100 having limited delay range input TTL pulse delay by 250 ns with DS1023-500 at that time DS1023 -100 is With 00000000 Addressed. Now the output pulse is delay by 250 ns, after this step required delay is 251ns to 499ns that is done with DS1023-100, DS1023-500 is with 00000000 Addressed. When it reaches to 499ns the DS1023-500 is set to 500 ns. Again repeat the procedure increase delay with 1ns step size up to 749 ns with the DS1023-100. 750ns set with DS1023-500**.**This procedure is followed tocover the range up to 1000ns with 1ns accuracy and 1ns resolution. Fig.5.Describe the Operation Of Programmable Delay Generator System.

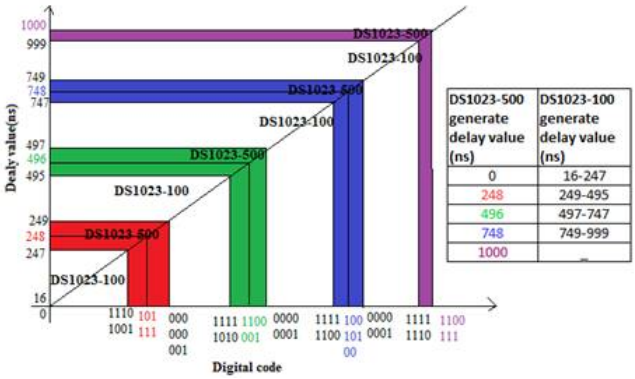

Fig.5.Operation of Programmable Delay Generator System

Table 1. Illustrate the processing of calibrate DS1023-500 IC with DS1023-100. Output of Programmable delay Generator system is 32ns for 00000000 Addressed.Reading was taken with respect to Reference Delay of DS1023-100.

Sr.No	Decimal Value DS1023-100	Decimal Value DS1023-500	Digital Addressed DS1023-100	Digital Addressed DS1023-500	Observed delay (ns)
1	0	_	0	_	16
_	_	_	_	_	_
2	233	_	11101001	_	247
3	_	47	_	101111	248
_	_	_	_	_	_
4	250	_	11111010		495
5	_	97	_	1100001	496
_	_	_	_	_	_
6	242	_	11111100	_	747
7	_	148	_	10010100	748
_	_	_	_	_	_
8	254	_	11111110	_	999
9	_	199	_	11000111	1000

Table.1. Calibration Reading

c) Reference Delay

In all delay lines there is an inherent, or step zero, delay caused by the propagation delay through the input and output buffers. In this device the step zero delay can be quite large compared to the delay step size. To simplify system design

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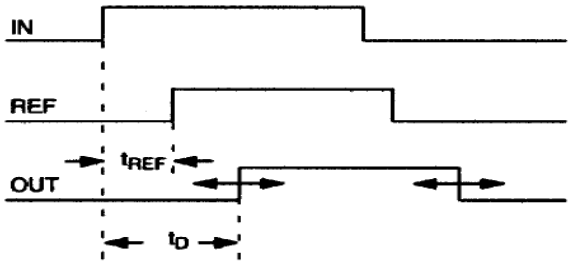
a reference delay has been included on chip which may be used to compensate for the step zero delay. In practice this means that if the device is supplied with a clock, for example, the minimum programmed output delay is effectively zero with respect to the reference delay.

d) Timing Diagram of the System



The timing diagram of overall system is shown in Fig 6
OUT is a copy of the input waveform that is delayed by an amount set by the programmed values. A programmed value of zero will still result in a non-zero delay. The signal on OUT is the same polarity as the input. REF is a fixed reference delay. It also is a copy of the input waveform but the delay interval is fixed to a value approximately equal to the Step Zero Value of the device.

III. RESULT AND DISCUSSION

We have designed and implemented a high resolution programmable delay generator. Programmable Delay Generator System Generate Variable Delay From 1ns to 1us with 1ns Accuracy & 1ns Resolution. All the performance tests have been done on an independent prototype circuit see figure 7.Two Programmable Delay Generator ICs are Used. Both ICs Have its Limited Range. To Cover Entire Range Cascade Both ICs. An Input to Programmable Delay Generator System is TTL pulse Which Delay by the Output of System with 32 ns with input Addressed Code is oooooooo.To Get Minimum Delay Output Is Taken with Respect to Ds1023-100 Reference Delay.

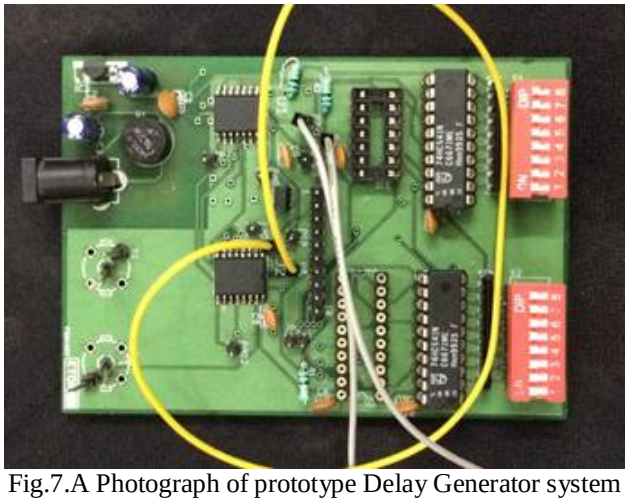


Fig.7.A Photograph of prototype Delay Generator system

Figure 8&9 shows delayed pulse signals, produced by the delay generator, on a Tektronix digital oscilloscope TDS3032 with an infinite display time. The oscilloscope was triggered by the rising-edge of the same pulse input to the delay generator. Since the delay timing only applied to the rising-edge not to the falling-edge. A less than ±290ps time

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jitter (resolution) of the rising-edge was measured. Programmable delay generator systems output from 16ns to 1000ns with 1ns step size & 1ns Resolution.

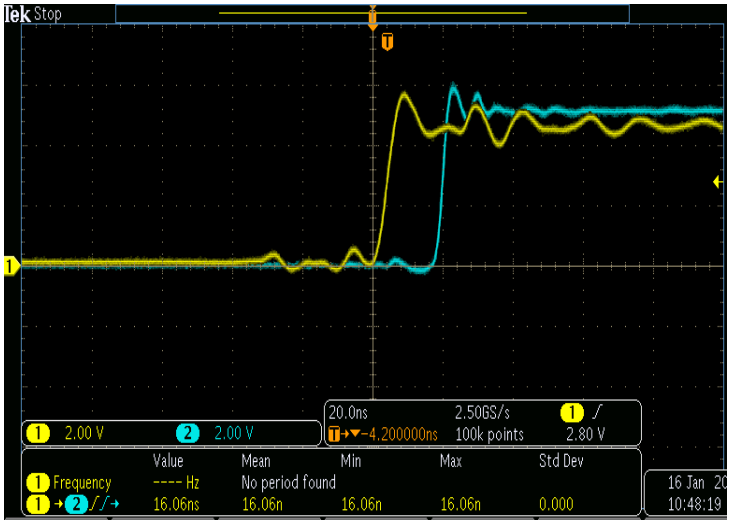

Fig.8.Input Pulse Delay by 16ns

In the Figure 8 Input Pulse Delay by 16ns When Input Digital Code is 00000000.This is Minimum Delay Taken With respect To DS1023-100 Reference Delay.

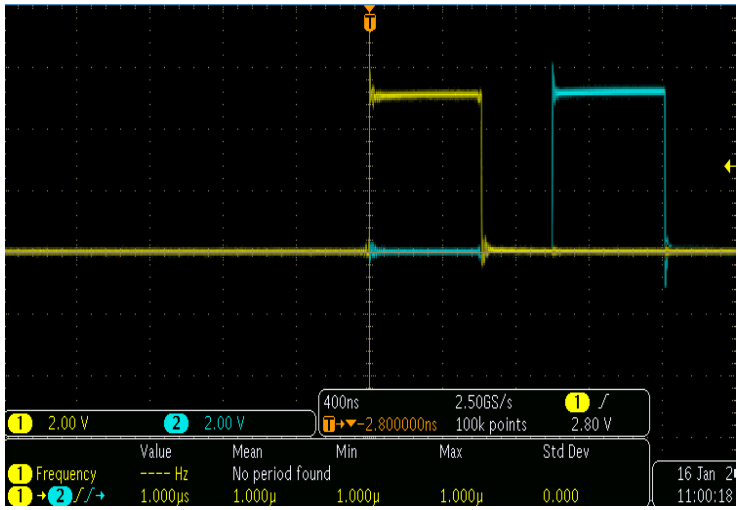

Fig.9Input Pulse Delay by 1000ns

In the Figure 9Input Pulse Delay by 1000ns When Input Digital Code is Maximum. This is Maximum Delay Taken With respect To DS1023-100 Reference Delay.

Figure.10. shows the observed Reading of Programmable Delay generator system with Addressed code.Graph Shows Digital Code Vs Observed Delay. Output of System for 00000000 Addressed code is 32ns, to get minimum delay from 16ns we take output reading with respect to DS1023-100 Reference Delay. Output Of the System Is Linear.

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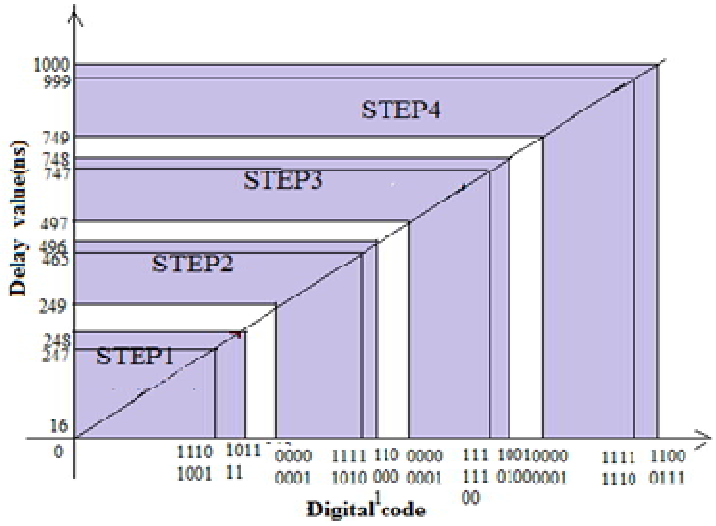

Fig.10 Observed Reading

Table 2shows the Observed Reading of Programmable Delay Generator System. The Entire Range Is Cover with Distributed Steps Which is The Combination of Both Delay Generator ICs.Programmable Delay Generator System Generate Delay from 16ns to 1us with 1ns Resolution & 1ns Accuracy.

STEP1		STEP2		STEP3		STEP4	
DS1023-100 Generate Delay Value(ns)	DS1023-500 Generate Delay Value(ns)	DS1023-100 Generate Delay Value(ns)	DS1023-500 Generate Delay Value(ns)	DS1023-100 Generate Delay Value(ns)	DS1023-500 Generate Delay Value(ns)	DS1023-100 Generate Delay Value(ns)	DS1023-500 Generate Delay Value(ns)
16-247	248	249-495	496	497-747	748	749-999	1000

Table 2.the Observed Reading of Programmable Delay Generator System.

IV.CONCLUSION

A programmable high-resolution delay generator has been designed and constructed. Our test results showed: (1) the delay generator had a less than ±290ps timing jitter that was essential for timing and coincidence measurement (2) the total delay range of the delay generator could be 16 ns to 1us with no performance degraded; (3) the delay time can be programmed at a coarse step of 16.7ns and a fine step of 1ns. This high-resolution delay generator is use in calibration of timing spectroscopy. This delay generator can also be used as a general device in other applications such as automatic test equipment and communications.

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