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Comparison of Voltage Quadrupler Boost Converter with Boost Converter

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ABSTRACT: Voltage quadrupler boost converter with high-voltage transfer gain and reduced semiconductor voltage stress is proposed in this paper along with comparison of boost converter. The proposed topology apply input-parallel output-series pattern for giving a much higher voltage gain excluding implementation of very large duty cycle. The proposed converter cannot only able to achieve maximize voltage gain with lowered component count but also lessen the voltage stress of both active switches and diodes. This will allow one to choose optimum lower voltage rating MOSFETs and diodes for minimizing both switching and conduction losses. Along with, due to the charge balance of the blocking capacitor, the converter highlights spontaneous uniform current sharing characteristics of two interleaved phase for voltage boosting mode comparatively than adding an additional circuitry or complex control techniques. The quadrupler boost converter voltages, currents and efficiency at different duty ratios are presented by comparing with boost converter. Some simulation results are presented to demonstrate the effectiveness of the proposed converter.

KEYWORDS: Automatic uniform current sharing, high boost converter, low voltage stress, transformer-less, voltage quadrupler.

I.INTRODUCTION

With global energy shortage and strong environmental movements, renewable or clean energy sources such as solar cells and fuel cells are increasingly valued worldwide. However, due to the inherent low voltage characteristic of these sources, a high step-up dc converter is essential as a prestage of the corresponding power conditioner [1]. The conventional boost and buck–boost converters [10] , due to the degradation in the overall efficiency as the duty ratio approaches unity. Obviously cannot fulfil the application need. Besides, the extreme duty ratio not only induces very large voltage spikes and increases conduction losses but also induces severe diode reverse-recovery problem.

Up to now many converters have been proposed to obtain maximum voltage gain. Those are dc-dc fly back converter and Phase-shifted full bridge converter etc [2]-[4]. These converters can provide large step-up voltage conversion ratios. Unfortunately, the voltage stress of diodes in those converters remains rather high and so many problems from these converters such as high voltage stress on switches, degradation in efficiency, high diode recovery problem, extra heavy circuit, etc [5]. So, in this paper, voltage quadrupler topology is proposed. It integrates two-phase interleaved boost converter to realize a high voltage gain and maintain the advantage of an automatic current sharing capability simultaneously [6]-[8].

The voltage quadruple topology is compared with the boost converter [11]-[12]. Furthermore, the voltage stress of active switches and diodes in the proposed converter can be greatly reduced to enhance overall conversion efficiency [9]. The efficiency and voltage gain of voltage quadrupler boost converter is high compare to boost converter is shown in simulation results.

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II. OPERATING PRINCIPLE OF THE BOOST CONVERTER

This is a dc-dc power converter with an output voltage greater than its input voltage. Boost converter is known as 'step-up chopper'. With the arrival of bipolar junction transistor (BJT) which is a self-commutated device it is used as a switch as an alternative of thyristor in dc-dc converters. It is having at least two semiconducting devices those are a diode and a transistor and at least one energy storage elements those are a capacitor, a inductor or both.

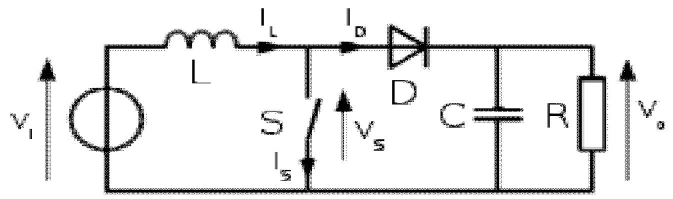

Fig1: Boost Converter

The operating principle of boost converter explained in moods. Those are ON-State and OFF-State.
ON-State: In this state the Switch S is closed. The inductor current will be raised.
OFF-State: In this state the Switch S is open. Then the inductor current flows across the diode D, capacitor C and the load R. The simulation diagram for Boost converter is shown in fig2.
The Corresponding Equations are:

Maximum Duty Cycle (D) = $1 - \frac{V_{in_{min}} * \eta}{V_{out}}$ (1)

Inductor current ripple (ΔI_L) = $\frac{V_{in_{(min)}} * D}{f_s * L}$ (2)

Inductor (L) = $\frac{V_{in}(V_{out} - V_{in})}{\Delta I_L f_s V_{out}}$ (3)

Capacitor(c) = $\frac{I_{out_{max}} * D}{f_s \Delta V_{out}}$ (4)

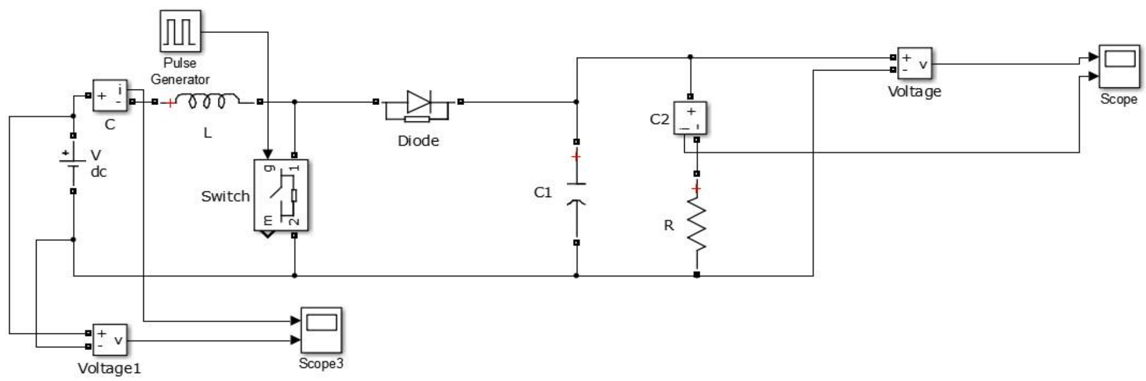

Fig2: Boost converter simulation diagram.

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III. OPERATING PRINCIPLE OF THE VOLTAGE QUADRUPLER BOOST CONVERTER

The voltage quadrupler boost converter uses two more extra capacitors and two more diodes, because of that during the energy transmission time divided inductor stored energy is stored in one capacitor and another divided inductor stored energy composed by the other capacitor energy store has transferred to the output to attain much higher voltage gain. Anyway, the voltage quadrupler boost converter efficiency is higher by comparing with boost converter at different duty ratios shown in fig11. The voltage gain of voltage quadrupler boost converter is high compare to boost converter. Also, the voltage stress of both active switches and diodes are less and uses automatic uniform current sharing ability without adding extra circuitry or control methods. The detailed operating principle is explained below.

The main objective is to obtain high voltage gain and such characteristic can only be achieved when the duty cycle is greater than 0.5 and in continuous conduction mode (CCM). Only for this case , However, with duty cycle lower than 0.5 or in DCM, as there is no enough energy transfer from the inductors to the blocking capacitors, output capacitors, and load side, and consequently it is not possible to get the high voltage gain as that for duty ratio greater than 0.5. Only with duty cycle larger than 0.5, due to the charge balance of the blocking capacitor, the converter can feature the automatic current sharing characteristic that can obviate any extra current-sharing control circuit.

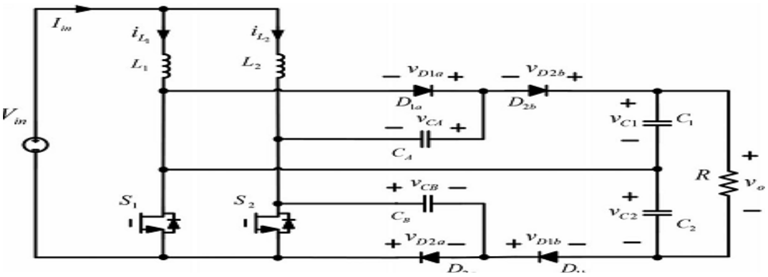
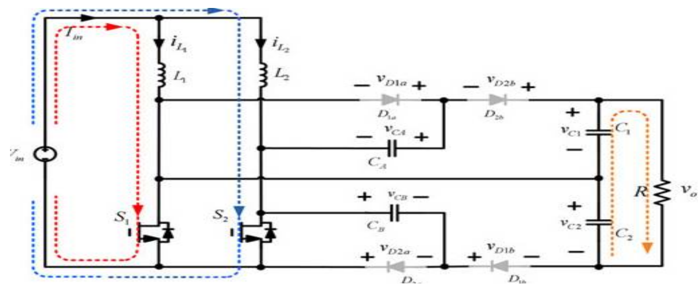


Fig3: voltage quadrupler boost converter

The operating principle of the voltage quadrupler boost converter can be classified into four modes. They are mode1, mode2, mode3, mode4.The current directions are also shown in figures.

Mode 1 ($t_0 \le t < t_1$): Switches S1 and S2 are turned ON. D_{1a} , D_{1b} , D_{2a} , D_{2b} are all OFF.



The Corresponding Equations are:

$$L_1 \frac{di_{L1}}{dt} = V_{in} \tag{5}$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} \tag{6}$$

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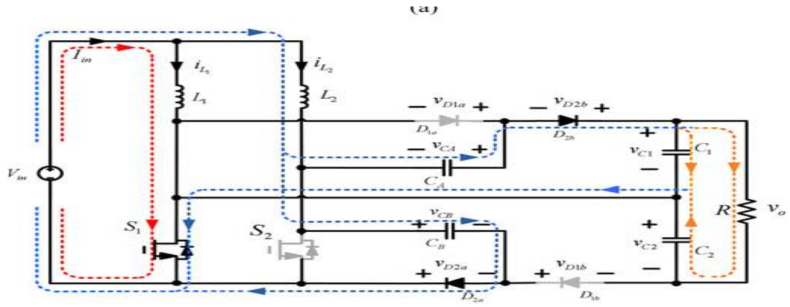
$$C_A \frac{dv_{C_A}}{dt} = 0 \quad (7)$$

$$C_B \frac{dv_{C_B}}{dt} = 0 \quad (8)$$

$$C_1 \frac{dv_{C_1}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R} \quad (9)$$

$$C_2 \frac{dv_{C_2}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R} \quad (10)$$

Mode 2 ($t_1 \leq t < t_2$): For this operation mode, switch $S1$ remains conducting and $S2$ is turned OFF. Diodes D_{2a} and D_{2b} become conducting.



The Corresponding Equations are:

$$L_1 \frac{di_{L1}}{dt} = V_{in} \quad (11)$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} + v_{C_A} - v_{C_1} = V_{in} - v_{C_B} \quad (12)$$

$$C_A \frac{dv_{C_A}}{dt} = i_{C_B} - i_{L_2} \quad (13)$$

$$C_B \frac{dv_{C_B}}{dt} = i_{C_A} + i_{L_2} \quad (14)$$

$$C_1 \frac{dv_{C_1}}{dt} = -i_{C_A} - \frac{(v_{C_1} + v_{C_2})}{R} \quad (15)$$

$$C_2 \frac{dv_{C_2}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R} \quad (16)$$

Mode 3 ($t_2 \leq t < t_3$): Both S1 and S2 are on. D_{1a} , D_{1b} , D_{2a} , D_{2b} are all OFF.

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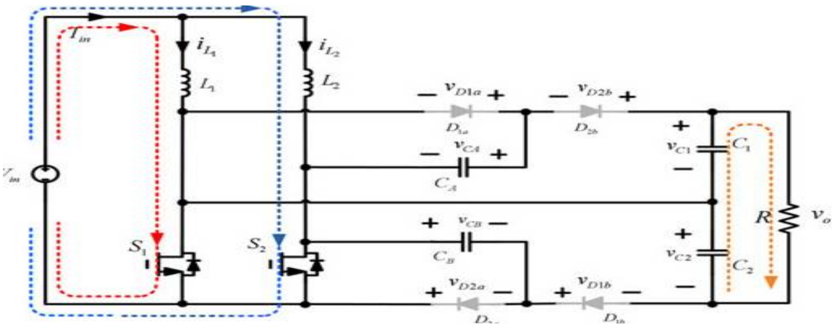


The Corresponding Equations are:

$$L_1 \frac{di_{L1}}{dt} = V_{in} \tag{17}$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} \tag{18}$$

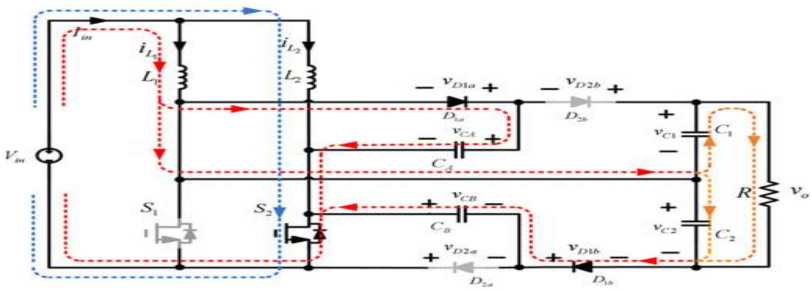
$$C_A \frac{dv_{C_A}}{dt} = 0 \tag{19}$$

$$C_B \frac{dv_{C_B}}{dt} = 0 \tag{20}$$

$$C_1 \frac{dv_{C_1}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R} \tag{21}$$

$$C_2 \frac{dv_{C_2}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R} \tag{22}$$

Mode 4($t_3 \leq t < t_4$): For this operation mode, switch $S2$ remains conducting and $S1$ is turned OFF. Diodes D_{1a} and D_{1b} become conducting. The part of stored energy in inductor $L1$ as well as the stored energy of C_B is now released to output capacitor $C2$ and load. Meanwhile, part of stored energy in inductor $L1$ is stored inC_A. In this mode, the output capacitor voltage $VC2$ is equal to V_{CB} plusV_{CA}.



The Corresponding Equations are:

$$L_1 \frac{di_{L1}}{dt} = V_{in} - v_{C_2} + v_{C_B} = V_{in} - v_{C_A} \tag{23}$$

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$$L_2 \frac{di_{L2}}{dt} = V_{in} \tag{24}$$

$$C_A \frac{dv_{C_A}}{dt} = i_{C_B} + i_{L_1} \tag{25}$$

$$C_B \frac{dv_{C_B}}{dt} = i_{C_A} - i_{L_1} \tag{26}$$

$$C_1 \frac{dv_{C_1}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R} \tag{27}$$

$$C_2 \frac{dv_{C_2}}{dt} = -i_{C_B} - \frac{(v_{C_1} + v_{C_2})}{R} \tag{28}$$

The voltage quadrupler boost converter is designed in such a way that, it should boost the input voltage. The converters part contains two MOSFET's for switching action. For this MOSFET, gate pulses are given by driver circuit. The simulation diagram for quadruple boost converter is shown in fig4.

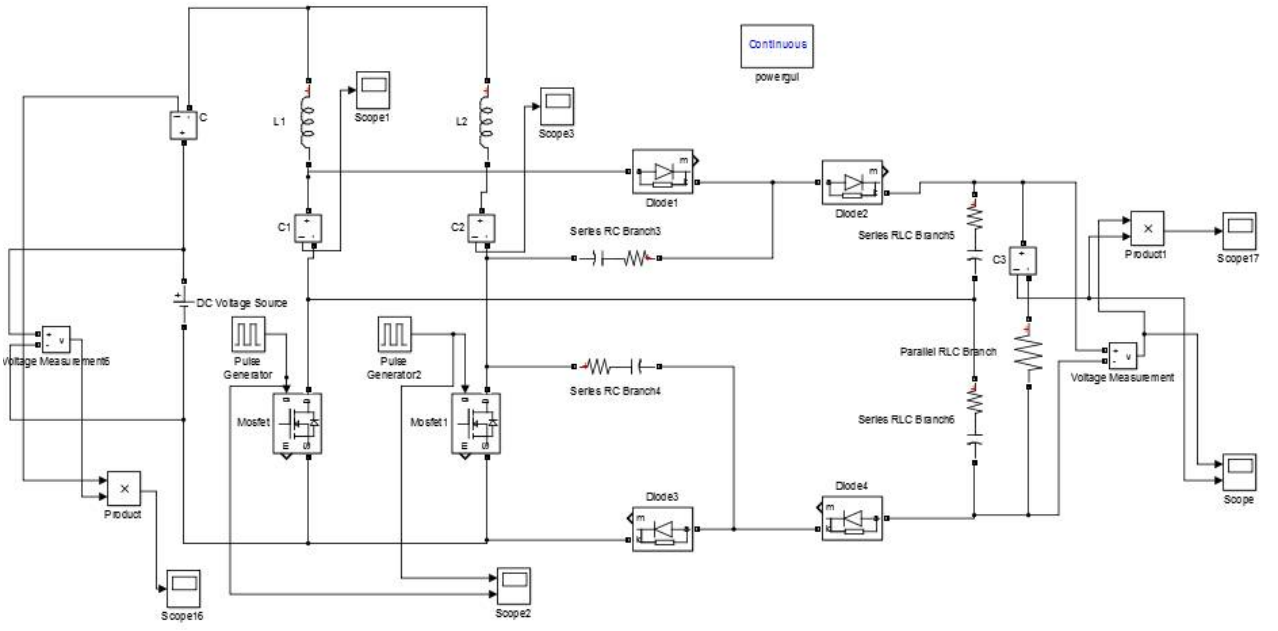

Fig4: Quadrupler boost converter simulation diagram

IV. SIMULATION RESULTS

To make better understanding of voltage quadrupler boost converter, first simulation is done. In simulation 394 Volt output voltage is observed against 25 volt input voltage for 0.76 duty ratio. Current ripples are getting down because of blocking capacitor. The 2 Mosfets are triggered by gating pulses. The gating pulses are given for different duty ratios. In below figure is also shows 394 volt boost of voltage against 25 volt input for Quadruple boost converter. The efficiency of both converters is compared in table 1.

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Duty Ratio	Boost Converter Efficiency(η)	Voltage Quadrupler Boost Converter Efficiency(η)
76%	47.71	92.5
50%	40.99	83.3
25%	48.1	73.3

Table 1:-Efficiency comparison of Boost Converter and Proposed Converter for different duty ratios.

In The Fig 5, it shows the graph of time Vs voltage .The output voltage waveforms for different duty ratios of quadruple boost converter are shown in fig 5.

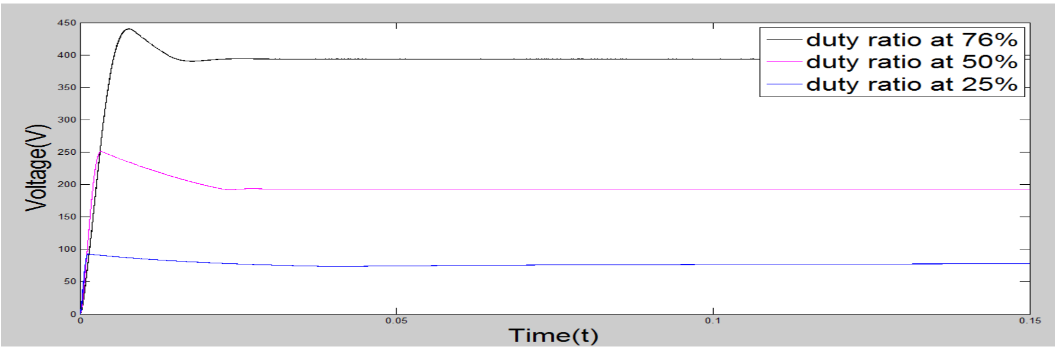

Fig 5: voltage waveforms of Quadruple Boost Converter for different duty ratios.

In The Fig 6, it shows the graph of time Vs current. The output current waveforms for different duty ratios of quadruple boost converter are shown in fig 6.

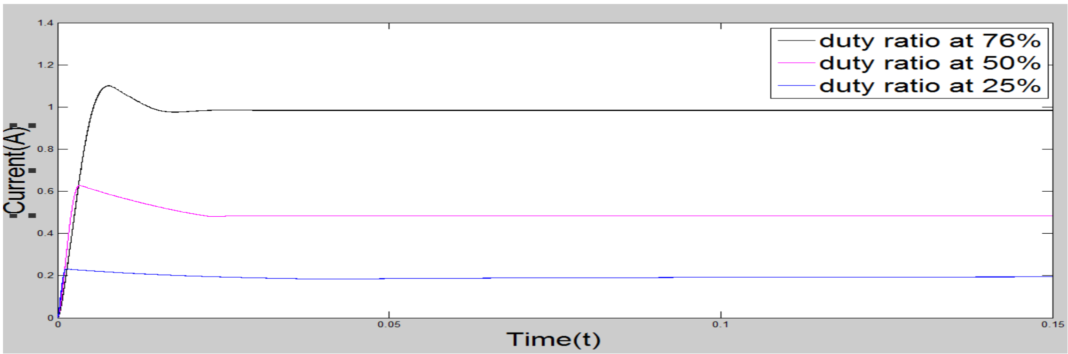

Fig 6: Current waveform of Quadruple Boost Converter for different duty ratios.

In The Fig 7, it shows the graph of time Vs voltage .The output voltage waveforms for different duty ratios of boost converter are shown in fig7.

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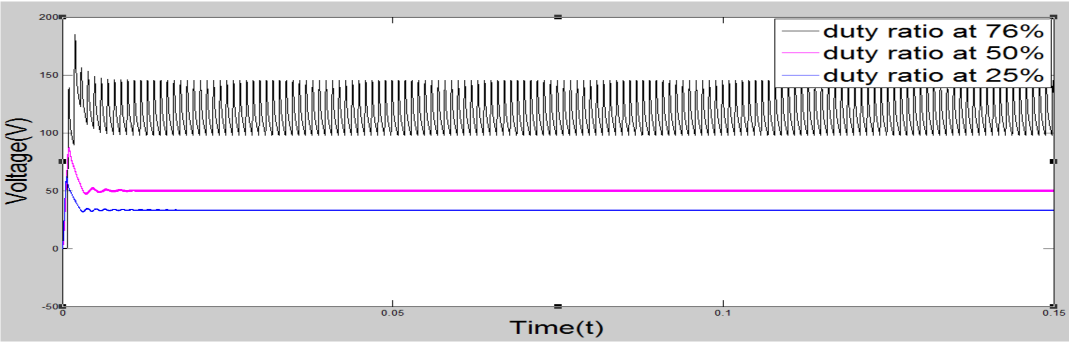

Fig 7: output voltage waveforms of boost converter for different duty ratio's.

In The Fig 8, it shows the graph of time Vs current. The output current waveforms for different duty ratios of quadruple boost converter are shown in fig 8.

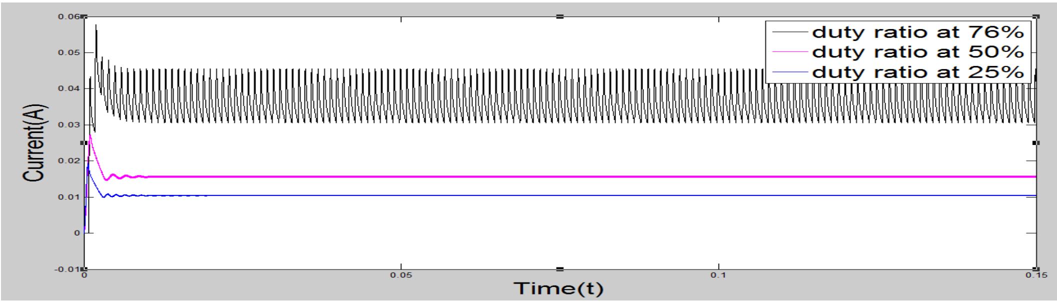

Fig 8: output current waveforms of boost converter for different duty ratio's.

In The Fig 9, it shows the graph of time Vs amplitude. The pulses given to pulse generator of Quadruple Boost Converter is shown in fig 9.

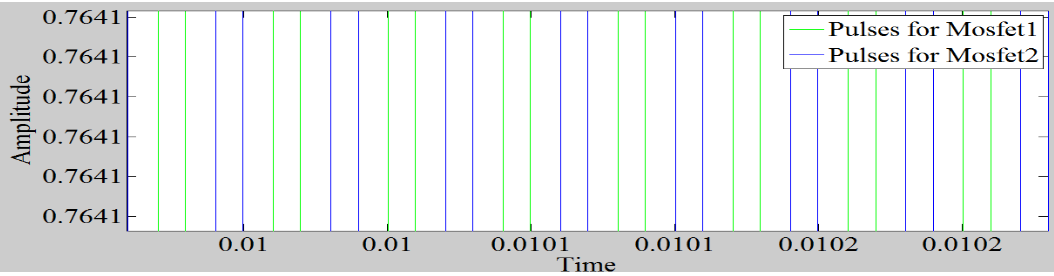

Fig 9: pulses for Quadruple Boost Converter

In The Fig 10, it shows the graph of time Vs amplitude. The pulses given to pulse generator of Boost Converter is shown in fig 10.

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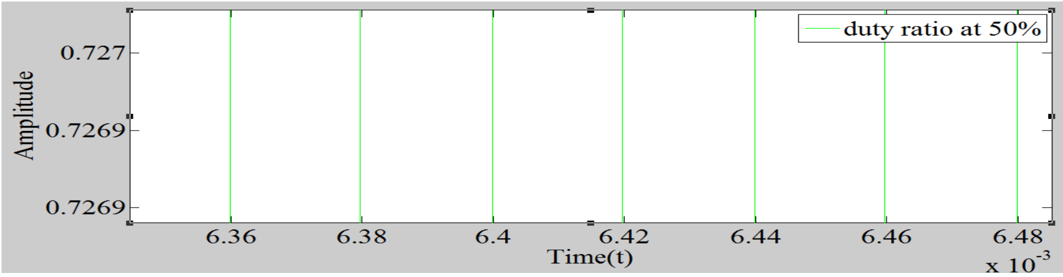

Fig 10: Pulses for Boost Converter.

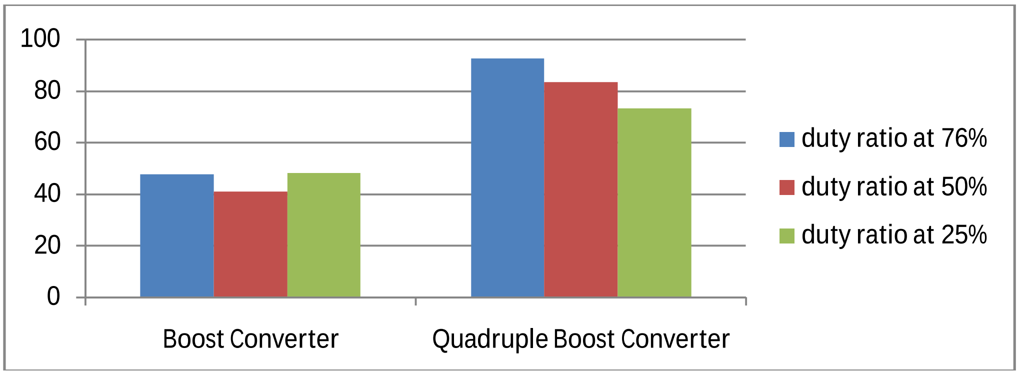

Fig: 11 Efficiency comparisons of Boost Converter and voltage quadrupler boost converter for different duty ratios

V. CONCLUSION

It can be seen that, 394V output is achieved in MAT lab simulation for 25V input. For this 0.76 duty cycle is taken. Very less voltage stress is on both diodes and active switches are gained. Main objective of this converter is to get much higher transfer gain is obtained for that low ratings of Mosfets can be used. Overall efficiency is better in designed model shown in figure 11. Conduction loss and switching losses are also made less by using lower ratings of MOSFET. No extra circuits needed to control since the use of blocking capacitor, automatic uniform current sharing of quadruple boost converter featured.

REFERENCES

[1] Ching-Tsai Pan, Chen-Feng Chuang, and Chia-Chi Chu, Member," A Novel Transformer-less Adaptable Voltage Quadrupler DC Converter with Low Switch Voltage Stress", IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 29, NO. 9, SEPTEMBER 2014.

[2] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA: Kluwer, 2001.

[3] L. S. Yang, T. J. Liang, and J. F. Chen, "Transformerless DC–DC converters with high step-up voltage gain," IEEE Trans. Ind. Electron., vol. 5 56,no. 8, pp. 3144–3152, Aug. 2009.

[4] Q. Zhao and F. C. Lee, "High-efficiency, high step-up DC–Converters, *IEEE Tran s. Power Electron.*, vol. 18, no. 1, pp. 65–73, Jan. 2003.

[5] Ramakant A. Gayakwad,"Op-amps and Linear Integrated Circuit", 4, publisher prentice Hall, 2000.

[6] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 871–887, Mar. 2008.

[7] H. Golnabi and A. Ashrafi," Phase-shift generation and monitoring by a simple circuit", Reach Gate.

[8] F. Zhang, L. Du, F. Z. Peng, and Z. Qian, "A new design method for high power high-efficiency switched-capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 832–840, Mar. 2008.

[9] E.H. Ismail, M. A. Al-Saffar, A. J. Sabzali, and A. A. Fardoun, "A family of single-switch PWM converters with high step-up conversion ratio," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 4, pp. 1159–1171, May 2008

[10] Rajendra Meena, "Simulation Study of Boost Converter with Various Control Techniques" International Journal of Science and Research (IJSR) ISSN (Online):2319-7064

[11] Sini P. Poulose and Archana P," A Quadrupler Voltage Interleaved DC-DC Boost Converter with Fuzzy Logic Implementation",The International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (IJAREEIE) Vol. 4, Issue 7, July 2 2015.

[12] D.Jeba Sundari Newlin , R.Ramalakshmi and S. Rajasekaran," A Performance Comparison of Interleaved Boost Converter and Conventional Boost Converter for Renewable Energy Application', Proceedings of 2013 International Conference on Green High Performance Computing, March 14-15, 2013.