ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 12, December 2017

Nanometre Regime Era : An Assessment of FinFET Based Low Power Digital Circuits

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ABSTRACT: The Nano-technology of integrated circuits brought a revolution by the development of devices which can be miniaturized sufficiently at Nano Scale. CMOS technology based circuit's offers scaling at nanometre regime leading to the arisement of short channel effects that have been greatly suppressed by FinFET technology. This work reviews the control of threshold voltage (Vth) and decrement of Drain-Induced Barrier lowering at different channel length via Multi Gate MOSFET. Here it also illustrates the XOR gate analysis in terms of power delay product at 16nm scale for various input supplies. Further, the investigation reviews the different types of flip flop architectures which explore in context of area, static power dissipation at the same channel length.

KEYWORDS: CMOS, Short Channel Effects, SOI, Quasi-Static, FinFET.

I.INTRODUCTION

In Nano-Scale Electronics it is desired to have an enormous quantity of components on a single silicon wafer. Hence technologies' promising excellent performance in least possible dimensions has been the topic of great research. Starting with MOSFETs the scaling went up to 20-25nm (channel length). Scaling MOSFETs beyond this, gate loses its control over the drain current and results in the leakage current. This leakage current won't allow the device to turn off even if there is no applied gate voltage. All these affects known as the "short channel effects" are attributed mainly to the "threshold shift" (decrement in the value of threshold) of the device. The problem is resolved to some extent by introducing an oxide layer ("buried oxide") [1] below the channel. This layer prevents the formation of "parasitic capacitances" [3] acting as insulator hence preventing threshold to decrease. This version of MOSFET is termed as SOI – Silicon on Insulator. SOI can be scaled down further than the normal MOSFETs. Both these architectures are planar. A more efficient architecture is proposed using vertical orientations of source, drain and gate. Moreover, the channel is also vertical in this architecture. This upright channel is referred as "fin" and the transistor is entitled the "FinFET" [2]. FinFET became the most popular substitute as it scored better than SOI and MOSFETs in controlling particularly the "short channel effects" which in turn controls the "threshold shift". Apart from this it out trended both SOI and MOSFET in power consumption, greater voltage gains, minor output conductance (i.e., slighter dIds/dVds in the current saturation region), enhanced on-state drive current (Ion) and consequently quicker circuit swiftness [25] and larger-channel width with comparatively less surface area. The basic difference between MOSFET and FinFET is of the channel. MOSFET employs channel formation through "inversion layer" while FINFET uses vertical channel- the fin. The inversion layer is formed in response to the applied gate voltage whether FinFET is a pre channelled device i.e., the channel is manufactured physically as a part of the device's basic structure. On operating MOSFETs over threshold and marginally increasing drain voltage, reduction in channel's thickness and length is observed. Slight increase in drain voltage reflects in the slight reduction of channel thickness. Going further with drain voltage the thickness of channel near the drain reaches its minimum known as 'pinch-off" point. At this point the drain voltage is the drain saturation voltage. Beyond this channel shrinks itself. So, it came out that drain current is a function of gate voltage, drain voltage and also of the threshold current [3] i.e.

$$\mathbf{IDS = f\ (VDS, VGS, VT)} \quad (1)$$

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ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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Website: www.ijareeie.com

Vol. 6, Issue 12, December 2017

When channel length becomes equal in magnitude with the source and drain depletion width, short channel effects come into action. Sub threshold current, velocity saturation and drain induced barrier lowering (DIBL) are main short channel effects. All these effects primarily result in the degradation of threshold value. FinFET offers a lot to attract circuit designers. Low delay power product, less power dissipation and faster switching are some of FinFET's merits over planar technology.

The paper is systematized as: Section I elucidates the introductory part of dissertation while section II deals the quasi-planar devices-modification in traditional bulk devices. Section III explains various operating modes of FinFET. Section IV consists of designing issues of digital circuits using FinFET. Section V concludes the paper.

II.PLANAR VERSUS NON – PLANAR DEVICES STRUCTURES

Traditional bulk device- The MOSFET is a three terminal device (body terminal is connected to the source terminal, hence effectively it's a three terminal device of one terminal each from source, drain and gate). Scaling beyond certain limit degrades its performance. Decreasing channel length gives rise to short channel effects. The most

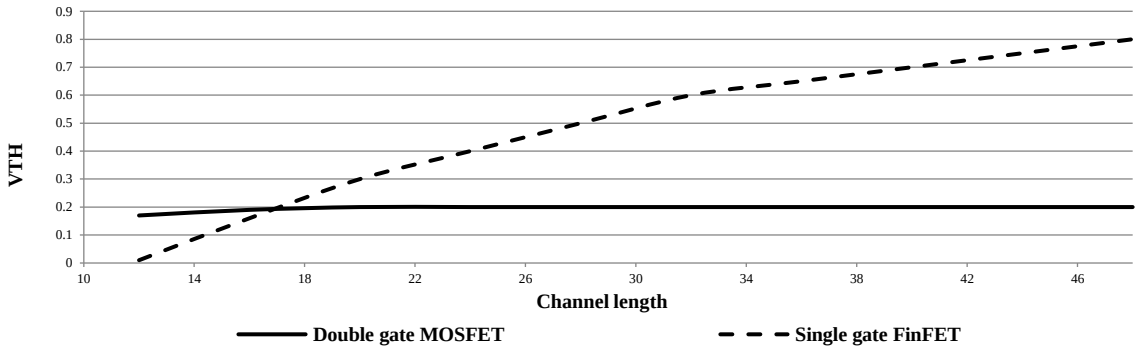

Figure1: Variation of the threshold voltage with the channel length (5)

important effect of short channel is the threshold roll off. Shifted threshold in turn allows sub threshold current to flow even in the absence of gate voltage hence posing barrier in turning off the device. Hence it can be easily established from the graph that threshold is proportional to channel length which is inversely related to drain current (leakage current) [3]. Dependence of threshold voltage (VTH) on channel length (L) for MOSFET, can be viewed in proportional relationship in equation (4).

$$VTH \propto L \quad (2)$$

And,

$$VTH \propto 1/ID \quad (3)$$

$$VTH \propto 1/ID \propto L \quad (4)$$

Graph representation of above mentioned equation (1) relationship is presented in Figure 1. These relations can be justified by looking into various short channel effects. DIBL is one such effect. It stands for Drain Induced Barrier Lowering. This is observed in short channel devices with high drain biasing. Due to drain biasing the drain-substrate depletion region expands itself. This expansion makes it easier for depletion region to interact with the channel i.e., electrons can easily find their way to channel. These transitions hence lower the potential barrier between channel and depletion region at drain end. This justifies the facts that drain current increases with decreasing threshold. Sub threshold current accompanied with DIBL elevates the problem of leakage current. Incursion of some electrons in the channel even after strong inversion results in leakage current below threshold point. Such diffusion of charges below threshold value gives rise to the sub threshold current. This can also be understood as the creation of new threshold i.e., the sub threshold below the actual threshold or simply the lowering of threshold point. Again justifying the fact that Vth decreases with increasing drain current. Also, drain current depends on the differences of the gate voltage and threshold voltage i.e., (VGS - VTH) [3]. In case of short channel devices when VTH falls it give rise to large drain current. Also if VGS is zero then the difference will be a small negative value (since VTH is small).

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ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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Vol. 6, Issue 12, December 2017

Hence even in cut off mode there will be a small leakage current which is further increased by the application of drain voltage. Sometimes some energetic electrons get trapped into the oxide during their transport over the barrier in to the oxide. Such electrons change the threshold and I-V relationship of the device. This hot electron effect can be treated by opting lightly doped source and drain regions.

II.(i) BULK MOSFET (THE PLANAR TECHNOLOGY)

As the dimensions of MOSFETs as shown in figure 2, are miniaturized, the close contiguity stuck between the source and the drain shrinks the aptitude of the gate probe to govern the potential distribution [8], plus movement of current in the channel region. These adverse effects are called "short-channel effects (SCE)" which starts afflicting the MOSFETs.

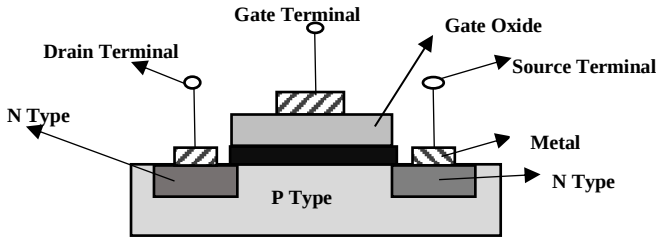

Figure 2: MOSFET Structure

II.(ii) SINGLE GATE SOI MOSFET (PLANAR TECHNOLOGY)

SCE can be reduced by using FDSOI MOSFET using single gate technology as presented in figure 3, however results in increased junction capacitance & increased body effect.

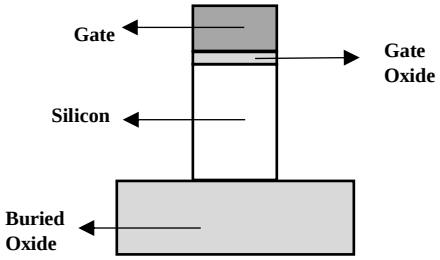

Figure 3: SOI MOSFET (7)

II.(iii) DOUBLE GATE SOI MOSFET/ FINFET (NON-PLANAR TECHNOLOGY)

The FinFET structure is identical to DELTA as illustrated in figure 4, except for the presence of a dielectric layer termed as "hard mask" on top of the silicon fin [8]. The hard mask is used to prevent the formation of parasitic in

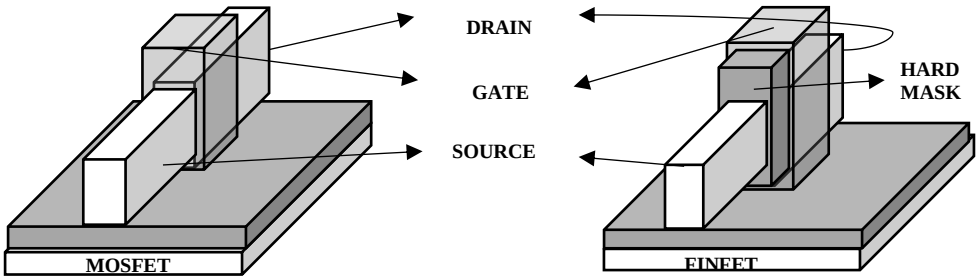

Figure 4: Different types of Double-gate MOS structure (8)

channels at the top corners of the device [8]. For all practical purposes, it seems unmanageable to shrink the extents of planar technology based "bulk" MOSFETs below 20nm scale. Thereby the practice of multi-gate devices permits individual to shrink the channel length even additional as depicted in figure 5, channel length (nm) versus DIBL

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ISSN (Online): 2278 – 8875

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Vol. 6, Issue 12, December 2017

(mv) in graphical form[12]. The decay of threshold voltage with declined channel length is a well-acknowledged as short channel effect entitled the "threshold voltage roll-off"' & can be easily control using double gate technology. To keep short channel effects in control following measures has to be taken as illustrated as: a) Minimizing Junction Depth (b) Minimizing Depletion Depth (c) Reducing Silicon Film (d) Reducing Buried Oxide Thickness. The FinFET employs "wrapped around channel" [4][11] by gates. It activates the current flow between drain to source with modulating the channel from both sides instead of one side. This technique provides an effective way of establishing a control over short channel effects and is the foundation of the improved performance of FinFET's over MOSFETs. Also according to the prediction of the ITRS (International Technology Roadmap for Semiconductors) double gate or multi gate devices will be perfect solution to obtain reduced leakage within short channels. [6]

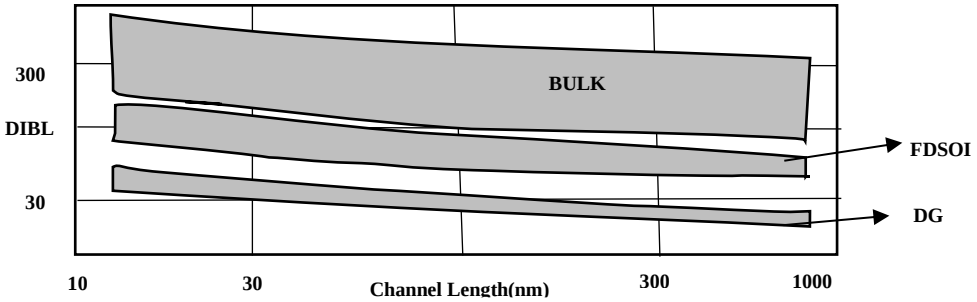

Figure 5: Emblematic drain-induced barrier lowering in bulk, fully depleted SOI (FDSOI) and double-gate (DG) MOSFETs(8)

III. OPERATING MODES OF FINFET

FinFET as depicted in figure 6 can be operated in four modes viz., short gate, independent mode, low power and hybrid mode depending upon the gate biasing.

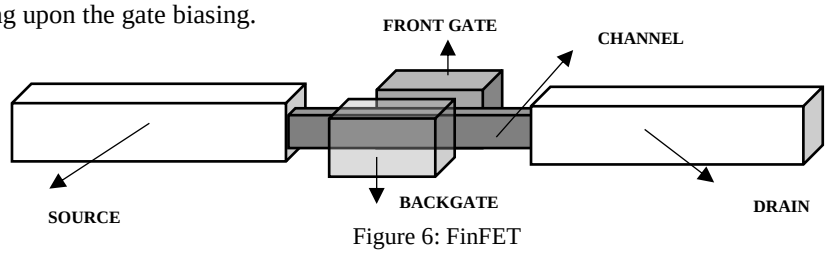

Figure 6: FinFET

In short gate mode both the back and front gate are tied with each other while in independent mode both gates operate on different gate voltages. Low power mode applies a reverse bias voltage to the back gate whilst hybrid mode employs the combination of low power and independent gate mode. Short gate mode as shown in figure 7, provides better control since both the gates are at same voltage. This allows the control via other gate in case one of the gate fails to control the operation i.e., becomes unstable. This technique results in better drive strength with low leakage. Improved efficiency is also observed in short gate mode. Visually short gate mode can be thought as the connected back and front gate over the fin, a sort of inverted U shape having fin in the space.

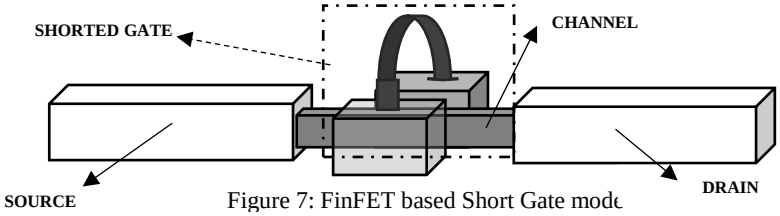

Figure 7: FinFET based Short Gate mode

Independent gate mode (figure 8) uses different voltage at both the gates which more transistors as compared to other modes. Increase delay is the short coming but has enhanced flexibility. Independent gate can be imagined as

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the separated front and back gate via fin. When the back gate is reverse biased the mode is called the Low power mode (figure 9) resulting in leakage with the short coming of reduced drive strength.

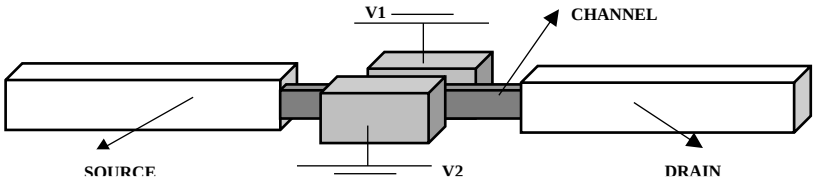

Figure 8: FinFET based Independent Gate Mode

Integration of multi gate based low power mode and independent gate mode results in amalgam mode i.e., back gate is operated with reverse bias voltage. The amalgam mode outcomes in improved switching speed.

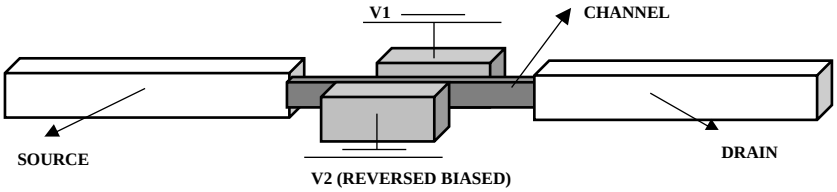

Figure 9: FinFET based Low Power Mode

IV. DIGITAL CIRCUIT'S DESIGNING ISSUES BASED ON FINFET AT NANO-SCALE

When it comes of digital circuits it is observed that it has many advantages over the analog circuits. The digital logic circuitry mainly consists of simply logic gates or their combinations. These circuits offer easy manufacturing, reliability, less device area i.e., more components on a single chip. Easy with information storage and the fact is achieved by special switching circuits that can latch onto information and hold it for as long as necessary. These circuits occupy an upper hand by allowing control through set of instructions i.e., they are programmable. All these benefits along with some other benefits cement the foundation of digital circuits over the traditional analog system. XOR is one of the digital circuits which represents the inequality function i.e., the output is true if the inputs are not alike otherwise the output being false. Here XOR is designed in low power mode and is then compared between the planar and non-planar architecture on the basis of power delay product (PDP) at different voltages in table I.

V_{DD} (mV)	Power Delay Product (PDP)	
	MOSFET based LP-XOR (aJ)	FinFET based LP-XOR (aJ)
630	2.2467	0.0164
665	2.3419	0.0202
700	2.5148	0.0254
735	2.8357	0.0322
770	3.2742	0.0409

Table I. Power Delay Product comparison between FINFET based LP-XOR AND MOSFET based LP-XOR at 16nm. (9)

Graphical representation is shown as in figure 10 where unit of power delay product is Armstrong Joule (aJ) and the values obtained are the result of immense simulations performed on H-Spice using 16nm PTM with power supply of 0.7V[9].One of the fundamental building blocks of digital electronics systems is flip-flop which is a sequential circuit and used as a storage element.In our context we have analysed different flip flop architectures based on structural design at 16nm considering area and static power as comparison parameters as shown in table II. master slave double latch structured [10] implemented by different methods for MOSFET and FinFET Results of ths comparison are also obtained by numerous H-Spice simulations using 16nm PTM with power supply of 0.85V graphical representation for each parameter is as shown in Figure 11, 12 and 13 respectively .Also, graph for static

ISSN (Print) : 2320 – 3765
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power as depicted in Figure 12 and Figure 13 is represented separately for each state i.e., for 0-to-1 and for 1-to-0. It is clear from these graphs that FinFET is better than MOSFET.

Q Edge		MOSFET 16 nm		FINFET 16 nm	
		Area(μm²)	Static Power(nW)	Area(μm²)	Static Power(nW)
FF1	0-to-1	0.541	6560	0.519	03.84
	1-to-0		76.53		04.70
FF2	0-to-1	0.698	66.40	0.679	07.27
	1-to-0		78.63		05.90
FF3	0-to-1	1.239	46.43	1.185	02.58
	1-to-0		73.57		03.44
FF4	0-to-1	1.487	71.42	1.413	08.06
	1-to-0		95.70		04.91
FF5	0-to-1	2.501	119.7	2.372	10.52
	1-to-0		111.2		06.56
FF6	0-to-1	0.631	13.82	0.589	01.42
	1-to-0		15.00		01.56
FF7	0-to-1	0.991	76.86	0.931	04.67
	1-to-0		75.45		09.31

Table II. Comparison of MOSFET and FINFET at 16 nm. (10)

Where: FF1: Transmission Gate based static flip-flop; FF2: Transmission Gate based pseudo-static flip flop; FF3: Bootstrap Transmission Gate based pseudo static flip-flop; FF4: C2MOS based pseudo-static flip-flop; FF5: Bootstrap C2MOS based pseudo-static flip-flop; FF6:C2MOS based dynamic flip-flop; FF7: TSPC N2MOS–P2MOS based dynamic flip-flop.

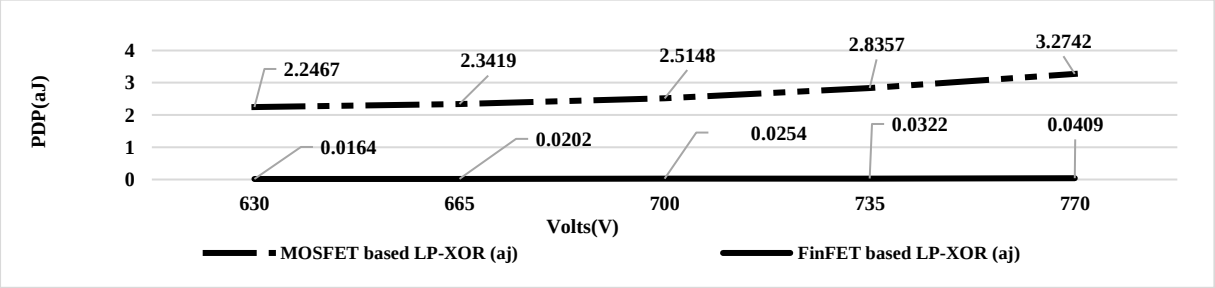

Figure 10: PDP (aJ) Variation of MOSFET and FINFET in XOR Circuit.

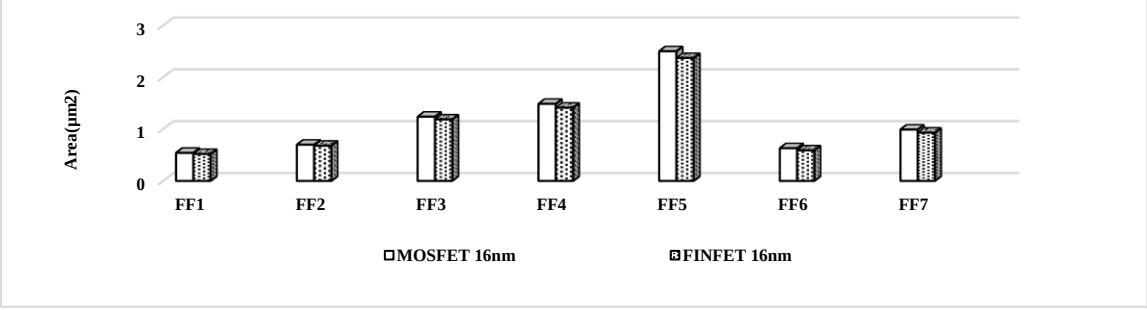

Figure 11: Area (μm2) comparison of MOSFET and FINFET at 16nm

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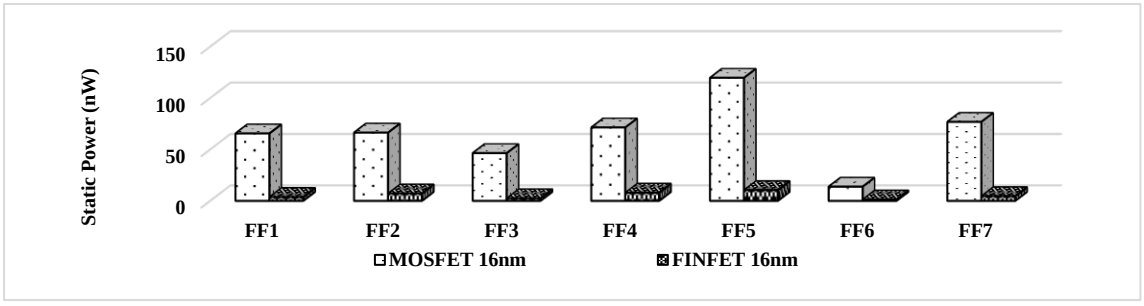

Figure 12: Comparison of Static Power (nW) (Q Edge: 0-to-1) of MOSFET and FINFET at 16nm

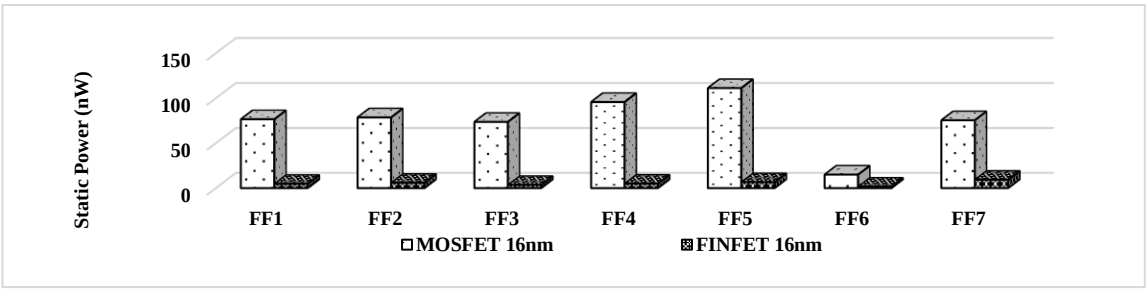

Figure 13: Comparison of Static Power (nW) (Q Edge: 1-to-0) of MOSFET and FINFET at 16nm

V. CONCLUSION

The basic understanding of FinFET is reviewed through this paper and comparison of this non-planar technology is made with the MOS technology. It can be concluded that the non-planar architecture of FinFET has several advantages over the traditional planar devices. Comparison between both the technologies is made on the ground of PDP, area and static power at the channel length of 16nm. PDP of XOR circuit for both bulk and FinFET is observed. PDP reading for FinFET comes out to be lesser than the MOSFET. Congruently master slave flip flops of different architectures design is compared considering the parameters area and static power. Silicon area occupied by the FinFET is more compact than the MOSFET while the readings of static power also fall in favour of FinFET.

VI. ACKNOWLEDGEMENT

First and foremost, I owe my entire acknowledgement to the almighty ALLAH (S.A.W.) the most beneficent and merciful. It is his will which has enabled me to accomplish my work which otherwise would not have been possible. I am also thankful to Department of Electrical Engineering; Jamia Millia University for their providing ample of resources. This review is supported by the faculty of Electronics & Communication Engineering, Mewat Engineering College, Mewat. The college also facilitated ample resources for literature study regarding the review paper. We pay our sincere thanks to the faculty of Electronics & Communication Engineering, Mewat Engineering College, Mewat and Mewat Engineering College, Mewat for supporting and encouraging us to write this review paper on the FinFET technology.

ISSN (Print) : 2320 – 3765
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