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Digital Synthetic Ripple Modulator for DC-DC Converter

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ABSTRACT: Synthetic ripple modulation (SRM) involves the generation of an artificial ripple me of carrier signal generation for PWM control enables voltage-hysteretic modulation to be achieved in the low-voltage VRM modules for microprocessors. With the inherent low-voltage ripple exhibited by a low-voltage VRM that is insufficient for conventional hysteretic operation, the SRM scheme on the other hand provides sufficient ripple for the PWM carrier signal. The SRM scheme blends in the advantages of current-mode control and hysteretic control providing superior transient performance.

KEYWORDS: Synthetic ripple modulation, Digital synthetic ripple modulation **,**pulse width modulation , metal oxide semiconductor field effect transistor, Analog to digital converter.

I.INTRODUCTION

Generation of carrier signals undergoes in pulse widthmodulation (PWM) control of converters or inverters with hysteretic mode of operation. The carrier signals are derived from converter/inverter parameters such as inductor voltage, drain-source voltage of power MOSFET, inductor current, and stator winding current. The carrier signal is generate according to the ripple associated with the variable to be maintain or control and a synthetic ripple derived by filtering a converter parameter value. Since the PWM control involves artificial carrier signal generation, the term synthetic ripple modulation promptly applies. The superimposing of the controlled variable with that of the synthetic ripple creates a significant amount of ripple similar to that exhibited in conventional current mode control. The modulation strategy is theoretically validated with an application involving the control of a DC-DC synchronous buck converter used as a switching regulator for powering microprocessors. The tight tolerance required on the output voltage of the switching regulator and the higher di/dt (120A/ns) requirement can be achieved with thesynthetic ripple modulation (SRM) technique. Since the SRM based control is a form of hysteretic control modulating the controlled variable directly within a hysteretic band, superior dynamic performance is inherently attained. The output voltage is bonded to a synthetic ripple, resulting in a carrier signal with proper amount ripple for PWM operation, allows the output voltage to be controlled directly and with the required tight tolerance.

The digital SRM (DSRM) scheme apply to control of the buck converter output & also involves a new method for deriving the duty ratio, with the time-intervals which produced are inversely related to a sampled converter parameter. The duty ratio generation scheme is based on a unique scaling process and eliminates the need for a high clock frequency. The modulation technique use the sampled inductor voltage, which is scaled and successively accumulated to produce the synthetic ripple. The error in the output voltage when compared to a reference or command voltage is added to the synthetic ripple resulting in the carrier signal for PWM operation. The carrier signal is modulated between hysteretic limits, resulting to match required duty ratio. Since the carrier signal involved in the PWM signal generation is derived from the converter parameters in the SRM scheme, natural input feed-forward control is also attained. This enablesbetter rejection of line input disturbances.

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II. DIGITAL SYNTHETIC RIPPLE MODULATOR

Digital Synthetic Ripple modulator (DSRM) functions as a digital to analog converter inproducing the PWM pulse signal based on sampled converter waveforms. The DSRM utilizes sampled version of converter parameters like inductor voltage, inductor current, or drain-source voltage of MOSFETS to synthesize an artificial ripple used as carrier signal in pulse width modulation. The modulation strategy is based on bonding the controlled variable to the syntheticripple generated by the DSRM. The resulting carrier signal is bound between hysteretic limits which dictate the commutation instants of the power MOSFET switches. The modulation strategy can be applied to the control of DC-DC and DC-AC power converters.

III.DESIGN CONCEPT OF DSRM

In DC-DC converters or DC-AC inverters employing current-mode control , the on-time and off-time of the power MOSFET switches are inversely proportional to the inductor voltage under steady-state conditions as given in Eq.3.1

$$\text{ton or toff} = \frac{\text{L} \times \Delta\text{L}}{VL} \text{------3.1}$$

where L is the value of the inductor and ΔIL indicates the peak-peak inductor current ripple.In the generic case, the time duration to be generated can be inversely proportional to acontrol input ($q(V, I)$) as given in Eq. 3.2.$t = \frac{\text{K}}{q(v,i)}$------3.2

Similar duty ratio or time duration requirements are exhibited in hysteretic PWM control having variable switching frequency. The conventional analog approach based duty ratio/ timing generators involve current sources and on-chip/off-chip capacitors. These approaches generally exhibit poor noise sensitivity and offer limited programmability. Timing generators and duty ratio generators based on digital schemes involve digital pulse width modulators (DPWMs) that are characterized by a linear relation between the time duration generated and the control input. The DPWMs are based on delay-lines , propagation-delay of basic gates or the time period of a fast running clock .

Synthetic Ripple Modulation is on the basis to control of power converters which involve carrier signalgeneration from converter based parameters value. This modulation strategy, when applied to the control of a DC-DC buck converter, utilizes the inductor voltage for its carrier signal generation .Hence, this modulation also involves generation of on-time and off-time duration for power MOSFET switches with inverse relation to a control voltage. In the analog domain, the inverserelation between the on/off-time of the power MOSFET switches and the inductor voltage as in Eq. 3.1 can be realized by employing a Gm-C circuit . An all-digital realization to generate timing inversely related to a voltage would involve area-intensive digital division hardware or a cost-intensive DSP processor based solution. The need for the inverse relation based duty ratio generation as in Eq. 3.2 led to the development of the digital inverse timing generator.

IV.ARCHITECTURE OF DIGITAL SYNTHETIC RIPPLE MODULATOR

In conventional PWM control, the output variable is regulated by comparing a modulating function with that of a carrier signal. The comparison process effectively modulates the time duration of a pulse controlling the on/off position of a switch which in turn determines the duty ratio. In synthetic ripple modulation, the carrier signal utilized in the comparison process is derived from a system parameter unlike the traditional approach of using external oscillators.

The modulation strategy is based on bonding the error between the controlled variable and a command variable to a synthetic ripple derived by filtering any ac waveform of the system. The combination of the error and the synthetic ripple forms the carrier signal (modulator output) which is bounded between hysteretic limits. The hysteretic limits dictate the on/off time duration of the switches in the system. Synthetic ripple modulation also deals with open-loop linear control of an output variable according to a command input. Since the modulation scheme derives the carrier signal from the system parameter, it enables natural feed-forward control. This modulation scheme when applied to the control of DC-DC converter or DC-AC inverters, the output voltage of a voltage regulator or the rotor speed in a motor drive can be controlled. In such applications the on/off-time or the duty ratio of the power MOSFET switches can be inversely related to a control voltage input as given in Eq. 3.1 or Eq. 3.2. Thus, the above mentioned digital timing

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generator can be used to produce the duty ratio. The generic architecture of a digital synthetic ripple modulator controlling a desired output variable in a system is illustrated in Figure 1.

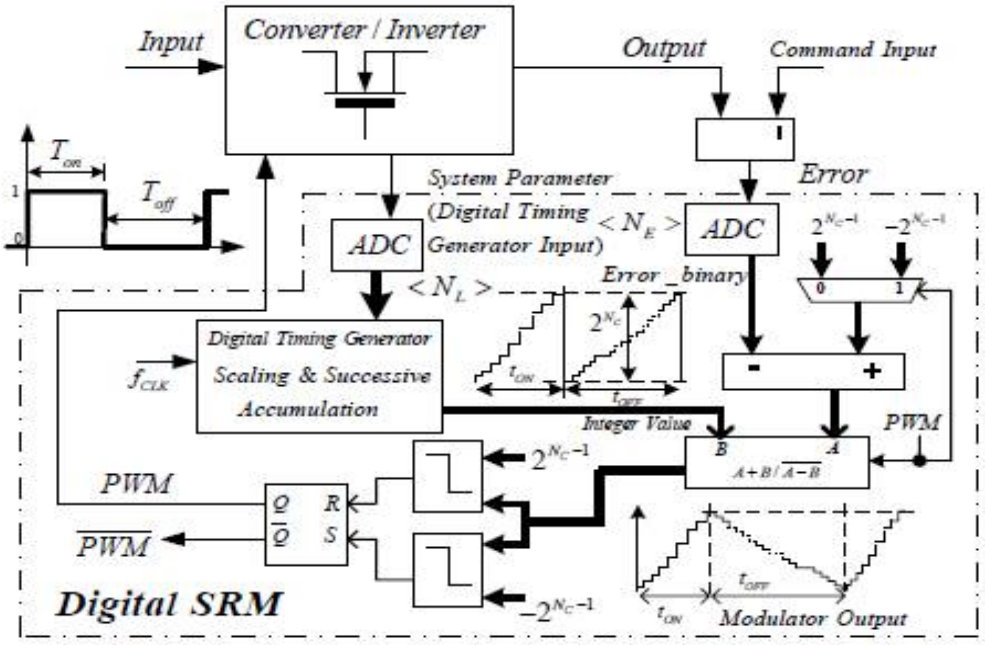

Fig. 1 Generic architecture of a system controlled by digital synthetic ripple modulator

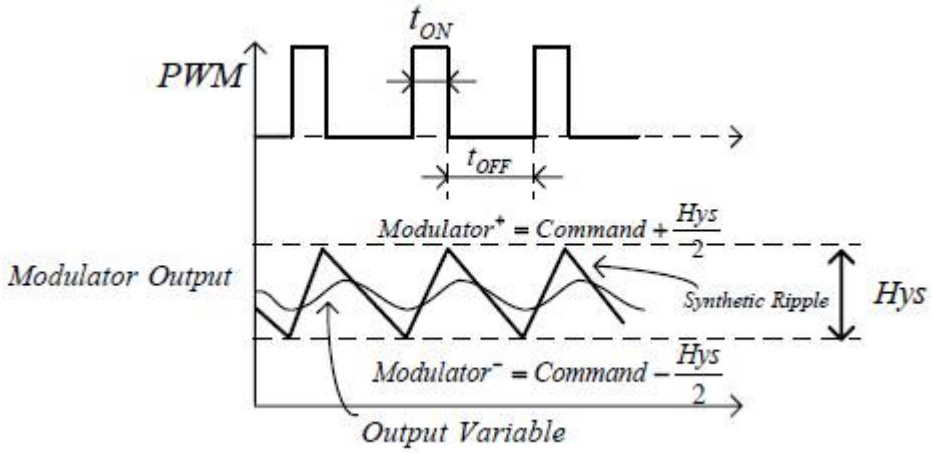

Fig. 2 Generic synthetic ripple modulation showing the hysteretic thresholds, command variable and PWM signal

As indicated in Figure 1, the system parameter related to the duty ratio is sampled andgiven as input to the digital timing generator. The digital timing generator scales the sampled input and generates the step value. The step value is successively accumulated between the hysteretic limits and the required duty ratio is generated. The PWM output is set

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to logic high or "1" when the modulator output exceeds the upper hysteretic threshold (2^{N_c-1}). The PWM outputis set to logic low or "0" when the modulator output is lesser than the lower hysteretic threshold (-2^{N_c-1}) .

PWM = { 1 Modulator output $\leq(-2^{N_c-1})$}
PWM={0 Modulator output $\leq (+2^{N_c-1})$ }----4.1

The PWM signal is retained in logic 1 or logic 0 when the modulator output is outside thehysteresis band. The PWM signal is set to the appropriate logic level once the modulator output is within the hysteresis band based on Eq.4.1 and normal SRM operation is resumed. The generic expression modeling the synthetic ripple modulator in the analog domain is given in Eq. 3-26.
ModulatorOutput _ Analog = Output Variable + Synthetic Ripple -----4.2
The modulator output generating the carrier signal is modulated between the hysteretic limitsgiven as follows
$Modulator^{+}$= Command variable+(Hys/2)
$Modulator^{-}$= Command variable – (Hys/2)-----4.3
whereModulator+ and Modulator− are the higher and lower hysteretic thresholds in the analog domain and Hysindicates the hysteresis band.
The schematic representation of Equations 4.2 and 4.3 is shown in Figure 2 . The subtraction of the command variable from the modulator output expression of Eq. 4.2 modifies the hysteretic thresholds to (+Hys/2) and (-Hys/2). The modulator output expression is changed accordingly as
ModulatorOutput_ Analog – Command = (Output-Command)+Synthetic Ripple -----4.4

In the digital SRM implementation, the error resulting from the difference between thecommand variable and the output variable is sampled by an A/D converter. The sampled error value indicated in Figure1 and the synthetic ripple information from integer value of the accumulator are used in the formulation of digital SRM modulator expression. The digital SRM modulator output is given as
Modulator Output = (Error _ binary) + Integer Value-----4.5

In the digital SRM, the sampling of the error value between the command and outputvariable instead of the actual output variable provides the benefit of allocating higher number of bits for the error. It also offers the benefit of controlling the output variable with better precision. The dynamics of the SRM is also enhanced by the fact that when the sampled value of the error between output and command variable exceeds its higher or lower quantization levels [saturation limits of the A/D (e.g. 0 or 255 with 8 bits of precision)], the PWM signal can be immediately set to logic "1" or logic "0" depending on the saturation limits. The subtraction of the command variable from Eq. 4.2 as explained earlier modifies the digital SRM hysteretic thresholds as (2^{N_c-1})and(-2^{N_c-1}) with the "*Hys*" level in analog SRM mapped to 2^{N_c}in the digital SRM. The integer value from the accumulator spans from 0 to 2^{N_C} during both the on-time and off time durations. Thus, to account for the modified hysteretic thresholds, the terms (2^{N_c-1})and (-2^{N_c-1}) are added to the digital SRM modulator expression during the off-time and on-timeduration respectively. The integer value varying from 0 to 2^{N_c}, themodulator output is always modulated with a hysteretic level of 2^{N_c}. The resulting digital SRM modulator expression is given in Eq. 4.6.

Modulator output = (2^{N_c-1}– Error _ binary [n]) – Integer value ; PWM=0
Modulator output = (-2^{N_c-1}– Error _ binary [n]) + Integer value ; PWM= 1-----4.6

In the equation of the digital SRM modulator, Error_binary[n] indicates the sampled error voltage of the output A/D and Integer Value[n] is the integer output extracted fromthe accumulator at t_{CLK}instant "n". Considering the modulator expression Eq. 4.6, Error_binary is negative when the output voltage is above Vcmd. Thus when PWM =1, the higher hysteretic threshold will be attained earlier and Integer Value will span to less than 2NC resulting in reduced on-time.

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Similarly when V_{out} is less than V_{cmd}, Error_binary is positive causing Integer Value to span to $2^{N}{}_{c}$, resulting in increased on- time. Similar argument can be applied for the factor of ($2^{N}{}_{c}{}^{-1}$− Error _ binary) during PWM=0. A low-pass filtering effect similar to integration is obtained in the digital timing generator's accumulator during floating pointaddition by discarding the least significant bits. Thus the Integer Value[n] qualitatively represents the low-pass filtered output of the sampled converter parameter.

V. RESULT AND DISCUSSION

The digital timing generator utilizes the sampled inductor voltage to generate the on-time/off-time& adjusting duty ratio. The block take the sampled inductor voltage, timing generator enable signal and the initial binary point location. The accumulated value, integer value, the current step value, and the carry output are fed back as inputs to the timing generator block.

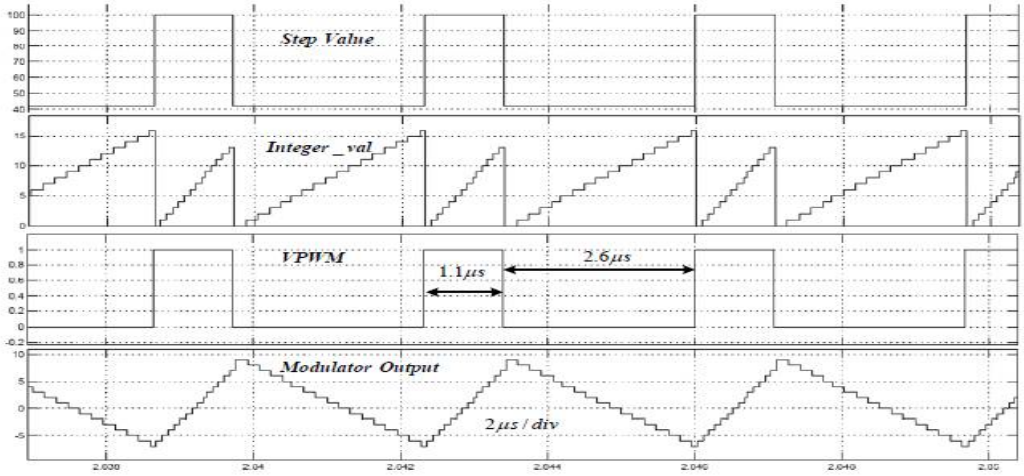

Fig. 3. Simulation outputs of the synchronous buck converter using MATLAB for Vcmd=1.3V

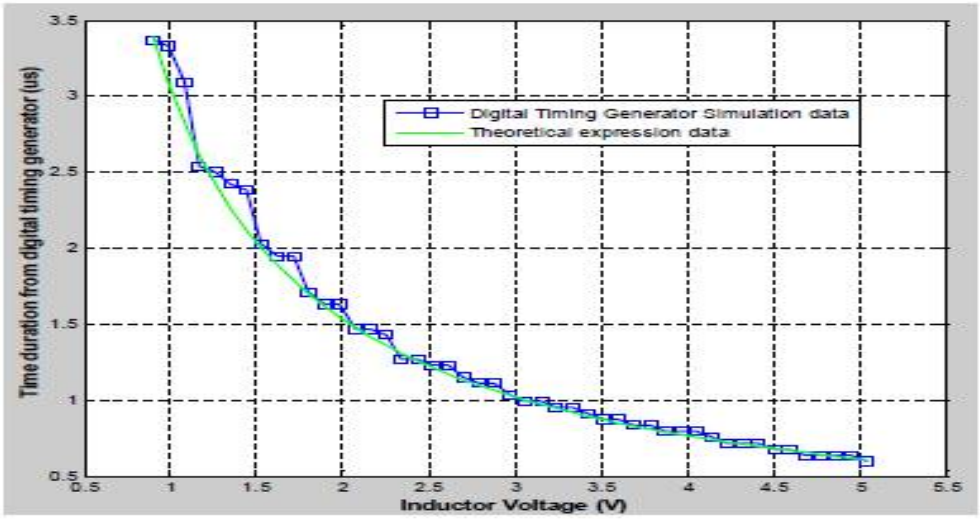

Fig. 4. Comparison between on-time/off-time generated based on theoretical equations and simulated SRM.

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VI.CONCLUSION

Synthetic ripple modulation technique enables carrier signal generation from systemparameters. The SRM facilitates the controlled variable to be regulated with a tight tolerance while providing sufficient ripple for PWM control. The modulation strategy superimposes the controlled variable with the synthetic ripple and thereby allows direct control of the output variable. The SRM technique also give the significant advantage of linear control of the output variable with a command signal even under open-loop conditions. Since the synthetic ripple modulation derives its principle from hysteretic mode of control, superior dynamic performance is guaranteed. Thus the potential benefits of current mode control and hysteretic mode control are achieved without the need for current sensing or a fast resolution PWM comparator.

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