ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An UGC Approved Journal)

Website: www.ijareeie.com

Vol. 6, Issue 8, August 2017

Power Factor Corrector Boost Converter with Self Tuned PID Controller by Genetic Algorithm

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ABSTRACT: The boost Converter (step-up converter), may be a topology of power to manage voltage DC/DC that may be enforced like intermediate part of a additional advanced system, which is wide used for the Three phase active correction of power issue (PFC).The input to the present device is usually Associate in Nursing unregulated rectifier line voltage, which is able to fluctuate attributable to changes of the load voltage magnitude. The most objective of management of this circuit is to convert the unregulated DC input voltage into a controlled DC output voltage ahead of changes within the load. In addition, in several applications it's desired to take care of a power factor correction (PFC). In this article, an inflammatory disease current mode management work by genetic algorithms (GA) is projected and its characteristics and application to the regulation of the ability converters and PFC square measure investigated. The advantage of the projected hybrid management is that not solely it retains the benefits of the prevailing current mode management; however it additionally affords a further standardization parameter which might be wont to modify the output response. Finally, it's bestowed some MATLAB/SIMULINK results as an instance the options of the projected management.

KEYWORDS: AC–DC power factor correction, phase-shifted modulation, single-stage converters, three-level converters, Genetic Algorithm.

I. INTRODUCTION

The boost converter (step-up converter), is a topology of power to regulate voltage DC/DC that can be implemented like intermediate component of a more complex system, and that is widely used for the active correction of power factor (PFC) (Martínez, 2004). The input to this converter is often an unregulated rectifier line voltage, which will fluctuate due to changes of the line voltage magnitude. The main objective of control of this circuit is to convert the unregulated DC input voltage into a controlled DC output voltage in front of changes in the load. Additionally, in many applications it is desired to maintain a sinusoidal input current (PFC). The problem of regulating the output voltage of these converters has been a subject of great interest for many years, due to the switching property included in their structure, DC/DC converters have a non-linear behavior and consequently their controlling design is accompanied with complexities. In addition, due to the no minimum phase nature of the boost converter, much effort has been directed at the control of this configuration.

Mathematical modelling of power DC/DC converters is a historical problem accompanying with the development of the DC/DC conversion technology since 1940's (Lin and Ye, 2004). The preliminary work on the mathematical modeling for DC/DC converters followed the traditional calculation manner using impedance analysis to obtain transfer function in the s-domain (Laplace transform) (Chan, 2007).

In this article, a PID current mode control fit by genetic algorithms (GA) is proposed and its characteristics and application to the regulation of the power converters and PFC are investigated. The advantage of the proposed

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hybrid control is that not only it retains the advantages of the existing current mode control, but it also affords an additional tuning parameter which can be used to modify the output response. Finally, it is presented some MATLAB/SIMULINk results to illustrate the features of the proposed control.

II. CONVERTER TOPOLOGY

The converter and its key waveforms are shown in Figs. 2 and 3, respectively. The proposed converter uses auxiliary windings that are taken from the converter transformer to act as "magnetic switches" to cancel the dc bus capacitor voltage so that the voltage that appears across the diode bridge output is zero. Auxiliary Winding 1 (Naux1/N1 = 2) cancels out the dc bus voltage when the primary voltage of the main transformer is positive, so that the output voltage of Diode Bridge 1 (DB1) is zero, and the currents in input inductors La1, Lb1, and Lc1 rise. Auxiliary Winding 2 (Naux2/N1 = 2) cancels out the dc bus voltage when the primary voltage of the main transformer is negative, so that the output voltage of Diode Bridge 2 (DB2) is zero, and the currents in input inductors La2, Lb2, and Lc2 rise.

When there is no voltage across the main transformer primary winding, the total voltage across the dc bus capacitors appears at the output of the diode bridges, and the input currents falls since this voltage is greater than the input voltage. If the input currents are discontinuous, the envelope of the input current will be sinusoidal and in phase with the input voltages. The converter has the following modes of operation during a half switching cycle; equivalent circuit diagrams that show the converter's modes of operation are shown in Fig. 4:

Mode 1 ($t0 \leq t \leq t1$): During this interval, switches S1 and S2 are ON. It should be noted that both dc bus capacitors and the flying capacitor are charged to half of the dc bus voltage. In this mode, energy from dc bus capacitor C1 flows to the output load. Due to magnetic coupling, a voltage appears across Auxiliary Winding 1 that is equal to the dc bus voltage, but with opposite polarity. This voltage cancels the total dc bus capacitor voltage so that the voltage at the diode bridge output is zero, and the input currents in La1, Lb1, and Lc1 rise.

Mode 2 ($t1 \leq t \leq t2$): In this mode, S1 is OFF, and S2 remains ON. Capacitor Cs1 charges and capacitor Cs4 discharges through Cf until the voltage across Cs4 , the output capacitance of S4 , is clamped to zero. The energy stored in the input inductor during the previous mode starts being transferred into the dc bus capacitors. This mode ends when S4 turns ON with ZVS.

Mode 3 ($t2 \leq t \leq t3$): In Mode 3, S1 is OFF, and S2 remains ON. The energy stored in input inductor L1 during Mode 1 is transferring into the dc bus capacitors. The voltage that appears across Auxiliary Winding 1 is zero. The primary current of the main transformer circulates through D1 and S2 . With respect to the converter's output section, the load inductor current freewheels in the secondary of the transformer, which defines a voltage across the load filter inductor that is equal to $-VL$.

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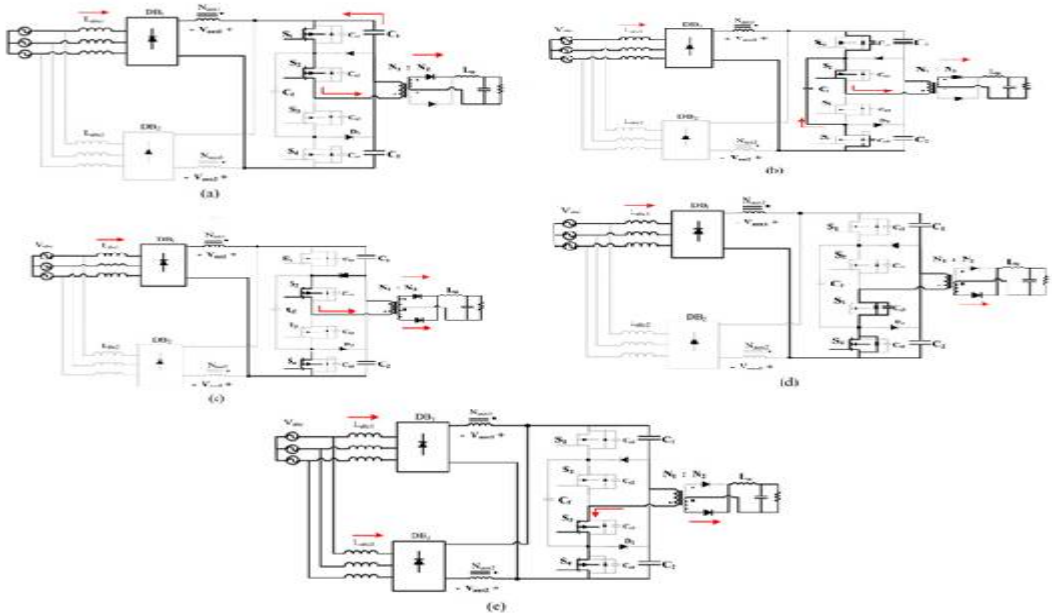

Fig. 4. Modes of operation. (a) Mode 1 (t0 < t < t1). (b) Mode 2 (t1 < t < t2). (c) Mode 3 (t2 < t < t3). (d) Mode 4 (t3 < t < t4). (e) Mode 5 (t4 < t < t5).

Mode 4 (t3 ≤ t ≤ t4): In this mode, S1 and S2 are OFF. The energy stored in L1 continues to be transferred into the dc bus capacitor. The primary current of the transformer discharges the output capacitor of Cs3 . If there is enough energy in the leakage inductance, the primary current will completely discharge the body capacitor of Cs3 , and current will flow through the body diode of S3.This current also chargesC2 through the body diodes of S3 and S4 . Switch S3 is switched ON at the end of this mode.

Mode 5 (t4 ≤ t ≤ t5): In this mode, S3 and S4 are ON, and energy flows from capacitor C2 to the load. A voltage appears across Auxiliary Winding 2 that is equal to the dc bus voltage, but with opposite polarity to cancel out the dc bus voltage. The voltage across the boost inductors L2 (L2 = Labc2) becomes only the rectified supply voltage of each phase, and the current flowing through each inductor increases. This mode ends when the energy stored in L1 is completely transferred into the dc bus capacitor. For the remainder of the switching cycle, the converter goes through Modes 6–10, which are identical to Modes 1–5 except that S3 and S4 are ON instead of S1 and S2 and DB2 conducts current instead of DB1 .

The input current is the sum of currents iL1 and iL2, corresponding to each set of input inductors, with each inductor having a discontinuous current. However, by selecting appropriate values for La1 = Lb1 = Lc1 and La2 = Lb2 = Lc2, two inductor currents such as iLa1 and iLa2 can be made to overlap each other so that the input current can be made continuous, thus reducing the size of input filter significantly.

There is a natural 180° phase difference between the currents in L1 and the currents in L2 as one set of currents rises when the transformer primary is impressed with a positive voltage, and the other set rises when the transformer primary is impressed with a negative voltage.

It should be noted that standard phase-shift PWM can be implemented in the converter, and thus, a standard phase-shift PWM IC can be used to generate the gating signal. This can be seen from Fig. 3 and the modal circuit diagrams. Switches S2 and S3 are not allowed to be ON at the same time, and switches S1 and S4 are not allowed to be ON simultaneously as well.

The converter is in an energy-transfer mode whenever switches S1 and S2 are ON or S3 and S4 are ON. It is in a freewheeling mode of operation whenever switches S1 and S3 or S2 and S4 are ON.

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The sequence of alternating energy transfer and freewheeling modes that occur during a switching cycle corresponds to the

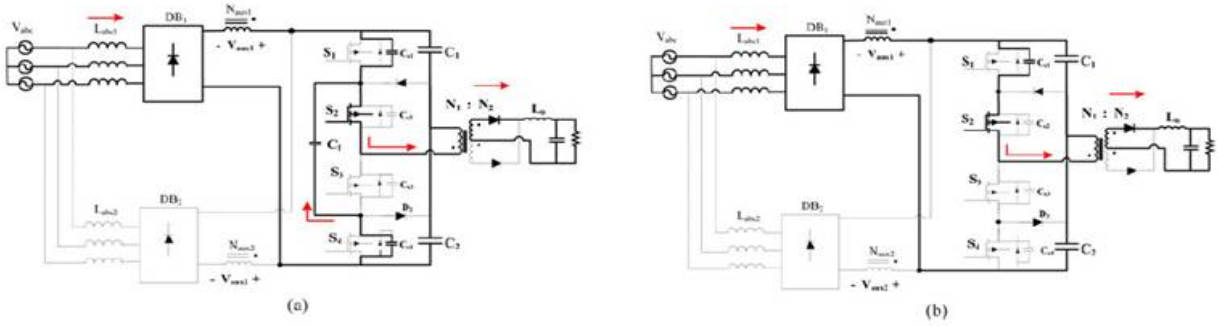

Fig. 5. Flying capacitor versus diode-clamped three-phase single-stage converter. (a) Mode 2 in the proposed flying capacitor converter (t1 < t < t2) (b) Mode 2 in diode-clamped converter (t0 < t < t1).
same sequence of modes that exists in a standard two-level phase-shift PWM full-bridge converter.

III. FLYING CAPACITOR VERSUS DIODE-CLAMPED MULTILEVEL THREE-PHASE SINGLE-STAGE CONVERTER

The proposed interleaved topology with flying capacitor can guarantee a ZVS turn-on for its very top and very bottom switches in a way that the converter presented in [17] cannot. To understand why this is so, first consider a standard two-level ZVS-PWM dc–dc full-bridge converter operating with phase shift PWM. For this converter, the leading leg switches (switches that are turned ON when the converter enters a freewheeling mode of operation) of this converter can be turned ON with ZVS. This is due to the fact that the transformer primary current is dominated by reflected output inductor current during this transition so that there is sufficient energy available to turn ON the leading leg switches with ZVS. It is the lagging leg switches (switches that are turned ON when the converter is exiting a freewheeling mode) that lose their ability to turn ON with ZVS under light-load conditions as it is only the transformer primary leakage inductance energy that is available to discharge and charge the appropriate switch output capacitances.

Now consider the converter proposed in [17], as shown in Fig. 5(b). It can be seen in Fig. 5(a) that the converter enters a freewheeling mode of operation when switch S1 is turned OFF. The converter exits this freewheeling mode by the turning OFF of S1 and then the simultaneous turning ON of switches S3 and S4. During this transition, it is only the leakage inductance energy that is available to turn S3 and S4 ON with ZVS. Similarly, switch S1 and S2 are turned ON when the converter exits the other freewheeling mode of the switching cycle, again, with only the leakage inductance energy available to discharge their output capacitances. What this means is that all the converter switches lose the ability to turn ON with ZVS under light-load conditions as only leakage inductance energy is available to discharge their output capacitances just before they are turned ON. With respect to the proposed converter, as can be seen from Mode 2 (just like Mode 7), shown in Fig. 5(a), when S1 (or S4) turns OFF and the converter enters a freewheeling mode of operation, the energy available to charge the output capacitance of S1 (or S4 in Mode 7) and discharge the output capacitance of S4 (or S1 in Mode 7) is the energy stored in leakage inductance plus the energy in output filter inductor that is “reflected” to the primary. Since the energy in the filter inductor is large compared to that required to charge/discharge the capacitances, the body capacitance of S4 (or S1 in Mode 7) can be discharged completely through flying capacitor Cf . Once this happens, switch S4 (or S1 afterMode 7) can be turned ON with ZVS in anticipation for later on in the switching cycle when the converter exits a freewheeling mode of operation.

The ZVS turn-on for switches S1 and S4 , when the converter is exiting a freewheeling mode of operation cannot happen for the converter presented in [17], as can be seen in Fig. 5(b). This is because there is no flying capacitor in the converter that provides a path for current to flow through when the converter enters a freewheeling

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mode of operation. These switches can only turn ON with ZVS if there is sufficient transformer leakage inductance energy to discharge the output capacitance of these devices when the converter is exiting a freewheeling mode of operation. Since this is rarely the case when the converter is operating under light-load conditions, these switches will not turn ON with ZVS. As a result, the proposed converter with flying capacitor has better light-load efficiency than the converter proposed in [17] because two of its switches can always turn ON with ZVS, regardless of the load.

IV. CONVERTER ANALYSIS & SELF TUNED PID using GENETIC ALGORITHM OPERATION

The analysis and design of the proposed converter are almost identical to that presented in [16] and [17] and therefore are not presented here in detail. Only graphs of key characteristic curves and general design guidelines are presented in this paper.

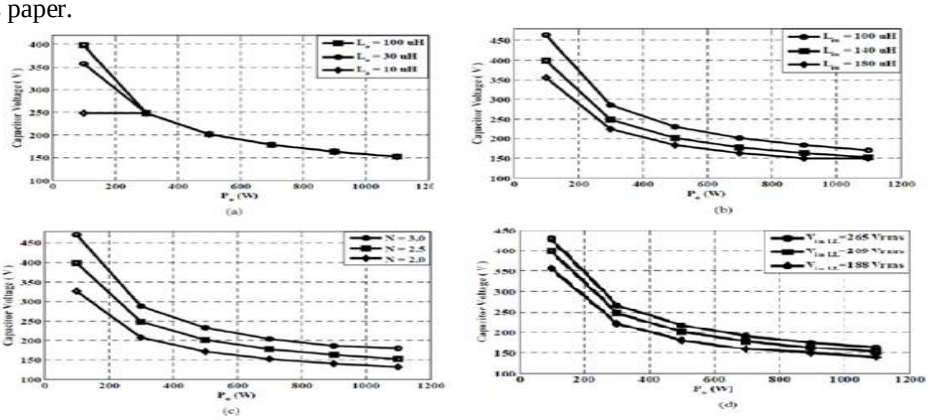

Fig. 6. Steady-state characteristic curves (Vin = 208 Vrms , Vo = 48 V, fsw = 100 kHz. (a) Effect of output inductor value Lo on dc bus voltage. (b) Effect of input inductor value Lin on dc bus voltage. (c) Effect of transformer ratio value N on dc bus voltage. (d) Effect of input voltage vin on dc bus voltage.

The reader is referred to [16] and [17] for details. In order to analyze and determine the steady-state operating points of the converter, a computer program such as the one presented in [16] has been used. Graphs of steady-state characteristics, such as the ones shown in Fig. 6, can be used as part of a design procedure. These graphs help to find out the appropriate parameter values based on the defined operating point. Assuming ideal operation to simplify the analysis, the characteristic curves of the proposed converter and the converter proposed in [17] are the same? This is because in this case, the Flying capacitor just affects the transition modes of the converter and does not affect the overall steady-state operation of the proposed converter.

Genetic Algorithm Operation

Artificial intelligence techniques have come to be the most widely used tool for solving many optimization problems. GA is a relatively new approach of optimun searching (Mitchell, 1999), becoming increasingly popular in science and engineering disciplines. GA inherits its ideas from evolution of the nature. Even a simple GA algorithm appears to be robust, and the complexity of algorithm and result of GA is irrelevant to the length of genetic string and the original state of population. GA is so simple that it only involves some selection, crossover and mutation operations, but it is so efficient that it can find a nearly optimum solution even for a large scale problem (Mitchell, 1999).

In this case, a random population of 20 real numbers double precision chromosomes is created, representing the solution space for the PID controller (*KP*, *KI* and *KD* codified like the genes of the chromosomes, in the range 0 to 1). Each member of this random population represents a different possible solution for de GA. The GA proceeds to find

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the optimal solution through several generations, the reproduction use crossover fraction of 0,6 with 2 elite count, the mutation function is adaptive feasible, and the crossover function is scattered. The objective function to minimize equation (5) was constructed using parameters of the response to step of the system, considering the magnitudes of the variables.

$$f(Tr, Ess, Ts, Mpu, \mathrm{I}_{\max}) = 100 \times Tr + Ess + 100 \times Ts + Mpu + I_{\max} \quad (1)$$

Where:

- *Tr* = Rise time [s].
- *Ess* = Steady-state error [V].
- *Ts* = Settling Time [s].
- *Mpu* = Overshoot [V].
- *Imax* = Current maximum in the inductor [A].

V. DESIGN GUIDELINES & SIMULINK RESULTS AND OUTPUTS

General considerations that should be taken into account when trying to design the proposed converter are discussed in this section of the paper. The key parameters values in the design of the converter are output inductor Lo , transformer turns ratio N, and input inductor Lin . The following should be considered when trying to select values for these components:

A. Transformer Turns Ratio N The value of N affects the primary-side dc bus voltage. It determines how much reflected load current is available at the transformer primary to discharge the bus capacitors. If N is low, the primary current may be too high, and thus, the converter will have more conduction losses. If N is very high, then the amount of current circulating in the primary side is reduced, but the primary current that is available to discharge the dc-link capacitors may be low, and thus, dc bus voltage may become excessive under certain operating conditions (i.e., high line). The minimum value of N can be found by considering the case when the converter must operate with minimum input line and, thus, minimum primary-side dc bus voltage and maximum duty cycle. If the converter can produce the required output voltage and can operate with discontinuous input and continuous output currents in this case, then it can do so for all cases.

B. Output Inductor Lo The output inductor should be designed so that the output current is made to be continuous under most operating conditions, if possible. The minimum value of Lo should be the value of Lo with which the converter's output current will be continuous on the when the converter is operating with maximum input voltage, minimum duty cycle, and minimum load. If this condition is met, then the output current will be continuous for all other converter's operating conditions. On the other hand, the value of Lo cannot be too high as the dc bus voltage of the converter may become excessive under very light-loads conditions.

C. Input inductor Lin : The value for L1 and L2 should be low enough to ensure that their currents are fully discontinuous under all operating conditions, but not so lowas to result in excessively high peak currents. It should be noted that input current is summation of inductor currents iL1 and iL2 which are both discontinuous. However, by selecting appropriate values for L1 (= La1 = Lb1 = Lc1) and L2 (= La2 = Lb2 = Lc2) in such a way that two inductor currents such as iLa1 and iLa2 have to overlap each other, the input current can be made.

D. Flying Capacitor Cf The flying capacitor is charged to half of the dc bus voltage.

When the converter is operated with phase-shift PWM control, as shown in Fig. 3, Cf is generally decoupled from the converter except during certain switching transitions, such as when S1 is turned OFF to start Mode 2 and when S4 is turned OFF during the equivalent mode later in the switching cycle; therefore, there is little opportunity for Cf to charge and discharge during a switching cycle. As a result, the converter can be designed according to the design procedure given in [17] as the operation of the two converters is very similar.

The following expression states the relation between Cf and its ripple voltage based on reflected load current:

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$$C_f = \frac{I.\Delta t}{\Delta V_{Cf}} = \frac{I_o(0.5 - D_{\max})}{N f_s \, \Delta V_{Cf}} \quad (2)$$

where Io is output current, Dmax is maximum duty cycle, N is transformer turns ratio, fs is switching frequency, and ΔVCf is the peak-to-peak ripple voltage of Cf . For maximum load Po = 1.1 kW and output voltage Vo = 48 V, the output current is Io = 23 A. If the maximum duty cycle is assumed to be Dmax = 0.4, the transformer turns ratio is N = 2.5, and the switching frequency is fsw = 100 kHz, then a 0.5% ripple for flying capacitor voltage results in ΔVCf = 0.005 × 400 = 2 V so that the minimum value for Cf according to (1) is Cf = 4.6 µF

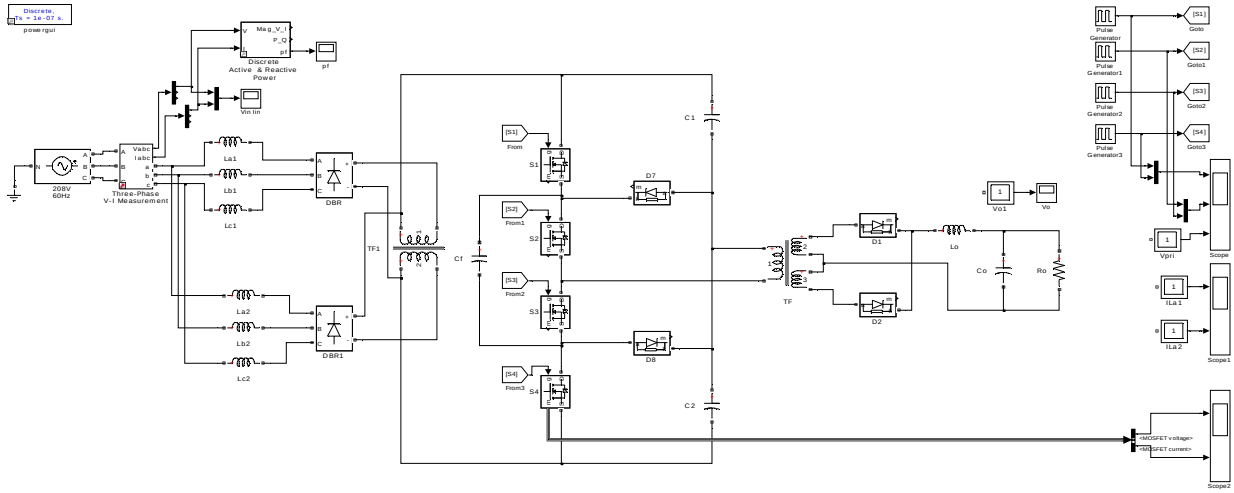
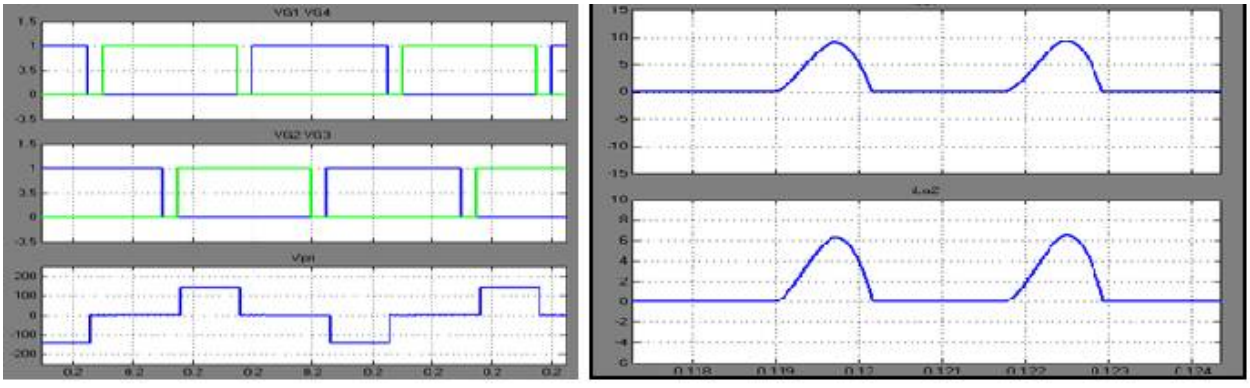


Fig 7 MATLAB/Simulink Model of the Proposed Three phase Interleaved PFC Converter



(a) (b)

Fig8. Simulation Waveforms of (a) Vg1,Vg2,Vg3,Vg4 & Primary Voltage (b) Inductor Currents Il1 ,Il2

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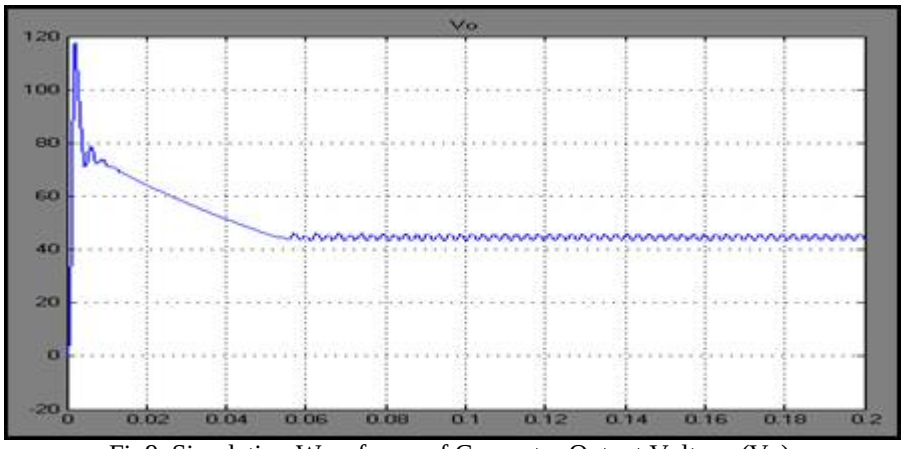

Fig9. Simulation Waveforms of Converter Output Voltage (Vo)

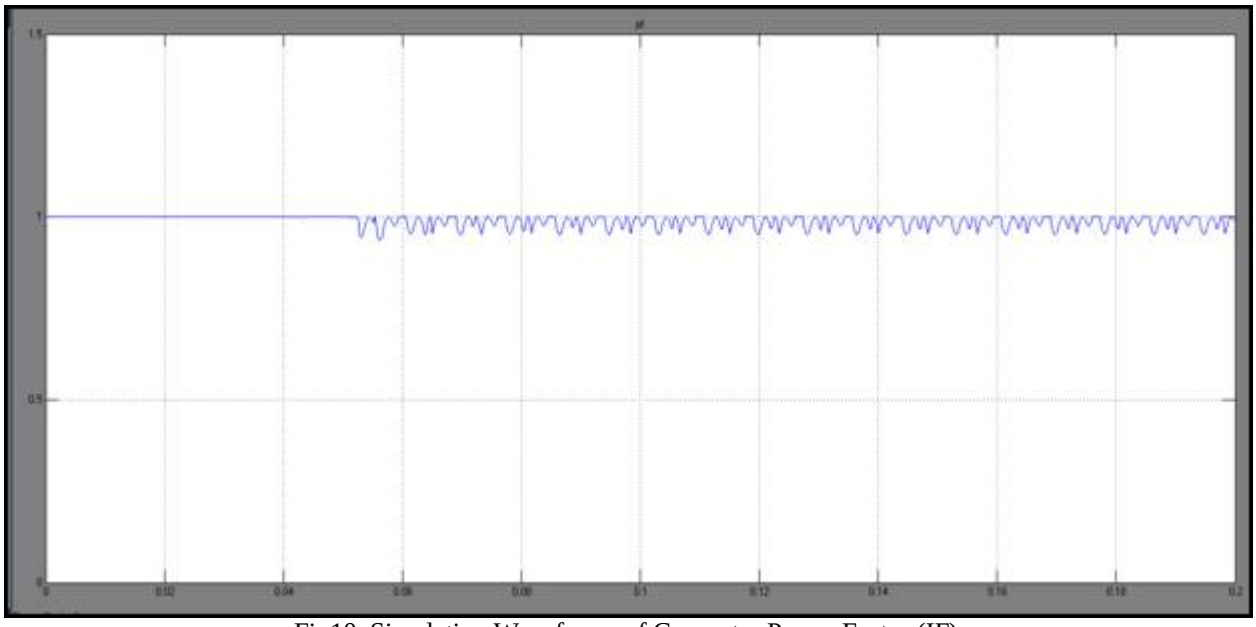

Fig10. Simulation Waveforms of Converter Power Factor (IF)

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

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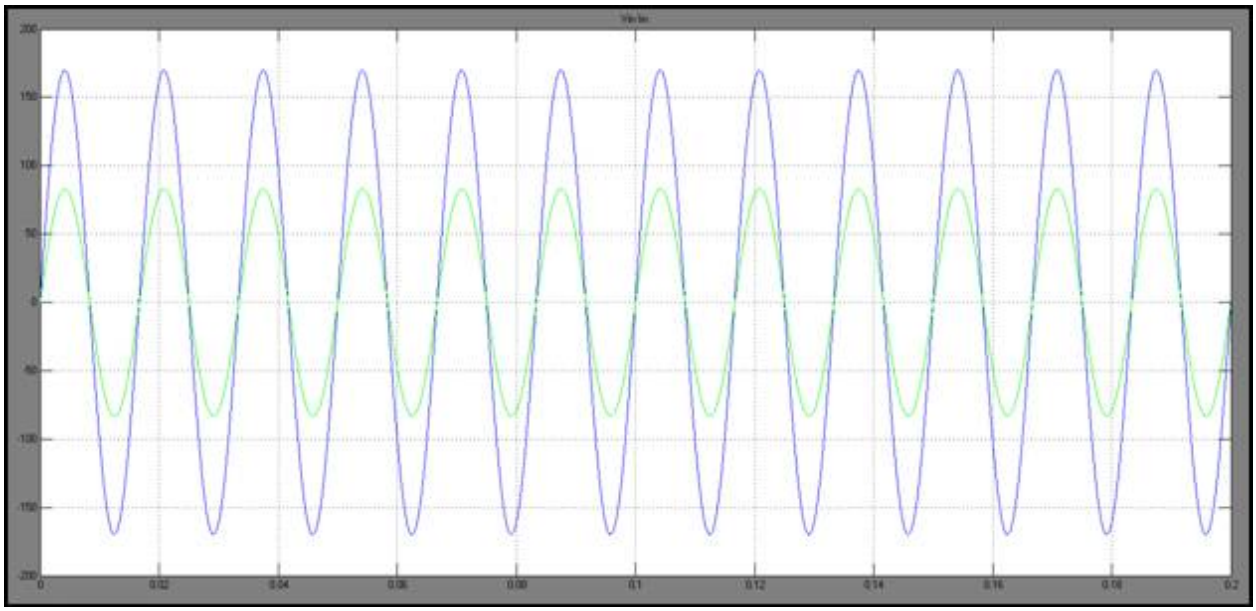

Fig11. Simulation Waveforms of Input Voltage (Vin) & Input Current (Is)

VI. CONCLUSION

In this paper we proposed a new hybrid algorithm for the regulation of voltage of the boost converter, and the active correction of the power factor. The algorithm integrates the main features of the current mode control (dynamic response, stability and PFC), and the reliability and design of PID controls. As alternative of optimal adjustment of the parameters of loop PID, considering the problem of combination and optimization of muti-variables, intends to use a genetic algorithm whose objective function is evaluated on the parameters of the answer of the model calculated from the average model of the boost converter. The scheme of control proposed was evaluated successful by simulation and on a laboratory prototype of 200 W, having demonstrated its viability and high performance in terms of output voltage regulation and PFC. An interleaved three-phase, three-level, and PFC ac–dc converter using standard phase-shift PWM was presented in this paper. In this paper, the operation of the converter was explained, and its feasibility was confirmed with experimental results obtained from a prototype converter. The efficiency of the new converter was compared to that of another converter of the same type. It was shown that the proposed converter has a better efficiency, especially under light-load conditions, and it was explained that this is because energy from the output inductor can always be used to ensure that the very top and the very bottom switches can be turned ON with ZVS, due to a discharge path that is introduced by its flying capacitor.

FUTURE SCOPE

This paper future extended on to design the controller parameters of the conventional Power Factor Correction (PFC) converter. The dynamics of the converter is nonlinear & Electrical Drive loads therefore, it is hard to derive desirable performance. Genetic algorithm is used to optimize the control parameters of PFC converter.

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