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FPGA Based IIR Filter Design and Analysis using Different Architectures

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ABSTRACT: Hardware Implementation of a circuit in its Field Programmable Gate Arrays (FPGAs) is a menacing job. Thereare plenty of ways in which any digital or analog circuit can be implemented. A lot of time and labour can be saved if a carefulchoice is made on implementation method. Design specification is an important parameter to determine the implementation methodology. By using various design tools these specifications can be converted to hardware descriptive languages (VHDLand Verilog) which reduce the complexity and provide an ease todefine a circuit more comfortably. In this paper a 64-Tap IIRfilter is designed using Fully Parallel and Partial Serialdesigning architectures and further these designs are implemented on FPGA.Hardware synthesis results in 67% utilisation of area along with20 multipliers using fully parallel design architecture whereas partially serial designing architecture uses only 10% of theavailable area with only 12 multipliers only. The results showthat the partially serial architecture uses 28% lesser multipliersas that of fully parallel implementation. Also the simulated filterdesign provides an approach which is much moreefficient in terms of area, speed and cost.

KEYWORDS: Field Programmable Gate Array (FPGA), InfiniteImpulse Response (IIR) Filter, Statistical Analysis, Synthesis.

I.INTRODUCTION

Each technology now a days is focused on cost reductionalong with an efficient performance. In order to yield lessercost, number of components needed to implement the designneeds to be minimised. Also for the lesser number ofcomponents, maintenance becomes easy. Thereare plenty ofdigital control techniques used to provide improvisation inthe reliability as well as performance. In generalmicrocontrollers, microprocessors, and DSPs are commonlyused to implement discrete-time control schemes and controlalgorithm [1, 2]. Significant advancements in the area ofdigital computers technology have provided a noteworthydevelopment in DSP. In the Digital Signal Processingvarious methods may be employed to enhance the overallthroughput of a system. One method to improve throughputof a system and to make it reliable is filtering.Filter is generally a circuit which acts as a selector to stop orpass a particular frequency range. There is a widecategorisation of these filters, whether analog (low pass,high pass, band stop and band pass) having input and outputas continuous-time signals or digital (IIR, FIR filters)imparting discrete time signals as input and output of afilter. The filters of prior focus in DSPs are IIR (infiniteimpulse response) filter, FIR (finite impulse response) filterwhich can be either of low pass, high pass, band stop orreject depending over the area of interest for which thecircuit is to be designed and further implemented in an orderto increase the utilisation factor [3].

Filter designing need parameters to be specified well beforein order to meet design specifications. By varying the valueof filter coefficients, response of filter can be calculated andvaried as well.In digital filters, if designed for same order, IIR filters arepreferred over FIR as they provide better frequencyresponse. Butterworth filters in IIR filtering have an edgeover other filters as they impart maximally flat frequencyresponse as well as there are no ripples in the pass band [4],[5]. It rolls off towards zero in the stop band. Frequencyresponse of Butterworth filter for different values of N isgiven below:

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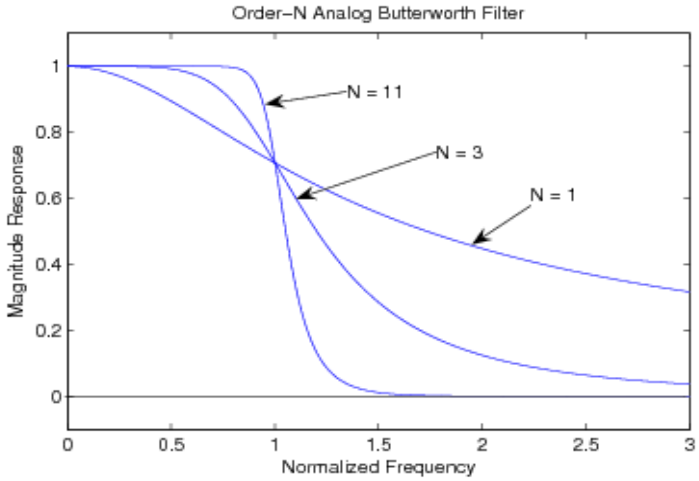

Fig. 1: Frequency response of Butterworth filter [4]

Exceptional performance of digital filters in DSP has raised its popularity in the recent years. This is because of the improved SNR as compared to analog filter. Analog filters add noise or other signals as a result of interference, hence degrades the required SNR. [4]

After developing these filters using some tool, these can be further implemented using the various FPGAs versions. These (FPGAs) give a proper insight of the overall performance of the system and also reduces the computational complexity. There are various types of FPGAs used in industries now a days. The implementation of design uses different types of FPGA families and target devices and yield resources corresponding to them. At early times programming was carried out using PLAs, PALs, CPLDs etc., but with a lot of compromises. With the new emerging technologies, advancements were made and an ultimate solution to all the shortcomings was provided in the form of FPGA [6].

II. FIELD PROGRAMMABLE GATE ARRAY

FPGA stands for field programmable gate array. It is an integrated circuit which can be implemented according to the end user's need. This technology has arrived in the mid-80s and was a lot appreciated because of its performance in various fields as in terms of performance and efficiency. It can integrate more than 10 million of gates and along with a lot many macro-functions provided as memory blocks and DSP units. One more reason for its reliability is its ease of programming. There can be multiple processes taking place at the same time on a single chip as it supports parallelism. A large improvement was made which in turn reduced the time-to-market that was needed for the new applications. All the above mentioned features make FPGA centre of attraction as it was user –friendly technology and was used in various applications. Working languages for the FPGAs generally are hardware description language (HDL) also it can be programmed using Verilog language which is somewhat similar to the HDL and can be designed for a particular application (ASICs) [2].

In today's scenario the parallelism property is widely used, which means many instructions are to be executed at a particular time instant, or we can say that it need to execute or perform multiple tasks simultaneously. So the remedy for this problem is FPGA. Another main feature of the FPGA is its throughput, which is a lot higher than the conventional DSPs and also at a very low cost of implementation. As mentioned earlier that these (FPGA) are ASICs based so it can be designed according to the end users need. FPGAs are a combination of many others sub-parts as well, which combine to form FPGA chip, which is capable of performing any operation required for the application or defined by the user. The various sub-parts includes digital sources which are various logic gates as AND and XOR , some register as they as need memory which is implied using flip flops , programmable logic blocks, interconnects to wire the various blocks that can be reconfigured accordingly, multipliers and sometime CPUs as well. FPGAs can be used to determine the circuit's reliability or its efficiency. An FPGA has an application to solve any problem which is

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related to computation. FPGA can be used to implement a soft microprocessor, such as the Xilinx Micro blaze or Altera Nios II. FPGA has gained popularity in various fields as in Aerospace and defence, Consumer electronics, and medical fields as well. Other various applications involve image processing, robotics, neural network and communication as well. The FPGA can be used as a controlling device and is a combination of various modules like A/D conversion control module, synchronization and modulating signals generation module etc. [7].

III.IIR FILTER DESIGN SIMULATION

To derive the transfer function H(z) of a system, digital filter design process is generally used. Digital filters are derivedusing two approaches: Infinite Impulse Response(IIR) or Finite Impulse Response (FIR). IIR filters do have feedback associated with them whereas FIR (finite impulse response filters) doesn't. As mentioned earlier, these filters (IIR Filters) are used generally in the linear time invariant (LTI) systems [3]. In real practice, the impulse response of these filters is almost zero or approaches to zero at higher values and is neglected after a certain point. However the physical systems which give rise to IIR or FIRresponsesis notsimilar. Analog electronic filters are compositionof components like resistor, inductors and capacitors and sometimes linear amplifiers and the combination of all the above mentioned is generally called as IIR filters. On the other contrary, discrete-time filters, which are based on a tapped delay with no feedback associated with them, are necessarily the FIR filters. The memory elements in the analog filters are capacitors or inductors generally and their internal state never completely relaxes following an impulse. But in the another case, after an impulse has occurred at the end of the tapped delay line, then the system has no further memory of that impulse and has to be returned to its initial state. The impulse response is exactly zero beyond that point [8]. Diagrammatically IIR filter is represented as:

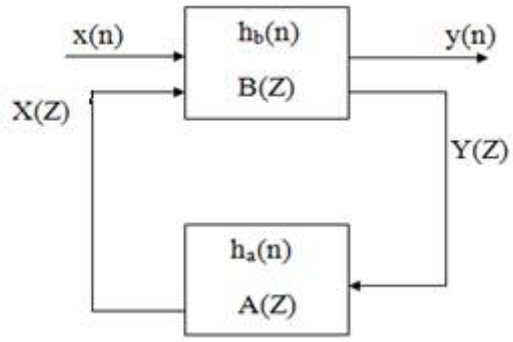

Fig. 2: Block diagram of IIR filter

Recursive filters use long convolution and achieve long impulse response in a very efficient manner. These filters employ a very fast processing speed as they can process the signal very rapidly [9]. The impulse response of these two filters is generally decaying exponentially, whereas there are digital filters, which uses the convolution process named as FIR filters. The IIR filter's methodology is to convert the specifications of the digital filter into a low pass analog prototype filter specifications. It can determine the transfer function Ha(s) of the analog low pass filter. In this paper we have designed a 64-Tap low pass IIR Butterworth with 48 KHz and 10.8 KHz as sampling frequency (Fs) and cut-off frequency (Fc) respectively. The magnitude and the phase response of the same are discussed below:

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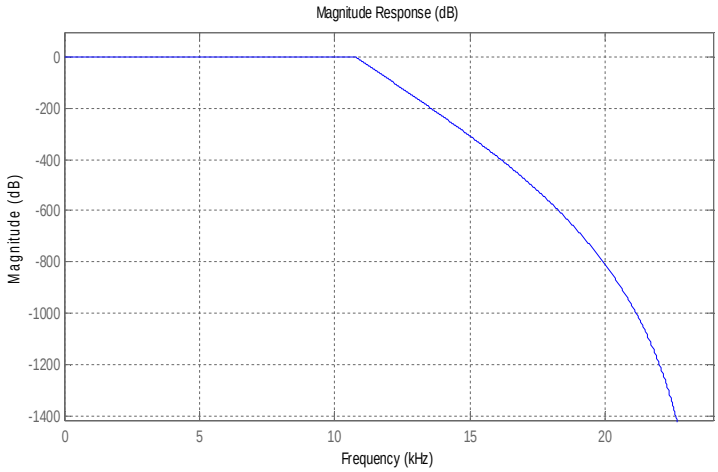

Fig. 3: Magnitude response of IIR filter

A 64- tap low pass Butterworth IIR filter is designed with fixed- point filter arithmetic.

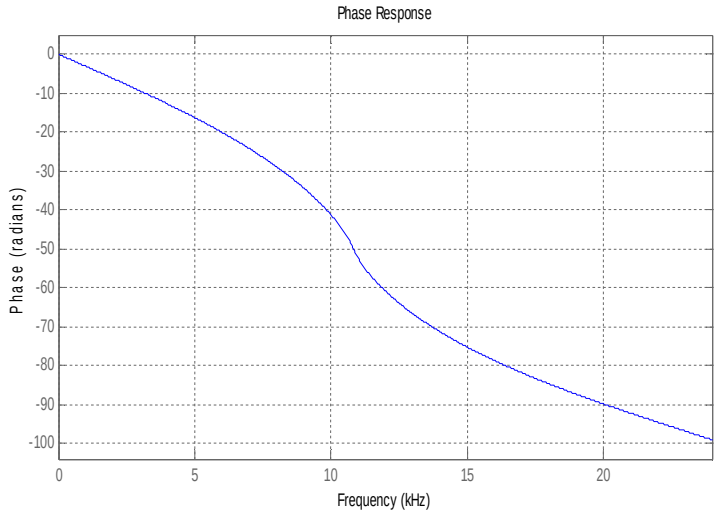

Fig. 4: Phase response of IIR Filter

As discussed above that hardware implementation requires proper selection of the methodology to yield better result. Parameter selection and the architecture play a vital role in an efficient designing. There are plenty of ways in which implementation can be enhanced like by variation in physical parameters (order of filter, frequencies associated etc.) or by using various architectures for designing (parallel, serial, partial serial etc.) [3], [10]. In this paper we will be taking the fully parallel and partially serial architecture as a centre of focus for the filter designing.

IV.HARDWARE SYNTHESIS

As discussed above that hardware implementation requires proper selection of the methodology to yield better result. Parameter selection and the architecture play a vital role in an efficient designing. There are plenty of ways in which implementation can be enhanced like by variation in physical parameters (order of filter, frequencies associated etc.) or

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by using various architectures for designing (parallel, serial, partial serial etc.) [3][10]. In this paper we will be taking the fully parallel and partially serial architecture as a centre of focus for the filter designing.

1. Parallel IIR filter design: Partial fraction is employed for the IIR filter in parallel-form using the transfer function H(z) of the system under consideration. Cost effective circuits can be made using small filter order. Small order ensures less multiplier used to carry out filter equation [11], [12]. Mathematically the transfer function can be given as follows:

$H(z) = C + \sum H_k(z)$ (1)

(Summation varies from k=1 to n.)

The transfer function for the 2nd order is given by:

$$H_k(z)=\frac{b_{ko}+b_{k1}z^{-1}}{1+a_{k1}z^{-1}+a_{k2}z^{-2}} \quad (2)$$

The equation no. (1) is generally equal to the equation representation of the IIR filter ideal equation representation.The k in equation no. (1)is the integer part of (N+1)/2.Poles and coefficient constitute a Transfer Function H(z). The diagram equivalent can be given as:

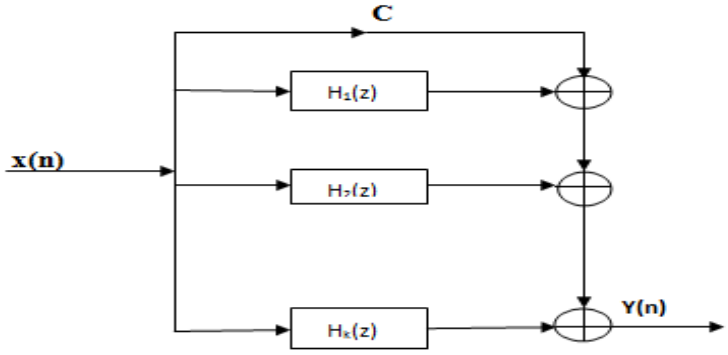

Fig. 5: Parallel-Form of IIR filter

Fully parallel architectures are generally used in the designing because of the speed of operation they provide.

2. Partially serial: Another form of architecture is the serial form. Serial form is easy to implement as compared to the parallel but the speed is compromised as it follows step wise formation where the output of one stage is the input to the second and so on. Block diagram representation is given as:

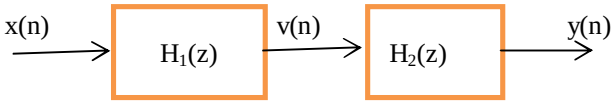

Fig. 6: Serial Form of IIR Filter

Partially serial architecture is the combination of serial along with parallel architectures. Initial stage can be parallel followed by serial architecture and vice versa.

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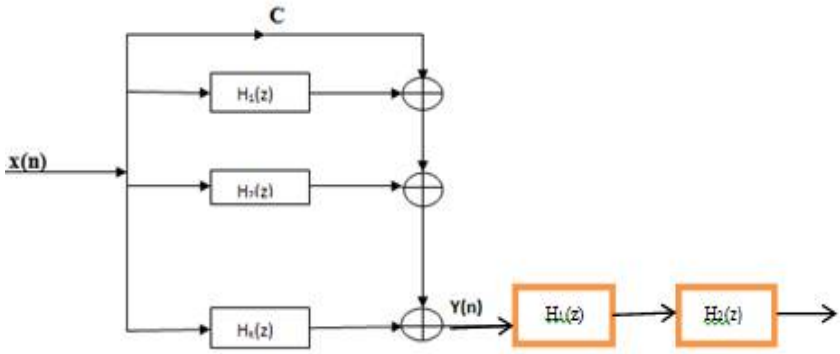

Fig. 7: Partially serial form of IIR Filter

The advantage of using partially serial approach over the serial or the parallel form is that it implies the positive points of both the designing architecture which eliminates shortcomings of both and results in overall better performance [3], [12].

V. RESULT AND DISCUSSION

Table 1 show results after filter design simulation on FPGA. The resource utilisation is given for Total slice flip flops, LUTs, IOBs and multipliers.

Table 1: Resource Utilisation Comparison

Logic utilisation	Fully Parallel Used/Avail.	Partially serial Used/Avail.
Total slice flip flops	1523/17344	2083/17344
No. Of 4- input LUTs	11706/17344	1796/17344
No. of bonded IOBs	35/190	35/190
MULTI18×18SIOs	20/28	12/28
Speed	36.444 MHz	34.559 MHz

The simulated designed is implemented on Spartan3E XC3S1200E device of FPGA in the form of HDL code. The above presented table gives proper insight of the overall throughput yielded by both the designing architectures under consideration.

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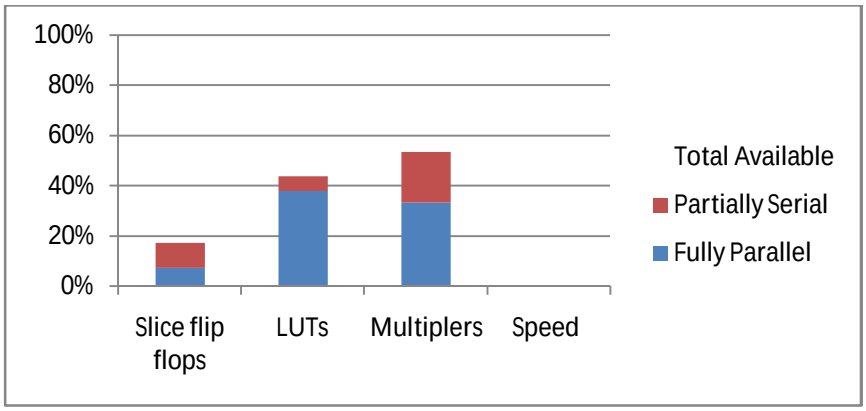
Table2: Bar chart Resource Utilisation Comparison



On the basis of above given bar chart representation, it can be clearly visualised that the usage of area is much more with Fully Parallel as compared to the Partially Serial method.

VI.CONCLUSION

The above given comparison gives a complete insight of the performance and analysis of Fully Parallel and Partially serial architecture with folding factor =64 of the 64- Tap IIR filter. It can be easily concluded on the basis of results that the partially serial architecture is better for this design as it uses lesser no. of LUTs available on chip along with lesser no. of multipliers which reduces the total area occupied. This (partially serial) architecture uses 57% lesser area than that of the parallel form. Also the usage of multipliers in partially serial form is 28% lesser as compared to the fully parallel form which uses 71% of the total provided multipliers on FPGA. Lesser multipliers reduce the cost of the design without any compromise with the speed which is also comparable.

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