ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 9, September 2016

Speed Control of DC Motor with Modified SEPIC Rectifier

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ABSTRACT: This paper proposes a new single-phase ac-dc power factor correction (PFC) bridgeless single ended primary inductor converter (SEPIC) rectifier with speed control of DC motor. It is used to improve the efficiency at low input voltage and reduce the switch-voltage stress. The absence of an input rectifier bridge in the SEPIC rectifier results in less conduction losses. Lower switch voltage stress allows utilizing a MOSFET. The topology is designed to operate in discontinuous conduction mode (DCM) to achieve almost a unity power factor. The DCM operation have advantages such as zero-current turn-on in the power switches and simple control circuitry. Speed control of the DC motor is done using this bridgeless SEPIC rectifier. Converter output is given to the input of the DC motor.

KEYWORDS: Power factor correction (PFC), bridgeless SEPICrectifier, DC motor, discontinuous current mode (DCM).

I.INTRODUCTION

Advantages of single ended primary inductor converter (SEPIC) circuit are isolation easy, EMI small and input current is continuous. The working principle of the different modes of the SEPIC-PFC areanalyzed. It is note that there are several problems in traditional circuit, such as the great loss of rectifier bridge structure, the reverse current recovery under continuous mode and so on. To solve the above mentioned problem, a new bridgeless SEPIC PFC circuit is presented.Based on traditional SEPIC power factor correction, new circuits utilize the bridgeless technique instead of the pre-rectifier in the corrector. In the process of turning on the switch, the input current only flow one diode, and it can effectively reduced energy consumption in the conduction process. The circuit works in the current DCM. The DCM operation results in soft turn-on switching and relatively low inrush current. The proposed bridgeless rectifier with coupled magnetic configurations results in higher overall efficiency and higher power density. The proposed topology has some advantages over the conventional SEPIC converter, such that the dc output voltage is lower than the peak input voltage, input–output isolation can be easily implemented.

II. SYSTEM MODEL AND WORKING

The proposed bridgeless power factor correction SEPIC converter with DC motor circuit is shown in Fig. 1. The proposed bridgeless configuration willreduce the conduction losses. The multiplier cell (D_1, $C_3$and D_2, C_3) will increase the gain and reduce the switch voltage stress. The proposed circuit consists of two symmetrical configurations and each will operate in a half-line cycle. Circuit consists of ac input voltage; 2 switches: Q_1 and Q_2; 5 diodes D_0, D_1, D_2, $D_p$and D_n; 3 inductors: L_0, L_1 and L_2; 3 capacitors: C_0, C_1 and C_2 and the DC motor. By the two diodes $D_p$and D_n, the output ground is always connected to the terminals of input ac voltage, which stabilizes voltage potential of output ground. The three separate inductors can be magnetically coupled into a single magnetic core to attain very low input current ripples. The proposed converter utilizes two non-floating switches, Q_1 and Q_2. Switch$Q_1$is turned ON/OFF during the positive half-line cycle andthat of switch $Q_2$is in negative half-line cycle. The two power switches Q_1 and Q_2can bedriven by the same control signal.

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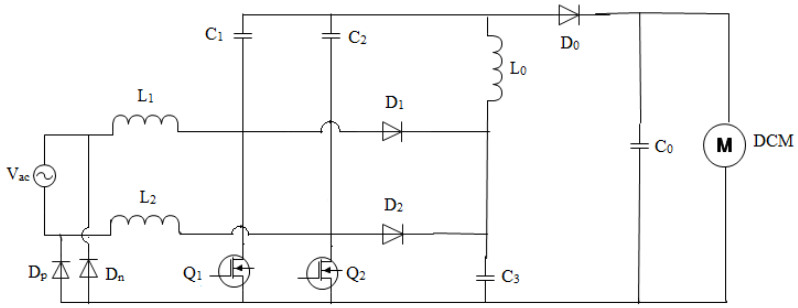

Fig. 1. Proposed bridgeless PFC SEPIC rectifier fed DC motor.

The circuit operation during one switching period $T_s$in a positive half-line period with the three inductors operating in DCM, can be divided into three distinct operating modes. They are:

MODE 1

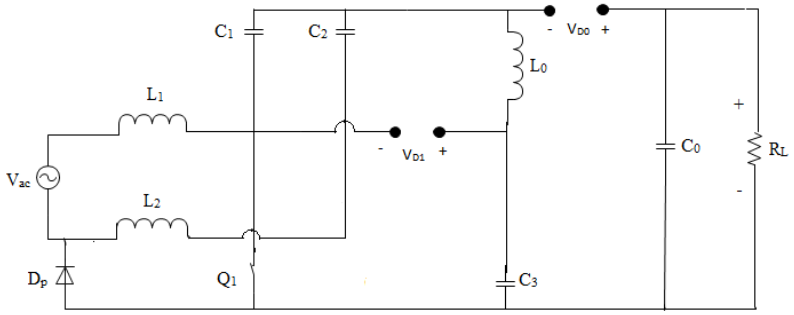

Fig. 2.Mode 1- Switch ON topology.

The mode 1- switch ON topology is shown in Fig. 2. Switch $Q_1$is turned-on by the control signal. Both the diodesD_1 and D_0 are reversed biased. In this stage, the three-inductor currents increase linearly at a rate proportional to the input voltage V_{ac}.

MODE 2

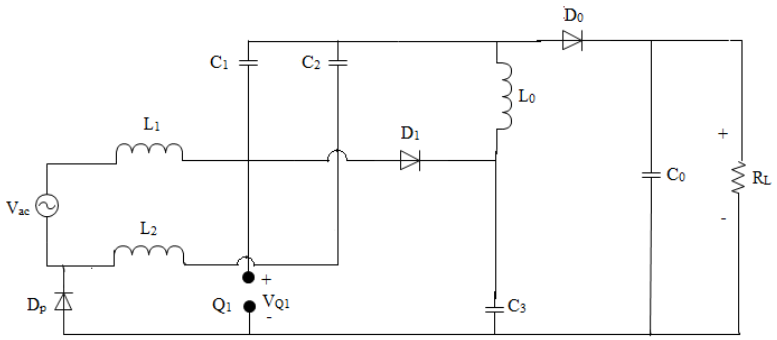

Fig. 3.Mode 2- Switch OFF topology.

The mode 2- switch OFF topology is shown in Fig. 3.Switch $Q_1$is turned-off. Both the diodes D_1 and D_0 will conduct simultaneously. These will provide a path for the currents of the three inductors. The three inductors' currents decrease linearly at a rate proportional to the capacitor C_1voltage V_{C1}. This stage continues till the sum of the currents flowing in the inductors adds up to zero,hence diodes D_1 and D_0 are reverse biased.

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MODE 3

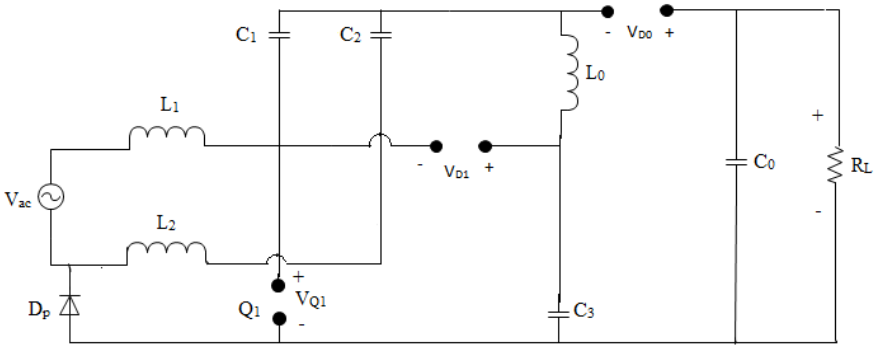

Fig. 4.Mode 3- DCM topology.

The mode 3- DCM topology is shown in Fig. 4.Switch Q_1remains turned-off. Both the diodesD_1 and D_0 are reverse biased. Diode $D_p$provides a path for the current of the inductor L_0. The three inductors behave as current sources, so there will be constant currents. Thereby, the voltage across the three inductors is zero. This period ends when switch $Q_1$is turned-on initiating the next turn-on of the switching cycle.

III. SIMULATION

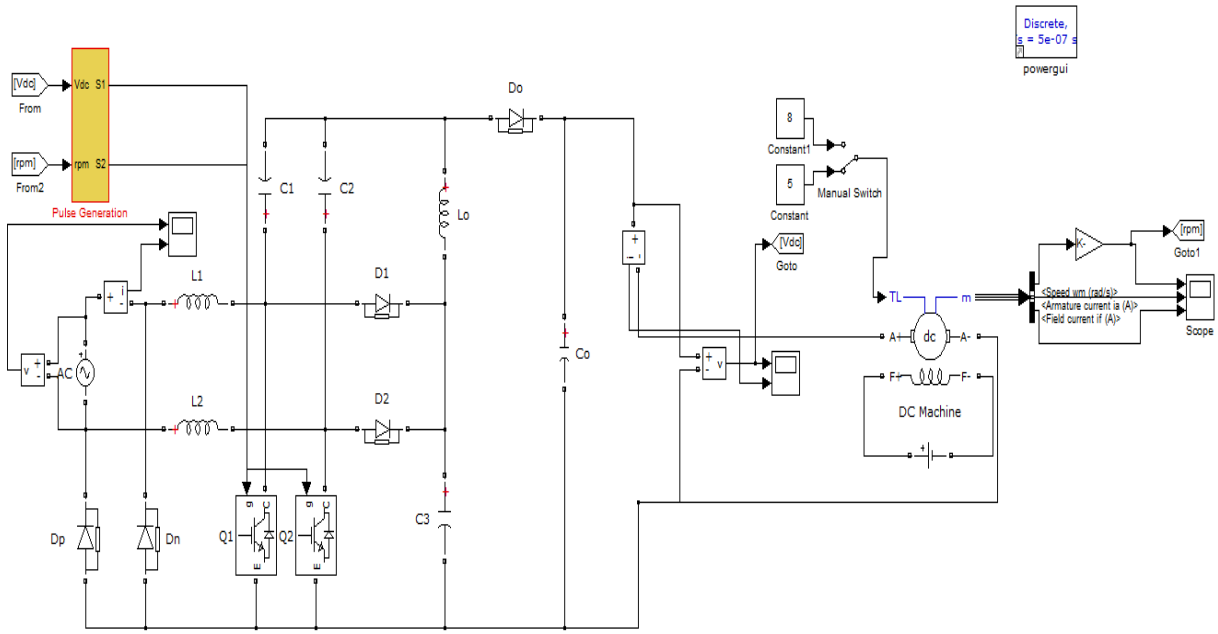

Fig. 5. Simulink model of the bridgeless PFC SEPIC converter fed DC motor.

The simulation was done in MATLAB/Simulink. The simulink model of the bridgeless PFC SEPIC converter fed DC motor is shown in the Fig. 5. The gate pulses generated for turn on/off of the switches are plotted. The output voltage and output current waveforms of the SEPIC rectifier are obtained. The speed, armature current and field current of the DC motor are also obtained from the Simulink model. Closed loop control is adopted for the proposed system.

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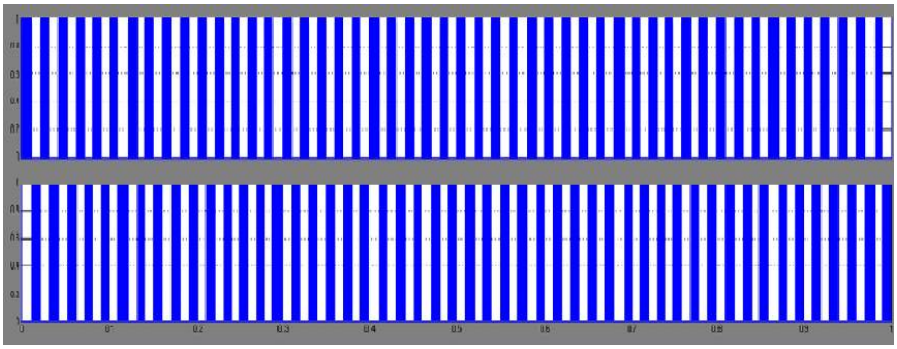

Fig. 6. Gate pulses for the switches $Q_1$and Q_2.

Here the proposed SEPIC converter input voltage is taken as 120V ac. The output voltage is designed for 54V dc. The gate pulses generated for the switches Q_1 and Q_2 are shown in the Fig. 6. The simulation result of the power factor obtained from the SEPIC rectifier is shown in the Fig. 7.

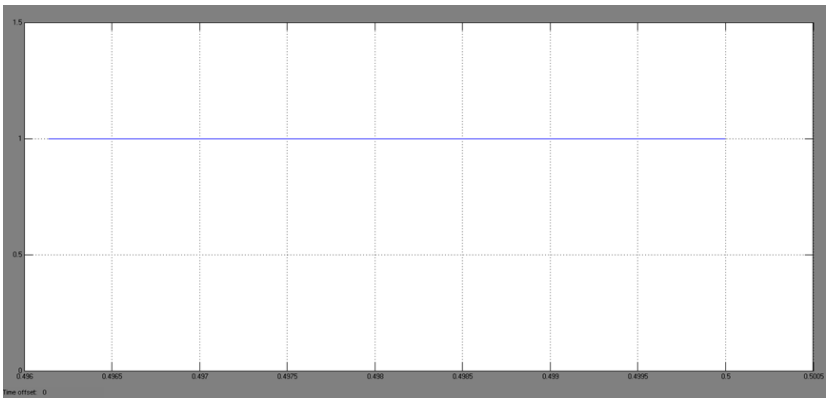

Fig. 7. Simulation result of the power factor obtained from the SEPIC rectifier.

The switching frequency is 50kHz. Simulation results of output voltage and output current of the SEPIC rectifier are shown in Fig. 8. The output voltage obtained is 400V and output current obtained is 0.5A.

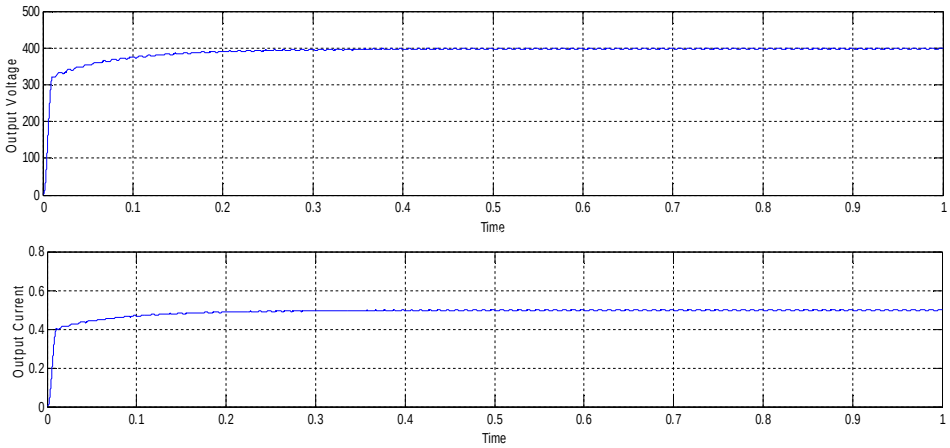

Fig. 8. Simulation results of output voltage and output current of the SEPIC rectifier.

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Simulation results of the speed, armature current, field current of the DC motor are shown in Fig. 9. The speed of the DC motor is obtained as around 1800 rpm and the armature current obtained almost as 0.1A.

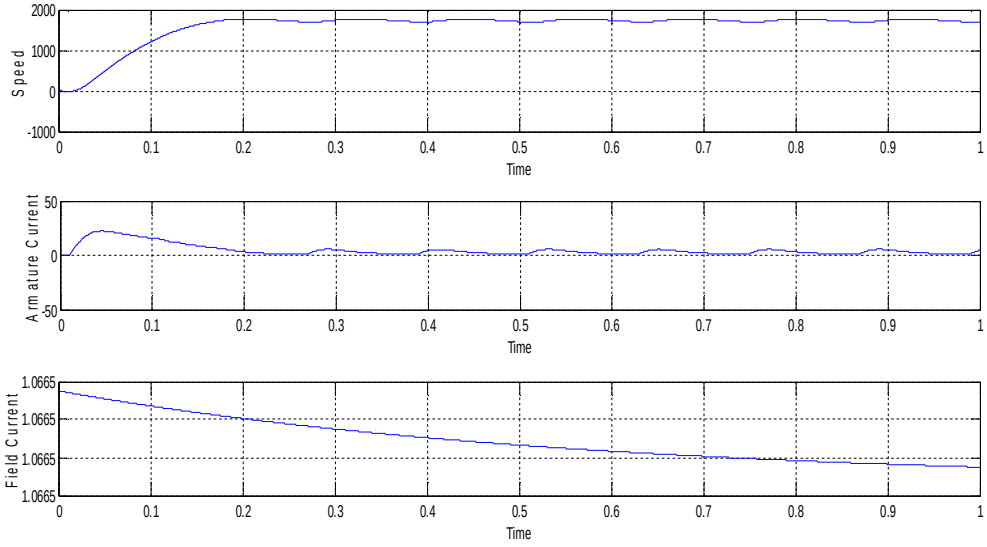

Fig. 9. Simulation results of the speed, armature current, field current of the DC motor.

IV. HARDWARE IMPLEMENTATION

Hardware implementation of the proposed bridgeless PFC SEPIC rectifier fed DC motor is given in the Fig. 10. The hardware setup consists of SEPIC converter circuit, driver circuit, control circuit and DC motor. The driver circuit contains FAN7382 used as the IC for the MOSFET. The processor chosen is ATmega328P, which is a low-power CMOS 8-bit microcontroller.

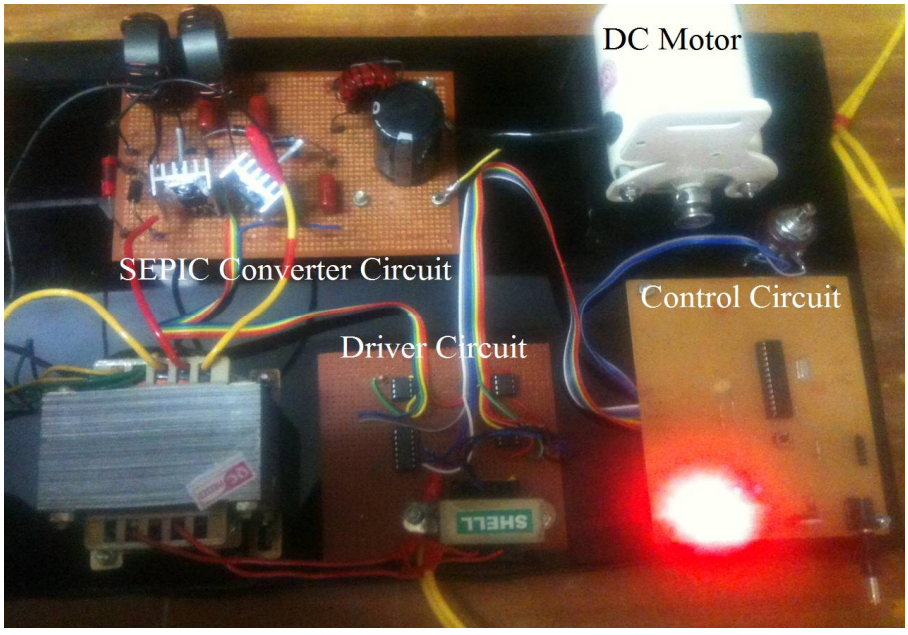

Fig. 10. Hardware implementation of the bridgeless PFC SEPIC rectifier fed DC motor.

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The result obtained from the hardware setup is given below. Hardware result of the gate pulses of the switches $Q_1$and Q_2 is shown in Fig. 11.

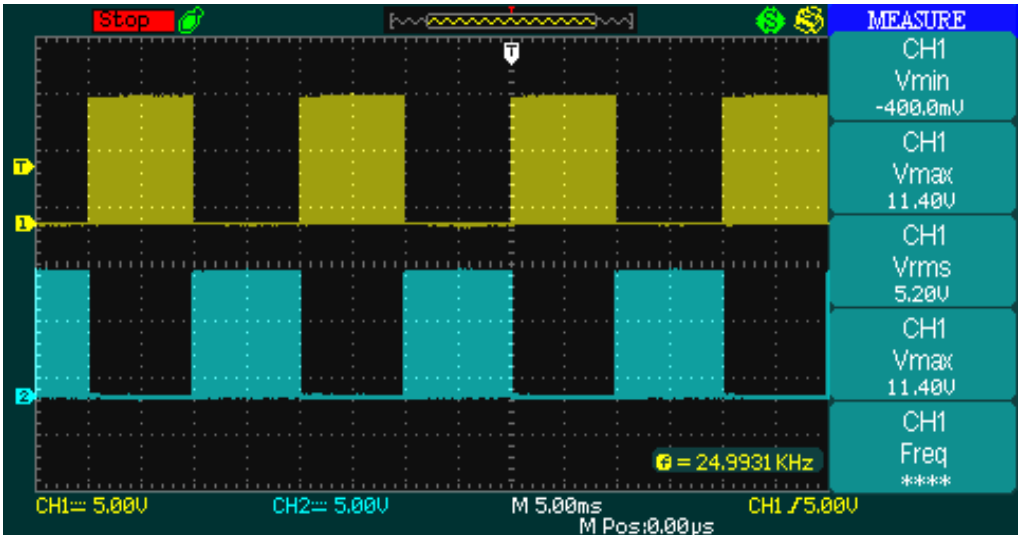

Fig. 11. Hardware result of the gate pulses of the switches $Q_1$and Q_2.

V. RESULT AND DISCUSSION

The proposed bridgeless power factor correction SEPIC rectifier fed DC motor is shown in Fig. 1 and its modes, mode1-switch ON topology is shown in Fig. 2, mode 2-switch OFF topology is shown in Fig. 3 and mode 3-DCM topology is shown in Fig. 4. Simulink model of the proposed SEPIC rectifier fed DC motor is given in Fig. 5. The simulation results obtained are given in the Fig. 6, 7, 8 and 9. Then the hardware is implemented. Hardware setup of the proposed SEPIC rectifier fed DC motor is given in Fig. 10. The result obtained from the hardware setup is given in the Fig. 11.

VI.CONCLUSION

A single phase ac-dc bridgeless power factor correction SEPIC converter fed DC motor is proposed in this paper. The SEPIC converter output is given to the input of the DC motor. The DC motor is driven by the voltage 54V. The proposed bridgeless rectifier with coupled magnetic configurations results in higher overall efficiency and higher power density. The proposed topology has some advantages such that the dc output voltage is lower than the peak input voltage, input–output isolation can be easily implemented. Experimental results are provided to confirm the converter operation in reference to conventional SEPIC converter operation.

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