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PFC Bridgeless Buck Boost Converter Fed BLDC Motor Drive

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ABSTRACT: Nowadays efficiency and cost are the major concerns in designing and developing low-power applications. Due the several advantages of brushless direct current motors (BLDC). These features are high efficiency, high flux density per unit volume, low electromagnetic interference, silent operation and low maintenance requirements. However, the use of BLDC motors is not limited to domestic applications only.This paper presents a power factor corrected (PFC) bridgeless (BL) buck boost converter fed brushless direct current (BLDC) motor drive as a cost effective solution for low power applications. An approach of speed control of the BLDC motor by controlling the dc link voltage of voltage source inverter (VSI). This helps the operation of VSI at fundamental frequency switching by using the electronic commutation of the BLDC motor which offers reduced switching losses. The diode bridge is eliminated using bridgeless configuration thus reducing the conduction losses associated with it. A PFC BL buck boost converter is designed to operate in Discontinuous Current Mode (DCM) to provide a better PFC at ac mains. This drive is compared with the conventional PFC scheme and without PFC scheme and shows satisfactory performance. The performance of the proposed drive is simulated in MATLAB/Simulink.

KEYWORDS: Bridgeless (BL) buck boost converter, brushless direct current (BLDC) motor, discontinuous current mode (DCM), power factor corrected (PFC), power quality..

I.INTRODUCTION

Nowadays efficiency and cost are the major concerns in designing and developing low-power applications, such as fans, air conditioners, blowers, mixers and other household devices. Due the several advantages of brushless direct current motors (BLDC) operating under these circumstances, a continuous growth in the number of applications has been noticed during the past years. These features are high efficiency, high flux density per unit volume, low electromagnetic interference, silent operation and low maintenance requirements. However, the use of BLDC motors is not limited to domestic applications only. They provide suitable solutions also for medical equipment, motion control, transportation or many other industrial tools. As energy consumption gained such an importance all over the world in order to fulfil the enormous demand, strict regulations have been announced by worldwide organizations like International Electro technical Commission (IEC) regarding the power quality of applications. Therefore, more advanced and "supply friendly" applications need to be developed by manufacturers. The choice of mode of operation of PFC converter is critical issue because it directly affects the cost and rating of the components used in the PFC converters. DCM is preferred as it requires only one sensor compared to CCM.

II. PFC BL BUCK–BOOST CONVERTER-FED BLDC MOTOR DRIVE

Fig. 1 shows the proposed BL buck–boost converter-based VSI-fed BLDC motor drives. The parameters of the BL buck–boost converter are designed such that it operates in discontinuous current mode (DCM) to achieve an inherent power factor correction at ac mains. The speed control of BLDC motor is achieved by the dc link voltage control of VSI using a BL buck–boost converter. This reduces the switching losses in VSI due to the low frequency operation of VSI for the electronic commutation of the BLDC motor. The performance of the proposed drive is evaluated for a wide range of speed control with improved power quality at ac mains.

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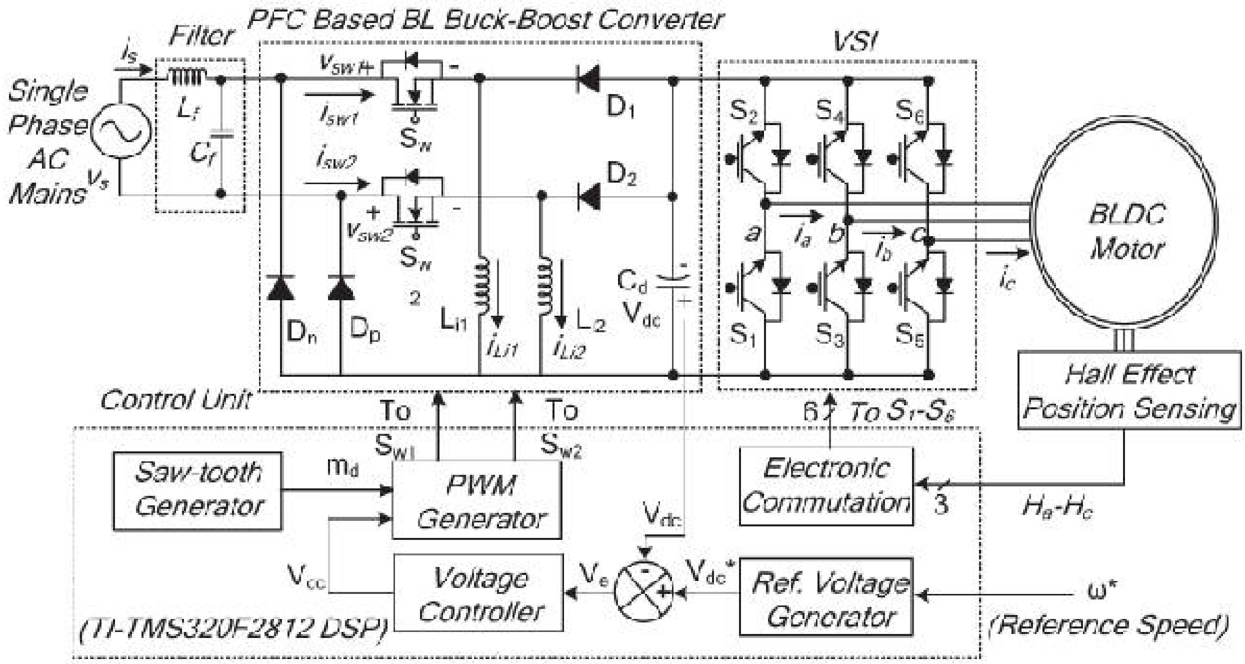

Figure 1 BLDC motor drive with front end BL Buck Boost Converter

III. OPERATING PRINCIPLE OF PFC BL BUCK–BOOST CONVERTER

The operation of the PFC BL buck–boost converter is classified into two parts which include the operation during the positive and negative half cycles of supply voltage and during the complete switching cycle.

- Operation During Positive and Negative Half Cycles of Supply Voltage

In the proposed scheme of the BL buck–boost converter, switches Sw1 and Sw2 operate for the positive and negative half cycles of the supply voltage, respectively. During the positive half cycle of the supply voltage, switch Sw1, inductor Li1, and diodes D1 and Dp are operated to transfer energy to dc link capacitor Cd asshown in Figure 2(a)–(c). Similarly, for the negative half cycle of the supply voltage, switch Sw2, inductor Li2, and diodes D2 and Dn conduct as shown in Figure 3(a)–(c).In the DCM operation of the BL buck–boost converter, the current in inductor Li becomes discontinuous for certain duration in a switching period. Figure 2(d) shows the waveforms of different parameters during the positive and negative halfcycles of supply voltage.

- Operation during Complete Switching Cycle

Three modes of operation during a complete switching cycle are discussed for the positive half cycle of supply voltage as shown hereinafter.

Mode I: In this mode, switch Sw1 conducts to charge the inductor Li1; hence, an inductor current iLi1 increases in this mode as shown in Figure 2(a). Diode Dp completes the input side circuitry, whereas the dc link capacitor Cd is discharged by the VSI-fed BLDC motor as shown in Figure 3(d).

Mode II: As shown in Figure 2(b), in this mode of operation, switch Sw1 is turned off, and the stored energy in inductor Li1 is transferred to dc link capacitor Cd until the inductor is completely discharged. The current in inductor Li1 reduces and reaches zero as shown in Figure 3(d).

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Mode III: In this mode, inductor Li1 enters discontinuous conduction, i.e., no energy is left in the inductor; hence, current iLi1 becomes zero for the rest of the switching period. As shown in Figure 2(c), none of the switch or diode is conducting in this mode, and dc link capacitor Cd supplies energy to the load; hence, voltage Vdc across dc link capacitor Cd starts decreasing. The operation is repeated when switch Sw1 is turned on again after a complete switching cycle.

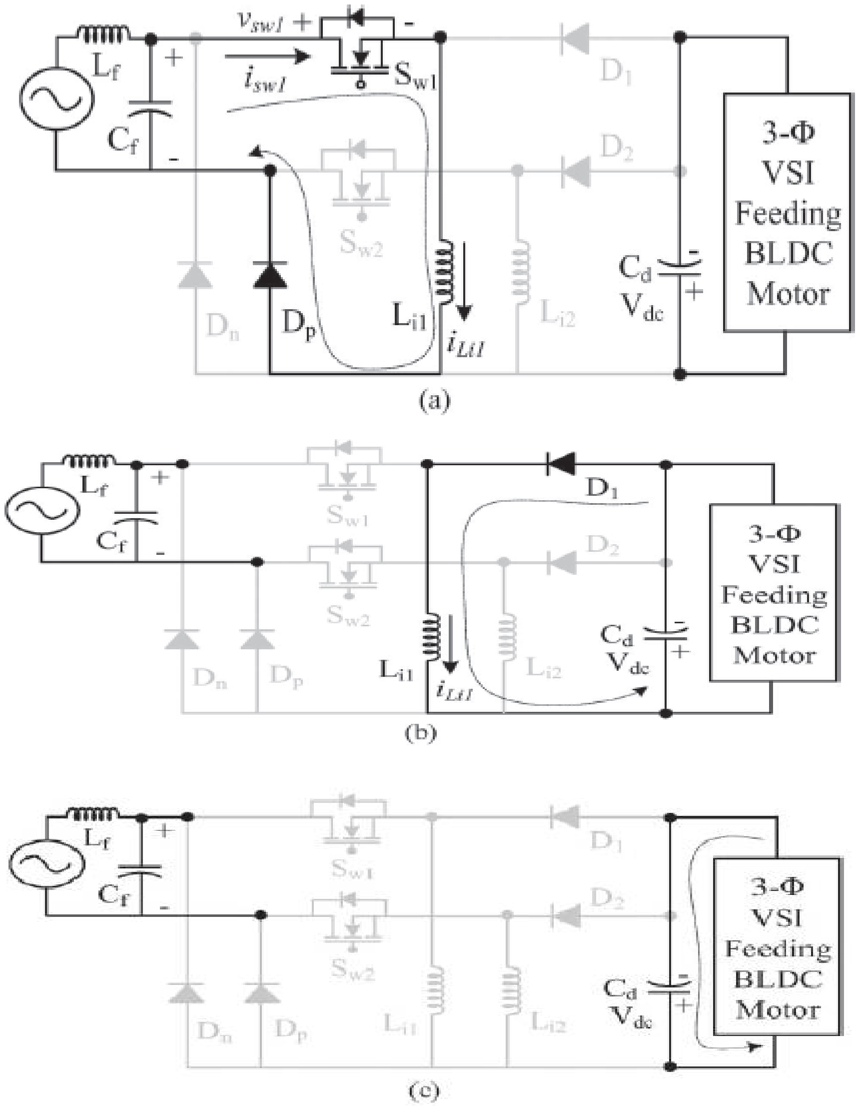

Fig. 2. Operation of the proposed converter in different modes (a)–(c) for a positive half cycle of supply voltage and (d) the associated waveforms. (a) Mode I. (b) Mode II. (c) Mode III. (d) Waveforms for positive and negative half cycles of supply voltage.

IV.DESIGN OF PFC BL BUCK–BOOST CONVERTER

A PFC BL buck–boost converter is designed to operate in DCM such that the current in inductors Li1 and Li2 becomes discontinuous in a switching period. For a BLDC of power rating 251 W (complete specifications of the BLDC motor are given in the Appendix), a power converter of 350 W (Po) is designed. For a supply voltage with an rms value of 220 V, the average voltage appearing at the input side is given as

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$V_{in} = \frac{2\sqrt{2}\,V_s}{\pi} \approx 198V$................ (1)

The relation governing the voltage conversion ratio for a buck–boost converter is given as

$d = \frac{V_{dc}}{V_{dc}+V_{in}}$ .... (2)

The proposed converter is designed for dc link voltage control from 50 V (*V*dc min value hence the minimum duty ratio (*d*min) corresponding to *V*dc min calculated as 0.2016 respectively.

A. *Design of Input Inductors (Li*1 *and Li*2*)*

The value of inductance *L*ic1, to operate in critical conduction mode in the buck–boost converter, is given as

$L_{ic1} = \frac{R(1-d)^2}{2f_s}$..................................... (3)

where *R* is the equivalent load resistance, *d* is the duty ratio, and *fs* is the switching frequency. Now, the value of *L*ic1 is calculated at the worst duty ratio of *d*min such that the converter operates in DCM even at very low duty ratio.. Hence, from (4), the value of inductance *L*ic min corresponding to *V*dc min is calculated as

$L_{ic1} = \frac{V^2 dc\min*(1-d)^2}{P_{min}*2f_s} = \frac{50^2}{90}\frac{(1-0.2016)^{\;\;2}}{2*20000} = 442.67\mu H.$ (5)

The values of inductances *Li*1 and *Li*2 are taken less than 1/10th of the minimum critical value of inductance to ensure a deep DCM condition [24]. The analysis of supply current at minimum duty ratio (i.e., supply voltage as 220 V and dc link voltage as 50 V) is carried out for different values of the inductor (*Li*1 and *Li*2).

B. *Design of DC Link Capacitor* (*Cd*)

The design of the dc link capacitor is governed by the amount of the second-order harmonic (lowest) current flowing in the capacitor and is derived as follows. For the PFC operation, the supply current (*is*) is in phase with the supply voltage (*vs*). Hence, the input power *P*in is given as

$$P_{in} = \sqrt{2}V_s \sin\omega t * \sqrt{2}I_s \sin\omega t = V_s I_s(1-\cos 2\omega t)$$

where the latter term corresponds to the second-order harmonic, which is reflected in the dc link capacitor as

$i_c(t) = \frac{V_s I_s}{V_{dc}}\cos 2\omega t$ .... (7)

The dc link voltage ripple corresponding to this capacitor current is given as

$\Delta V_{dc} = \frac{I_d}{2\omega C_d}\sin 2\omega t$................ (8)

For a maximum value of voltage ripple at the dc link capacitor, Sin(ωt) is taken as 1. Hence, (8) is rewritten as

$C_d = \frac{I_d}{2\omega\Delta V_{dc}}$...................... (9)

Now, the value of the dc link capacitor is calculated for the designed value *V*dc des with permitted ripple in the dc link voltage (Δ*V*dc) taken as 3% as

$$C_d = \frac{I_d}{2\omega\Delta V_{dc}} = 1857.7\mu F \approx 2200\mu F$$

Hence, the nearest possible value of dc link capacitor *Cd* is selected as 2200 μF.

V.SIMULATED PERFORMANCE OF PROPOSED BLDC MOTOR DRIVE

The performance of the proposed BLDC motor drive is simulated in MATLAB/Simulink environment using the Sim-Power-System toolbox. The performance evaluation of the proposed drive is categorized in terms of the performance of the BLDC motor and BL buck–boost converter and the achieved power quality indices obtained at ac mains. The parameters associated with the BLDC motor such as speed (N), electromagnetic torque (*Te*), andstator current (*ia*) are analyzed for the proper functioning of the BLDC motor. Parameters such as supply voltage (*Vs*), supply current (*is*), dc link voltage (*V*dc), inductor's currents (*i*Li1, *i*Li2), switch voltages (*V*sw1, *V*sw2), and switch currents (*i*sw1, *i*sw2) of the PFC BL buck–boost converter are evaluated to demonstrate its proper functioning**.**

C. *Steady-State Performance*

The steady-state behavior of the conventional and proposed BLDC motor drive for two cycles of supply voltage at rated condition (rated dc link voltage of 200 V) is shown in Fig. 5,6,7. The discontinuous inductor currents (*i*Li1 and *i*Li2) are obtained, confirming the DICM operation of the BL buck–boost converter. The harmonic spectra of the supply current at rated and light load conditions, i.e., dc link voltages of 50 V, are also shown in Fig. 8,9,10.

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respectively, which shows that the THD of supply current obtained in proposed and conventional scheme with PFC is under the acceptable limits of IEC 61000-3-2.

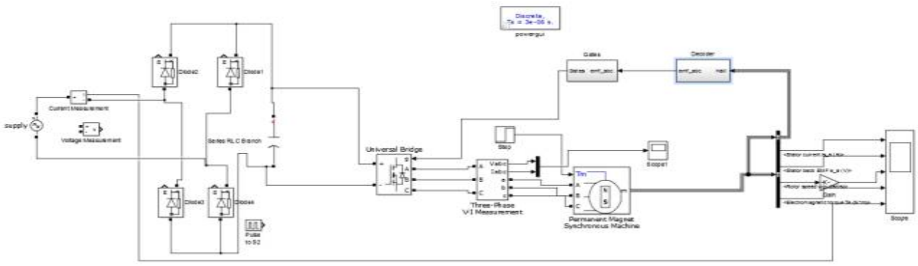

Figure 5: conventional drive without PFC

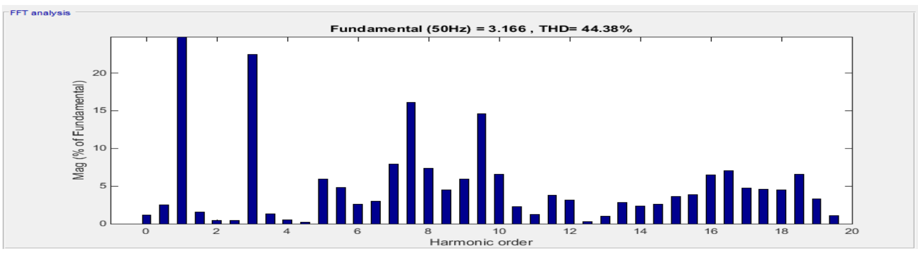

Figure 7: Total Harmonic spectra of conventional drive without PFC

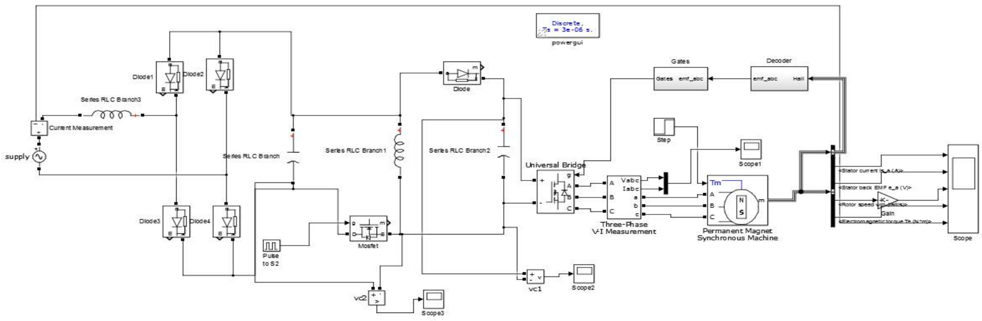

Figure 8: Conventional drive with buck boost PFC fed BLDC motor

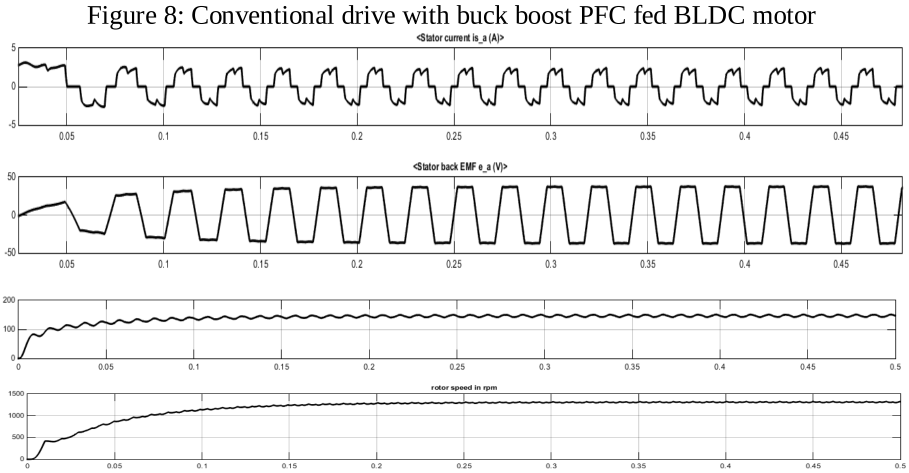

Figure 9: different parameters of the conventional drive with buck boost PFC fed BLDC motor drive

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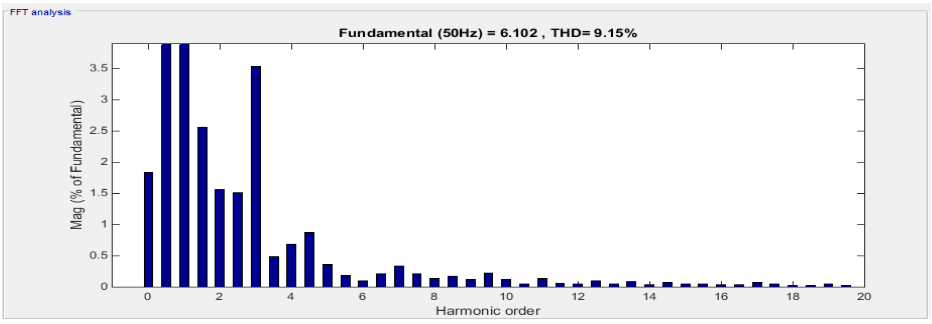

Figure 10: total harmonic distortion of conventional drive with buck boost PFC fed BLDC motor drive

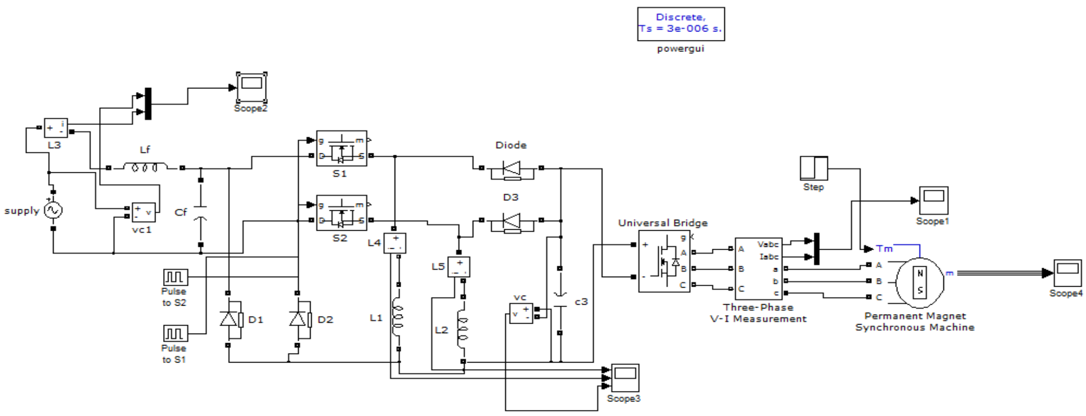

Figure 11: Proposed BLDC motor drive with front-end BL buck–boost converter

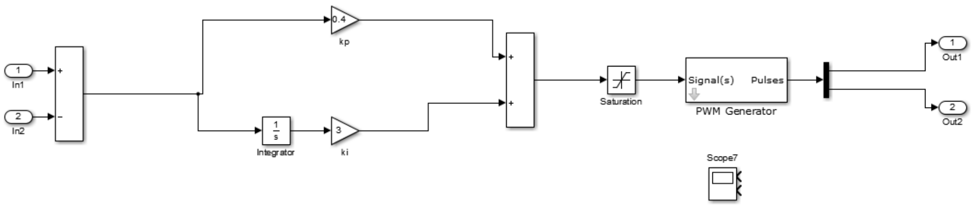

Figure 12: Control subsystem of Front-End PFC Converter

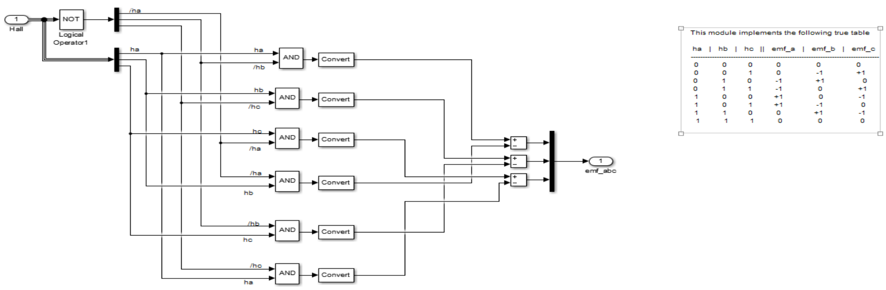

Figure 13: subsystem of hall sensor signal generation.

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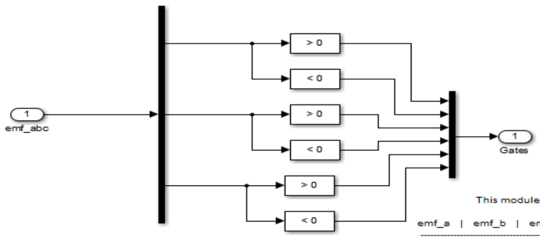

emf_a	emf_b	emf_c	Q1	Q2	Q3	Q4	Q5	Q6
0	0	0	0	0	0	0	0	0
0	-1	+1	0	0	0	1	1	0
-1	+1	0	0	1	1	0	0	0
-1	0	+1	0	1	0	0	1	0
+1	0	-1	1	0	0	0	0	1
+1	-1	0	1	0	0	1	0	0
0	+1	-1	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0

Figure 14: switching states for achieving electronic commutation of bldc motor based on hall-effect position signals

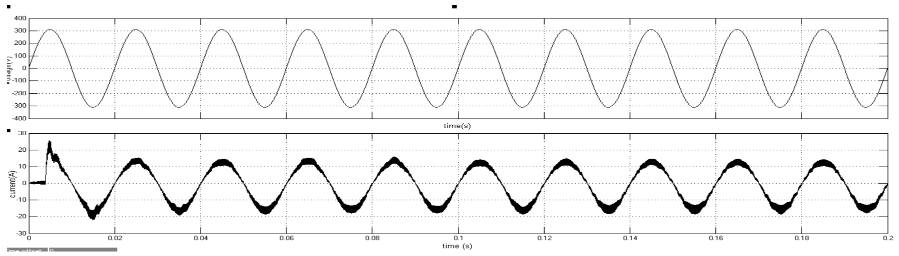

Figure 15: simulation results of input voltage and current

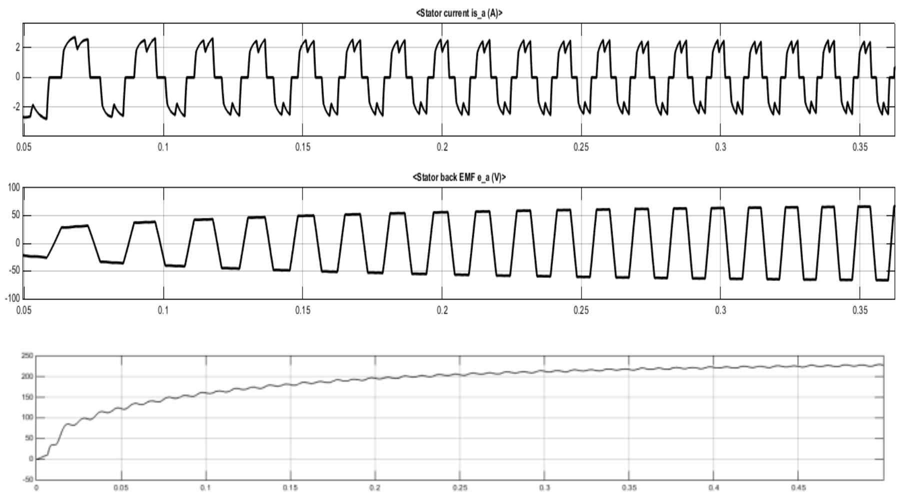

Figure 17: different parameters obtained for the proposed buck boost PFC fed BLDC motor drive.

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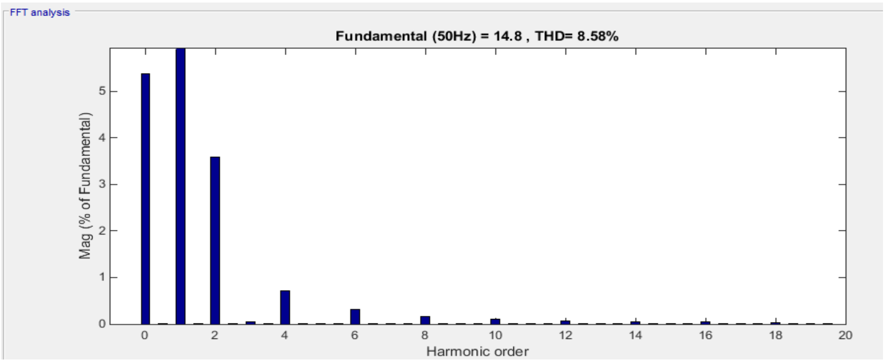

Figure 18: total harmonic distortion spectra obtained for the proposed drive

VI.CONCLUSION

A PFC BL buck–boost converter-based VSI-fed BLDC motor drive has been proposed targeting low power applications. A new method of speed control has been utilized by controlling the voltage at dc bus and operating the VSI at fundamental frequency for the electronic commutation of the BLDC motor for reducing the switching losses in VSI. The front-end BL buck–boost converter has been operated in DCM for achieving an inherent power factor correction at ac mains. A satisfactory performance has been achieved for speed control with power quality indices within the acceptable limits of IEC 61000-3-2. A comparative analysis of the proposed BL buck–boost converter-fed BLDC motor drive is carried out with conventional schemes.

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