ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Special Issue 8, November 2016

Synchronization of Grid Voltage under Symmetrical and Asymmetrical Faults for a Distributed System Using DDSRF-PLL Technique

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ABSTRACT: Power distribution systems are requiring more generating power and we also need to increase the renewable energy power generations, for this reason Wind and PV systems are mainly used in the distribution systems. Transmission system operators are facing low voltage problem for wind and solar connected lines, to reduce these problems STATCOM and DVR systems are normally used. These systems will compensate the fault conditions and low or higher voltage conditions, even though they are not giving the satisfied results. It take some time get the grid synchronization. To achieve fast and accurate grid synchronization results advanced algorithms are developed. To fulfill this scenario this paper analyzes the synchronization capability of three advanced synchronization systems: the decoupled double synchronous reference frame phase-locked loop (PLL), the dual second order generalized integrator PLL, and the three-phase enhanced PLL, designed to work under such conditions. Although other systems based on frequency-locked loops have also been developed, PLLs have been chosen due to their link with dq0 controllers.

KEYWORDS: STATCOM; Phase Locked Loop (PLL); Grid voltage synchronization; DDSRF-PLL; DSOGI-PLL; 3phEPLL; frequency change;

I. INTRODUCTION

In the actual grid codes needs (GCR) bound constrains for the operation of alternative energy plants lower grid voltage fault conditions, have advance an excellent importance. These needs verify the fault boundaries with those a grid connected turbine shall continue connected to the network, giving rise to specific voltage profiles that specify the depth and clearing time of the voltage sags that wind turbines should stand up to while not tripping. Like concern square measure referred to as Fault Ride Through (FRT) or Low Voltage Ride Through (LVRT) and that they square measure represented by a voltage vs time characteristic, denoting the negligible needed immunity of the alternative energy station [7].

Although the LVRT needs within the totally different |completely different} standards might be terribly different, as shown in [8], the primary issue that alternative energy systems would like afford once a voltage sag happens is that the condition of their transient response, so as to avoid its careful disconnection from the network. this can be the case, for example, of fastened speed WTs supported coop induction generators (SCIG), Spot the voltage drip within the mechanical device windings will conduct the generator to associate degree over speed tripping, as shown in [9]. Likewise, versatile speed WTs supported doubly fed induction generators (DFIG) might loose the manageable within the dose of active/reactive power owing to the division of the rotor aspect device lower such conditions [10]-[11]. finding supported the event of auxiliary systems like as STATCOMs and DVRs get contend a decisive role for raise the FRT capability of SCIGs WTs, as exhibit in [12]-[16Likewise, leading management helpful for the ability converters of wind generation potency are additionally projected for reducing over currents in DFIGs lower these conditions in [10]-[11] and [17]-[18]. In any case a quick notice the fault contributes to enhance the results of those things, and as a consequence the FRT capability of the system. Phase-locked technology dated principally employed in communications, part and user natural philosophy systems wherever a neighborhood generator is synchronal with some external signal. In power systems, the Synchronous frame of reference PLL (SRF-PLL) is that the principally extended

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technique for synchronizing with three-phase systems [30]. Though, and despite the very fact that the performance of SRF-PLL is satisfactory lower balanced conditions, its response may be inadequate lower unbalanced, faulty or coloured conditions [31]-[33].

In this paper 3 leading grid synchronization systems: the Decoupled Double synchronous frame of reference PLL (DDSRF PLL) [34], the twin SOGI PLL (DSOGI PLL) [35] and therefore the 3 part increased PLL (3phEPLL PLL) [36] are studied. The study can calculate their performance and accuracy on the amplitude and part notice the positive sequence of the voltage, lower unbalanced and distorted location, that, so as to achieve a a lot of realistic approach, gain resolve in line with experimental grid fault patterns get from [37] -[38]. within the following sections the assorted illustration of every PLL are careful (§IV), later a quick description of the various structures (§III).

II.GRID SYNCHRONIZATION SPECIFICATIONS BASED ON GCR

Even though several works are published within the field of grid synchronization, almost all of them are centered on analyzing the individual energetic performance of each proposal, without first determining a time response window within the energetic behavior of the system under test, which would be considered to be satisfactory. In this paper, in order to evaluate the response of the grid synchronization topologies under test, a familiar performance requirement for all the structures has been established in this section, considering the needs that can be derivational from the LVRT requirements. Despite the fact that the detection of the fault can be carried out with plain algorithms, as shown in [39] and [40], the importance of advanced grid synchronization systems lies in the requirements of having accurate information about the magnitude and phase of the grid voltage during the fault, in order to inject the reactive power enforcd by the TSO. In the German standard [2], it is stated that voltage control need take place within 20 ms after the fault recognition, by providing a reactive current on the low voltage side of the generator transformer to at least 2%of the rated current for each percent of the voltage dip, as shown in Fig. 1. 100% reactive power delivery need be possible, if necessary. A similar condition is given in the Spanish grid code, where the wind power plants are required to block drawing inductive reactive power within 100 ms of a voltage drop and be easy to inject full reactive power after 150 ms, as shown in Fig. 2.Considering these demands, this paper will consider that the evaluation of the voltage conditions will be carried out within 20–25 ms, as this target permits it to fulfill the most restrictive requirements, in terms of dynamical response, available in the grid codes. This action will be extended to frequency estimation; although this parameter is more related to secondary control algorithms than LVRT, the same time window among 20 and 25 ms will be considered in this work for the detection of the disturbance.

III.DESCRIPTION OF THE THREE SYNCHRONIZATION SYSTEMS

Many of the positive-sequence detection algorithms are based on SRF PLLs [32]. Despite having a great response lower balanced conditions, their performance becomes insufficient in unbalanced faulty grids (95% of cases), and their great operation is highly conditioned to the frequency stability, which is unsuitable with the idea of a robust synchronization system. Many authors have discussed different advanced models, which are easy to overcome the problems of the classical PLL, using frequency and amplitude adaptive structures which are easy to deal with unbalanced, faulty, and harmonic-polluted grids. In the framework of these topologies, three PLL structures will be discussed and calculate in this paper.

A. DDSRF PLL

The DDSRF PLL, published in [34] and [41], was developed for developing the conventional SRF PLL. This synchronization system exploits two synchronous reference frames rotating at the major utility frequency, one counter clockwise and another one clockwise, in order to achieve an accurate expose of the positive- and negative-sequence segments of the grid voltage vector when it is affected by unbalanced grid faults. The design of the DDSRF PLL is shown in Fig. 3.

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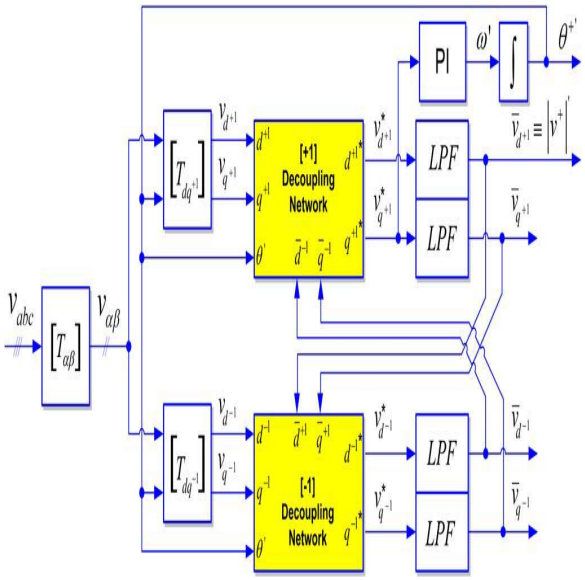

Fig 3.1 DDSRF PLL Algorithm

B. DSOGI PLL

The operating principle of the DSOGI PLL for supposing the positive- and negative-sequence segments of the grid voltage vectors is based on using the instantaneous symmetrical component (ISC) method on the $\alpha\beta$ stationary reference frame, as explained in [35]. The diagram of the DSOGI PLL is shown in Fig. 4. As it might be noticed, the ISC method is implemented by the positive-sequence calculation block.

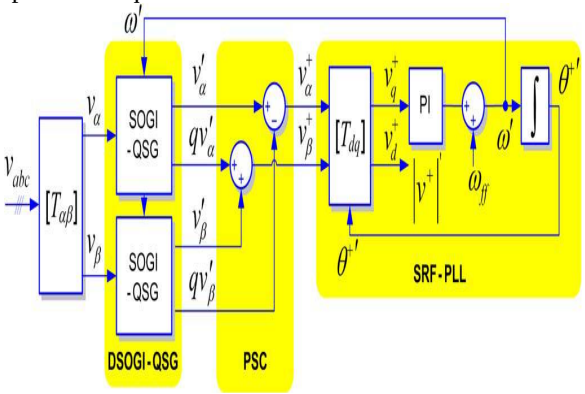

Fig 3.2 DSOGI PLL algorithm

C. 3PHEPLL

The enhanced phase-locked loop (EPLL) is a synchronization system that has proven to provide good results in single phase synchronization systems [43]. An EPLL is actually an adaptive band pass filter, which is able to adjust the cutoff frequency as a function of the input signal. Its structure was later adapted for the three-phase case [44], in order to catch the positive-sequence vector of three-phase signals, obtaining the 3phEPLL that is represented in Fig. 5.

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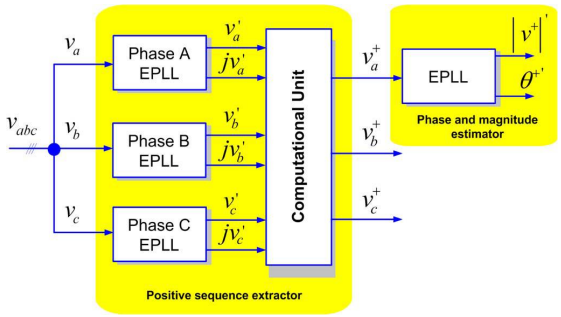

Fig 3.3 3PHE PLL algorithm

IV. SIMULATION RESULTS

The different PLL algorithms have been implemented in a control board based on a floating-point Texas Instruments TMS320F28335 DSP at 150 MHz (6.67-ns cycle time). Their capability to perform a fast and accurate synchronization has been tested in the laboratory under different grid fault scenarios, where the three-phase voltage waveforms experience transients due to the arrival of voltage sags, frequency variations, and harmonic pollution.

Fig 4.1 shows the overall circuit and control designs of the system. It contains source to load circuit.

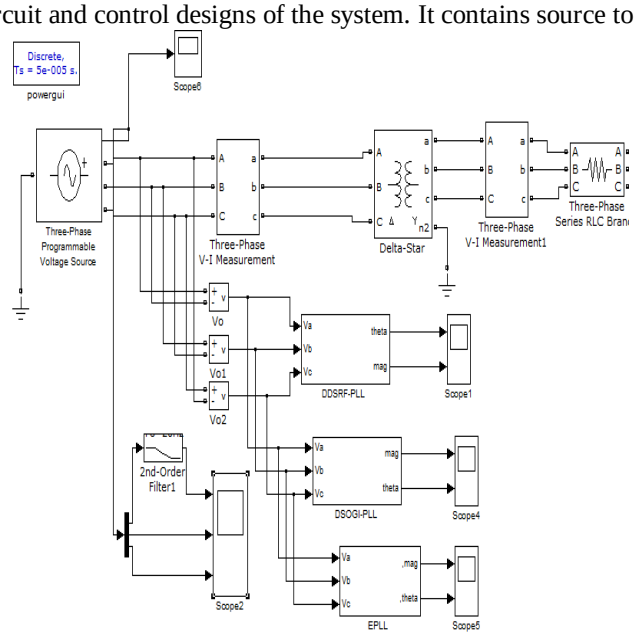

Fig 4.1 Overall simulation circuit

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Magnitude ad theta

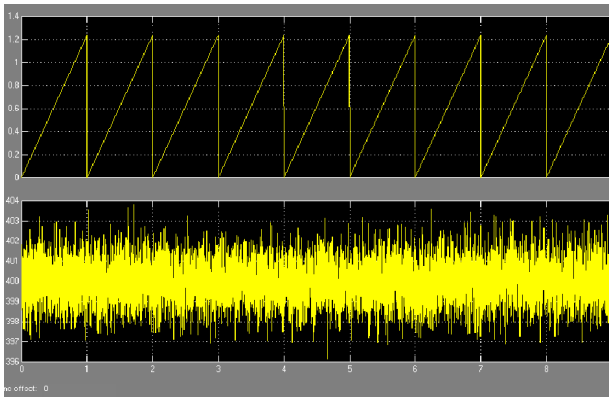

Fig 4.2 Magnitude and theta values

Fig 4.2 shows the Magnitude and theta value of the feedback voltage. By using this feedback voltage control systems are designed and voltage synchronization is achieved

A. POLLUTED SOURCE VOLTAGE

From fig 4.3 it is understand about the source voltage which is get polluted by the fault. Simulation result shows the three phase voltage signals with pollution.

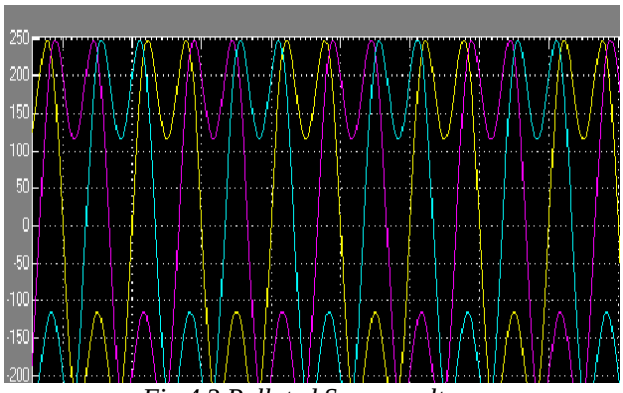

Fig 4.3 Polluted Source voltage

B. FILTERED VOLTAGE

Filtered voltage is displayed in the fig 4.4. This simulation results display the single phase voltage signal.

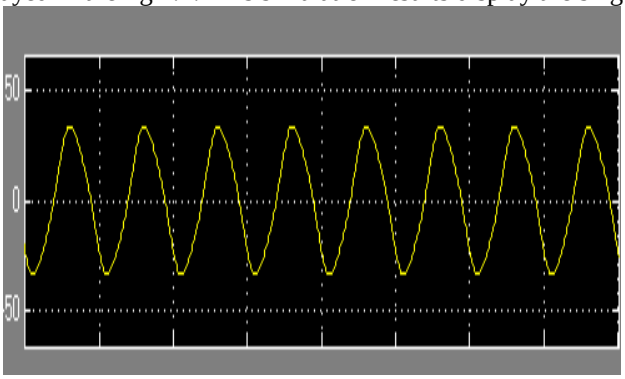

Fig 4.4 Filtered voltage

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C. TOTAL HARMONIC DISTORTION

Total Harmonic Distortion (THD) value is shown in the fig 4.5. The value of the THD is 6.27%, which means the system have more THD during the fault condition and now it is limited by using filter circuit.

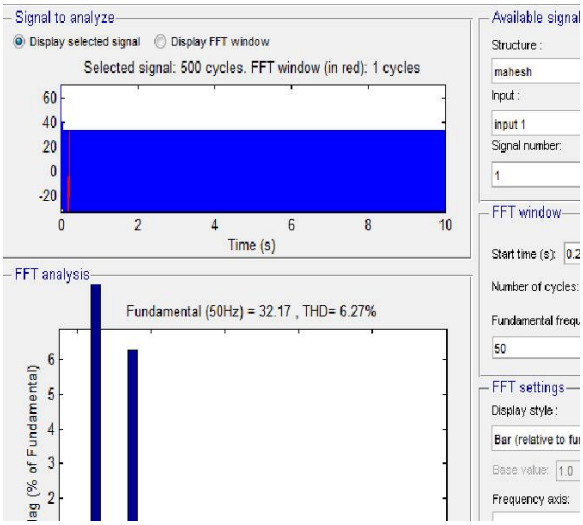

Fig 4.5 THD value of the voltage

V. CONCLUSION

This paper studied the behavior of three advanced grid synchronization systems. Their structures have been presented, and their discrete algorithms have been detailed. Moreover, their performances have been tested in an experimental setup, where these algorithms have been digitally implemented in a commercial DSP, allowing proof of their satisfactory response under balanced and distorted grid conditions.

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