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Design of High Frequency 16/17 Dual Modulus Prescaler Using TSPC Flip Flop

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ABSTRACT: A high speed and high frequency CMOS TSPC based divide-by-16/17 dual modulus prescaler is proposed. Dual-modulus prescaler is implemented without using any extra logic gates by exploiting the special feature of the TSPC flip-flop. The speed of the prescaler is improved in two aspects. First, by adopting a new pseudo divide-by-2/3 prescaler, the minimum working period is effectively reduced by half a NOR gates delay. Second, by changing the connection of TSPC D-Flip-Flops, the minimum working period is further reduced by half an inverters delay. Designed in 180-nm CMOS process, the proposed circuit is capable of operating up to 6.5 GHz. The power consumption is 3.25 mW at the maximum operating frequency under 1.6 V supply voltage.

KEYWORDS: Dual modulus, Prescaler, Divide-by 2/3,TSPC

I.INTRODUCTION

The rapid evolution of the communications industry has increased the demand for low cost, low power and wide bandwidth RF circuits. Today's technologies make possible powerful computing devices with multi-media capabilities. Consumer's attitudes are gearing towards better mobilityandaccessibility. This caused a demand for an ever-increasing number of portable applications requiring low-power and high throughput.Intensive efforts are made to develop RF circuitsoperating at GHz range using low-cost CMOS process. Low power consumption is required to increase the battery life time and to reduce the operating temperature.

Frequency dividers,also known as prescalers are used in many communications applicationssuch as frequency synthesizers, timing-recovery circuits and clock generation circuits. It is one of the most critical block in the frequency synthesizer because it operates at the highest frequency and consumes large power. Thus the power reduction in the first stage of the prescaler is important in realizing a low power frequency synthesizer.High speed dual-modulus frequency prescalers have an important role in phase-locked loop (PLL) designs too[1] - [4].They allow multiple division ratios using a single divider. Power consumption,speed and maximum operating frequency are the major factors to be considered while designing a dual modulus prescaler.

II.RELATED WORK

Several techniques are available for frequency prescalers such as current mode logic(CML) [2], inject locking prescaler,true single phase clocked logic (TSPC) etc. Even though current-mode logic and inject locking prescaler can provide working frequency of hundreds/tens GHz with process of SoI CMOS or InP DHBTs and so on, TSPC dual-modulus prescaler is commonly utilized in several GHz with standard CMOS process [3], [4]. CML consumes high power,hence it is used only for very high frequency applications where other topologies cannot work.TSPC has the merits of single clock phase, low power, small area, and large output swing. Speed improvement is an important design issue for TSPC prescaler. In the transistor level, forward body biasing technique can improve the speed by decreasing the threshold voltage of nMOS transistors [5], [6]. However, it suffers from high minimum working frequency as well as increased cost and decreased robustness. In the gate level, adopting extended- TSPC flipflops can effectively improve the operating speed [5]. But the current leakage is serious, thus the minimum working frequency performance is limited. In the RTL level, enhance the speed of divide-by-16/17 prescaler [7], [8]. However, in these papers, several

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design rules of TSPC circuits are broken. It leads to shrinking frequency range because these prescalers are no longer suitable for low frequency operation.

Today both the divide-by-2/3 and divide-by-4/5 prescaler are most widely utilized. Usually, divide-by-2/3 prescaler has the advantage of speed more than divide-by-4/5 and these prescaler is more power efficient too. Thus, divide-by- 2/3 prescaler is preferred in 16/17 prescalers. On the other hand, divide by 4/5 prescaler is preferred in applicationswhere large division ratio is required, such as 128/129 prescalers and it helps to minimize the critical path.

In this brief, two aspects can improves the maximum working frequency of the divide-by-16/17 prescaler. First, develop a new pseudo divide-by-2/3 prescaler and adoptedinto the divide-by-16/17 prescaler, which leads to reduce the minimum working period by half a NOR gates delay. Second, the minimum working period is further reduced by half an inverters delay, by changing the connection of efficient TSPC D-flip-flops (DFFs).

III. TSPC D FLIP FLOP

D-flipflop is the data flip flop transfers the data withoutany flipping.A high-speed TSPC DFF proposed is shown in Fig. 1, where clock-controlled transistors are placed close to a power supply line to increase switching speed.The setup time of the TSPC DFF can be written as

$t_{setup} = t_{D\text{-}S}$

Where $t_{D\text{-}S}$means the propagation time from node D to node S, which is a clocked inverters delay. The propagation delay of the TSPC DFF can be written as

$t_{D\text{-}Qn} = t_{S\text{-}T} + t_{T\text{-}Qn}$

Where $t_{D\text{-}Qn}$ is the propagation delay from CLK to Qn. $t_{S\text{-}T}$ and $t_{T\text{-}Qn}$ represents the propagation delay from node S to T, T to Qn respectively. One inverter stage is required at node Qn to get the correct Q output.

An advantage of TSPC circuits is that AND/OR logic gates can be absorbed into the first stage of TSPC DFFs and the logic depth can be reduced [9]. After AND/OR gate absorption, the first stage of the TSPC DFFs will become a clocked NAND/NOR gate. The logic depth can be reduced by about two inverters delay after absorption.

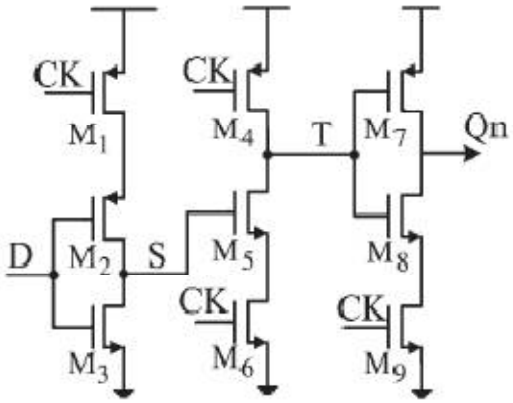

Figure 1: Structure of TSPC DFF.

IV. CONVENTIONAL DIVIDE-BY-16/17DUAL-MODULUS PRESCALER

Fig.2 shows the schematic of a conventional divide by16/17 prescaler. It is designed based on a divideby- 2/3 prescaler. It consists of a divide-by-2/3 prescaler, an asynchronous divide by 8 counter, four input NAND gate and a two OR gates. It has two critical paths. First, critical path #1(Q1 path) comes through D-FF1and OR1. Second, critical path #2(MC1 path) comes through DFF1, DFF2, NAND AND OR1.

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Within a period of Fin, signal must pass path #1 while within a periods of Fin it should pass path #2.theoritically, it is critical to identify which path decides the minimum working period. But the result varies in different designs. In conventional divide by 16/17 prescaler there is a trade-off between lengths of the two critical paths. The optimized design is to make the length of critical path #1 approximately equal to half length of critical path #2. In conventional divide-by-16/17 prescaler, In front of DFF0 two logic gates (NAND and OR1) are located. In addition, there are two critical paths. Apparently, it is not the optimized design.To achieve a high speed both the critical paths should be optimized, which is a great challenge for designers.

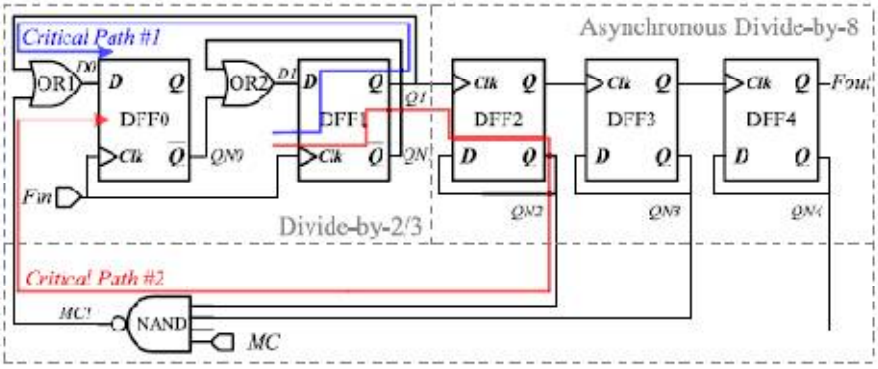

Fig.2: Schematic of conventional divide-by-16/17 prescaler.

V. PROPOSED DIVIDE-BY-16/17 DAUL MODULUS PRESCALER

Function of three branches of TSPC flip flop shown inFig.1 is as follows. The first branch samples input data when CK = 0 (negative cycle) and holds the data when CK = 1 (positive cycle), the second branch precharges node T during the negative clock cycle and evaluates the data during the positive cycle, and the third one passes the evaluated data during the positive cycle and holds the output during the negative cycle. Therefore, the evaluation result in the second branch decides the output of the DFF. When the input is high, the charge on the node T holds, and output Qn goes low immediately after the clock rises high. On the other hand, when the input is low, the node T has to be discharged before Qn goes high, which inherently limits the speed of TSPC operation. Since the second branch works as a domino logic, adding a transistor to the node T creates a NOR logic gate that can change the output value without passing through the first branch. We exploit this behavior to design high-speed dual-modulus prescalers.

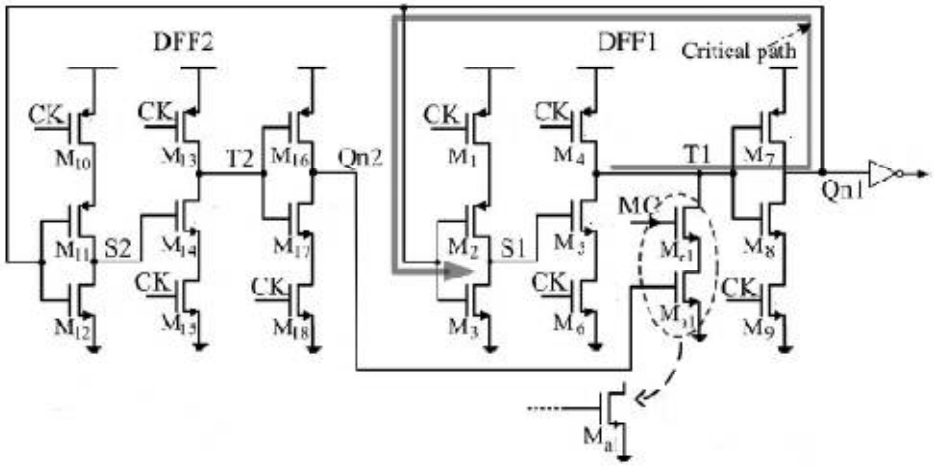

Fig.3: Proposed high-speed 2/3 frequency prescaler.

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Fig. 3 shows a new 2/3 prescaler by adding NOR gate to node T. Here the separated logic gates in conventional design are removed, and the two transistors Ma1 and Mc1 are added to implement a NOR gate at the node T1. When set to a divide-by-2 mode, the control signal MC is low, and the added transistors do not affect the behavior of the node T1, except for adding a small capacitive load. When MC goes high, the path from the output of the DFF2 to the node T1 is enabled. Once Qn2 goes high, the added path forces T1 to logic low and extends the high level of the output Qn1; therefore, the division ratio becomes 3.

In divide by 2 operation, the circuit is identical to asingle TSPC flip flop except a small parasitic capacitance at node T.Hence the operating speed is closer to that of a single TSPC flip flop. During divide by 3 operation, since Qn2 skip first branches in DFF1 and forces node Qn1 to low directly,operating speed is even faster than divide by 2 operation.

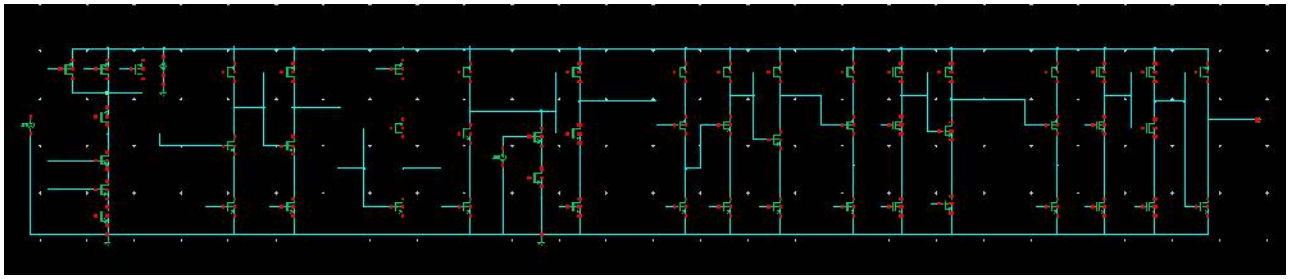

Fig.4: Schematic of proposed 16/17 prescaler.

This 2/3 prescaler is used to implement 16/17 prescaler. Schematic of 16/17 dual modulus prescaler using the above 2/3 prescaler is shown in Fig.4. The operation mode of proposed circuit is as follows. When MC = 1, MC1 changes its value according to (QN2, QN3, QN4). The pseudo divideby- 2/3 prescaler controlled by MC1 accomplishes seven times of divide-by-2 operations and one time of divide-by-3 operation in a cycle. The whole circuit operates in divideby- 17 mode. When MC = 0, MC1 keeps low and the pseudo divide-by-2/3 prescaler keeps on divide-by-2 operation. The whole circuit works in divide-by-16 mode.

VI. MEASUREMENT RESULTS

The proposed divide-by-16/17 prescaler is designed in 180 nm CMOS technology. Output waveform of 16/17 prescaler is shown in Fig.5. Measurement results show thatthe proposed circuit achieves a maximum working frequency of 6.5 GHz under 1.6 V supply voltage.

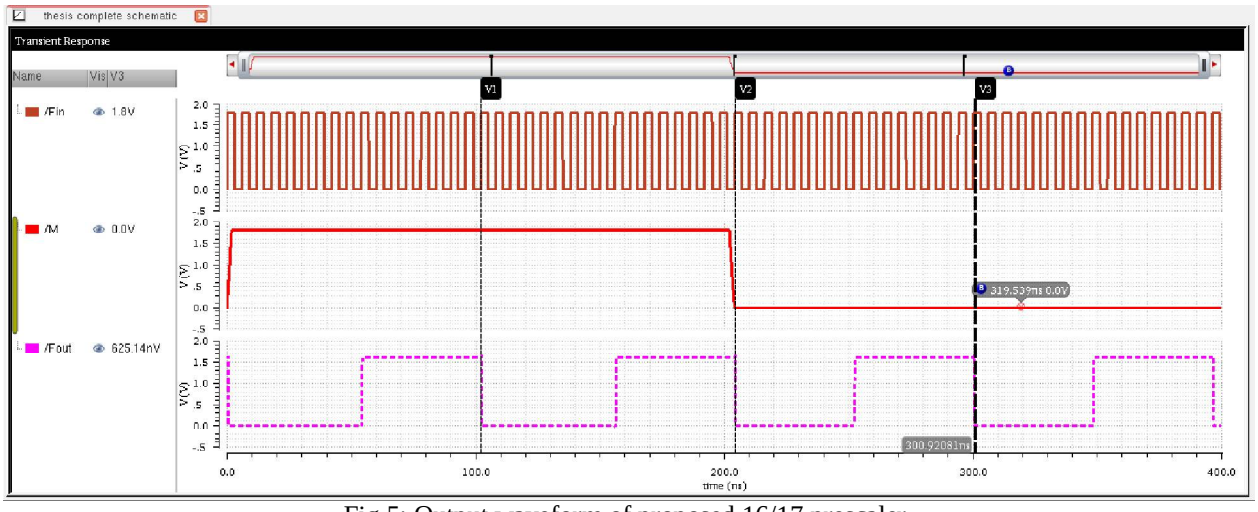

Fig.5: Output waveform of proposed 16/17 prescaler.

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Table I shows the comparison of conventional 16/17 prescaler with the proposed prescaler. Power, delay and number of transistors are less for the proposed design.

	Cnventional	Proposed
Frequency(GHz)	4	6.5
Power(mW)	4.5	3.25
Delay(ps)	150	68
No.of Transistors	71	55
Power Supply(V)	1.6	1.6

Table I: Comparison of proposed circuits with conventional system

Fig. 6 shows the frequency Vs power graph of conventional prescalerand the proposed prescalers. Power increases linearly with input frequency and reaches 3.25mW at maximum working frequency (6.5 GHz) and for conventional design it is 4.5 mW.

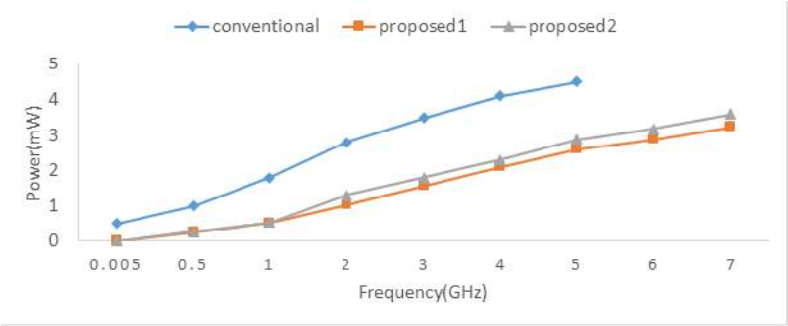

Fig.6: Frequency Vs Power consumption.

Layout of the proposed 16/17 prescaler is shown in Fig.7.

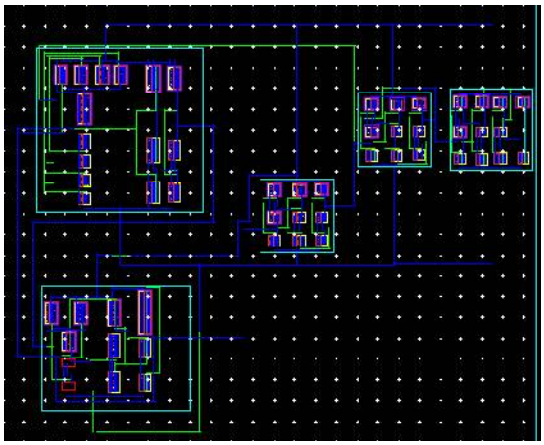

Fig.7: Layout of proposed 16/17 prescaler.

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VII.CONCLUSION

This brief presents a novel high speed TSPC divide-by- 16/17 dual modulus prescaler. The proposed circuit reduces and power and increases the speed of operation which inturn increases the maximum operating frequency. The speedof prescaler is improved in two aspects. First is by adopting a new pseudo divide-by-2/3 prescaler. Second is by changing the connection of TSPC D-Flip-flops, i.e., by avoiding the fourth stage in TSPC flip flop, the minimum working period is reduced by half an inverters delay. Designed in 0.18um CMOS technology, the proposed circuit achieves a 6.5 GHz maximum working frequency.

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