

ISSN (Print) : 2320 – 3765 ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization) Vol. 5, Issue 10, October 2016

5-Step and 6-Step Nested-Current-Mirror Rail-to-Rail Output Single-Stage Amplifier with Enhancements of DC Gain, GBW and Slew Rate

Geethumol K K¹, Premanand B²

PG Scholar [VLSI & ES], Dept. of ECE, Government Engineering College, Idukki, Kerala, India¹

Assistant Professor, Dept. of ECE, Government Engineering College, Idukki, Kerala, India²

ABSTRACT: For better performance, rail-to-rail output single-stage amplifiers are a potential replacement of their multi-stage counterparts, especially for display applications that entail massive buffer amplifiers in their column drivers. This paper describes a nested-current-mirror (NCM) technique for a single-stage amplifier to achieve high DC gain, gain-bandwidth product (GBW) and slew rate (SR). NCM technology is customizable for different mirror steps, and sub mirror ratios, to balance the performance metrics while preserving a rail-to-rail output swing. NCM amplifier can mitigate the fundamental power-efficiency limit set by the basic differential-pair (DP) amplifier. Two prototypes, 5-step and 6-step NCM amplifiers, were designed and analyzed in 0.18 μ m CMOS for systematic comparison with the 3-step and 4-step NCM amplifier. 5-step NCM can provide 91 dB DC gain and 0.137–0.424 MHz GBW over 0.25 – 1 nF with >70^o phase margin (PM). 6-step NCM design attaining 98 dB DC gain and 0.397–0.841 MHz GBW over 0.45– 1 nF with >75^o PM.

KEYWORDS: DC gain, GBW, slew rate, nested current mirror, effective transconductance(G_{M,eff}), mirror factor(K)

I.INTRODUCTION

Low-temperature polysilicon (LTPS) LCD panels consist of thousands of buffer amplifiers in their column drivers. The area and power budgets of each buffer amplifier are very important because these factors determine the market pressure on cost and display quality [1]. Now-a-days multi-stage amplifiers dominate those applications owing to their key advantages of high DC gain and rail-to-rail output swing. Classical single-stage amplifiers were not commonly used in such application due to their limited capability in most metrics. So it is beneficial to revisit the fundamental limits of single-stage amplifiers and find a solution.

Most single-stage amplifiers suffer from a tight tradeoff between its power and performance. Telescopic amplifiers feature a GBW-to-power efficiency as high but sacrifice output swing. Folded cascode amplifiers partially surmount such swing limit, but at the expense of power. For LCD column drivers, current-mirror amplifiers are favored for their rail-to-rail output swing, and provide an extra design flexibility via adjusting the mirror ratio, K. A large K benefits most performance metrics (i.e., effective transconductance ($G_{M,eff}$), GBW and SR),but at the expense of noise and phase margin (PM). This paper introduces a nested-current-mirror (NCM) single-stage amplifier to advance its GBW-to-power/area efficiency and C_L drivability beyond the multi-stage designs, while preserving a rail-to-rail output swing. This nested-current-mirror (NCM) single stage amplifier can alleviate the tight performance tradeoffs in conventional single-stage amplifier topologies. Current-mirror factor K offers a freedom to leverage the various performance metrics such as effective transconductance, gain-bandwidth product and slew rate. The prototyped 5-step and 6-step NCM amplifiers achieve favorable performances with respect to 3-step and 4-step NCM amplifiers.

II. NCM SINGLE-STAGE AMPLIFIER SYSTEM MODEL

The basic principle of the NCM amplifier is to subdivide a current mirror into a number of pieces with different ratios, and sequentially combine their outputs to concurrently advance effective transconductance (Gm,eff) and output resistance (Rout) beyond those of the differential pair(DP) and current-mirror amplifiers. To attain high DC gain and GBW, more mirror stages and bigger ratios are preferred. To reduce the noise, the largest amount of current can be



(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 10, October 2016

allocated to the 1st mirror with a small K_1 . To increase SR, most of the current can be assigned to the second-last mirror with enlarged K_{N-1} and K_N . Indeed, the mirror stages and ratios of the NCM are only limited by the PM and transistor mismatches. Thus, the DC gain of the NCM can be as high as that of a folded-cascode amplifier, but without the output swing penalty. Moreover, unlike the folded-cascode and current-mirror amplifiers, cutting the current of the output stage does not essentially degrade SR.



Fig. 1.Development of the NCM amplifier from the current-mirror amplifier.

Figure 1 shows the development of NCM amplifier from current mirror amplifier. Here the biasing current I_{b1} is distributed to the left N divided differential pair(DP) transistors and these transistors are alternately connected to Vp and Vn. These DP transistors outputs are combined via N nested current mirrors with different mirror ratio. Since these DP transistors are located in the signal path all those transconductance are contributed to an effective transconductance $G_{M, eff}$. Correct selection of the mirror ratio have great influence on the performance matric.

The number of step is a design parameter. We show below 5-step and 6-step NCM design as they can provide appreciable gain, GBW and slew rate.

III. FIVE-STEP NCM AMPLIFIERS



Figure 2: Schematic of 5-step NCM

Figure 2 shows the schematic of a 5-step NCM amplifier. The DP transistors are split into M_1 to M_5 . Their outputs are summed via the NCM mirrors realized by M_6 to M_{15} . M_{16} collects the output of the left, to form the single-ended output together with M_{15} . To show how the mirror ratios K_1 to K_9 contribute to the effective transconductance ($G_{M,NCM5}$), GBW, DC gain and SR quantitative analyses are conducted, and they are valid for both single-ended output and differential output implementations.

$$G_{M,NCM5} = \frac{K_9 \times (2K_8 \left(\frac{K_7 + K_6}{K_7}\right) + 1)}{\sum_{I=1}^9 K_I + 1} \times g_{mp}$$
(1)



(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 10, October 2016

The $G_{M,NCM5}$ is mainly determined by the product of K_9 and $K_8 \times (K_7 + K_6)/K_7$ with a given sum of K_1 to K_9 . Since the product is readily sized to be much higher than the sum, $G_{M,NCM5}$ is significantly boosted. The DC gain of the 5-step NCM amplifier is expressed as the product of $G_{M,NCM5}$ and $R_{O,NCM5}$. In addition to $G_{M,NCM5}$ that already considerably improves its DC gain $R_{O,NCM5}$ is also enhanced over that of the DP amplifier, and can be represented by

$$R_{O,NCM5} = \frac{\sum_{I=1}^{9} K_I + 1}{K_9} \times r_{on} || r_{on}$$
⁽²⁾

The gain enhancement seen in $R_{O,NCM5}$ is attributed to substantial bias current reduction in the output stage in comparison with that of the DP amplifier. Thus, an overall DC gain enhancement over the DP amplifier can be observed. SR determines the amplifier's settling performance. Suppose a large negative step appears at Vp, it follows that the second-last mirror turns off. Consequently, almost all the current in M_5 is directed into M_{14} and amplified by the 5th mirror to discharge C_L . Similar analyses can be applied when there is a large positive input step occurring at Vp, resulting in a symmetric SR expressed by

$$SR_{NCM5} = \frac{K_9 \times (K_8 + 1)}{\sum_{l=1}^9 K_l + 1} \times \frac{2I_b}{C_L}$$
(3)

If numerator > denominator the SR of the proposed amplifier increases that of the DP amplifier, which can be realized by selecting relatively large K_8 and K_9 .

IV. DESIGN AND STABILITY ANALYSIS OF 5-STEP NCM

Design : Mirror factors (K) selected for the circuit design can be mention as $K_1 = 4$, $K_2 = 12$, $K_3 = 2$, $K_4 = 6$, $K_5 = 4$, $K_6 = 9$, $K_7 = 3$, $K_8 = 18$, $K_9 = 2$. For the 5-step NCM, the total bias current (3 μ A) is divided into 120 unit-current (Iu = 25 nA). To leverage the key metrics, the 1st mirror (M₆ to M₇) uses a small ratio of only 3 (K₁ = 4 and K₂ = 12). The 2nd mirror (M₈ to M₉) draws less current under a larger ratio of 3 (K₃ = 2 and K₄ = 6) to boost the DC gain and GBW, as they contribute less noise. Also, a larger K₈ enhances the SR. The 3rd mirror (M₁₀ to M₁₁) is assigned the ratio of 2 (K₅ = 4 and K₆ = 9). The 4th mirror (M₁₂ to M₁₃) is assigned the ratio of 6 (K₇ = 3 and K₈ = 18). The 5th mirror (M₁₄ to M₁₅) is assigned the ratio 2 (K₉ = 2) to benefit the SR and G_{M,NCM5}. Substituting these values into the DC gain, GBW and SR equation we can see that these are theoretically improved.



Figure 3: Block diagram of the proposed 5-step NCM amplifier



(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 10, October 2016

The equivalent small-signal diagram of the 4-step NCM amplifier is shown in Figure 3. G_{m1} , G_{m2} , G_{m3} , G_{m4} and G_{m5} are the transconductances of M_{1-5} respectively while Z_{b1} , Z_{b2} , Z_{b3} , Z_{b4} and Z_{b5} correspond to the input impedances of the 1st to 5th mirrors. The transconductances of the transistors in the five mirrors are respectively represented by G_{mb1-5} , while Z_{out} models the output impedance that includes C_L .

V. SIX-STEP NCM SINGLE-STAGE AMPLIFIER



Figure 4: The schematic of the 6-step NCM amplifier

Figure 4 shows the schematic of a 6-step NCM amplifier. The DP transistors are split into $M_1 - M_6$. Their outputs are summed via the NCM mirrors realized by $M_7 - M_{18}$. M_{19} collects the output of the left, to form the single-ended output together with M_{18} . To show how the mirror ratios K_1 to K_{11} contribute to the effective transconductance ($G_{M,NCM6}$), GBW, DC gain and SR quantitative analyses are conducted, and they are valid for both single-ended output and differential output implementations.

$$G_{M,NCM6} = \frac{K_{11} \times \left(2\left(\frac{K_{10} \times K_8 \times K_6}{K_7 \times K_9} + \frac{K_8 \times K_6}{K_9} + K_9\right) + 1\right)}{\sum_{l=1}^{l} K_l + 1} \times g_{mp}$$
(4)

Since the product is readily sized to be much higher than the sum, $G_{M,NCM6}$ is significantly boosted.

The DC gain of the 4-step NCM amplifier is expressed as the product of $G_{M,NCM6}$ and $Ro_{,NCM6}$. In addition to $G_{M,NCM6}$ that already considerably improves its DC gain, $Ro_{,NCM6}$ is also enhanced over that 3-step and 4-step NCM, and can be represented by

$$R_{O,NCM6} = \frac{\sum_{I=1}^{11} K_I + 1}{K_{11}} \times r_{on} || r_{on}$$
(5)

The gain enhancement seen in Ro_{,NCM6} is attributed to substantial bias current reduction in the output stage in comparison with that 3-step and 4-step NCM.

SR determines the amplifier's settling performance. Suppose a large negative step appears at Vp, it follows that the second-last mirror turns off. Consequently, almost all the current in M_6 is directed into M_{17} and amplified by the last mirror to discharge C_L . Similar analyses can be applied when there is a large positive input step occurring at Vp, resulting in a symmetric SR expressed by

$$SR_{NCM5} = \frac{K_{11} \times (K_{10} + 1)}{\sum_{l=1}^{11} K_l + 1} \times \frac{2I_b}{C_L}$$
(6)

The SR of the proposed amplifier increases, which can be realized by selecting relatively large K₁₀ and K₁₁.



(An ISO 3297: 2007 Certified Organization) Vol. 5, Issue 10, October 2016

VI. DESIGN AND STABILITY ANALYSIS OF 6-STEP NCM



Figure 5: Block diagram of the proposed 6-step NCM amplifier

Mirror factors (K) selected for the circuit design case can be mention as $K_1 = 7$, $K_2 = 6$, $K_3 = 7$, $K_4 = 12$, $K_5 = 15$, $K_6 = 1:5$, $K_7 = 38$, $K_8 = 10$, $K_9 = 27$, $K_{10} = 11$, $K_{11} = 16$. For the 6-step NCM, the total bias current (3 μ A) is divided into 240 unit-current (Iu = 12.5nA). To leverage the key metrics, the 1st mirror ($M_7 - M_8$) uses a small ratio of only 1 ($K_1 = 7$ and $K_2 = 6$). The 2nd mirror ($M_9 - M_{10}$) draws less current under a ratio of 1 ($K_3 = 7$ and $K_4 = 12$) to boost the DC gain and GBW, as they contribute less noise. Also, a larger K_7 enhances the SR. The last mirror ($M_{17} - M_{18}$) is assigned the largest ratio ($K_{11} = 16$) to benefit the SR and $G_{M, NCM6}$. Substituting these values into the DC gain, GBW and SR equation we can see that these are theoretically improved.

The equivalent small-signal diagram of the 6-step NCM amplifier is shown in Figure 5. G_{m1} , G_{m2} , G_{m3} , G_{m4} , G_{m5} and G_{m6} are the transconductances of M_{1-6} respectively while Z_{b1} , Z_{b2} , Z_{b3} , Z_{b4} , Z_{b5} and Z_{b6} correspond to the input impedances of the 1st to 6th mirrors. The transconductances of the transistors in the six mirrors are respectively represented by G_{mb1-6} , while Z_{out} models the output impedance that includes C_L .

VII. EXPERIMENTAL RESULTS OF 5-STEP AND 6-STEP NCM

In the 5-step and 6-ste NCM the unit-NMOS and unit-PMOS operate at the inversion levels corresponding to gmnu/Iu = $23.5V^{-1}$ and gmpu/Iu = $23.1V^{-1}$. AC analysis of the circuit provide the gain and stability information. 5-step NCM will provide a gain of 91dB and phase margin of $>70^{\circ}$. If the load capacitance change from 250 pF to 1 nF 5-step NCM can achieve favorable performance in 0.424-0.137MHz frequency region. In the case of 6-step NCM it provide a gain of 98 dB and phase margin of $>75^{\circ}$. And if the load capacitance change from 450 pF to 1 nF 6-step NCM can achieve performance in 0.841 – 0.397 MHz frequency region.



(An ISO 3297: 2007 Certified Organization) Vol. 5, Issue 10, October 2016



Figure 6: AC response of 5-step NCM



Figure 7: AC response of 6-step NCM

Slew rate determines the amplifiers settling performance. Slew rate can also defined as the rate of change of output or how quickly the output change with respect to the given input. When a large negative step appears at V_P , the value of negative SR obtained at the output. Similarly a large positive at V_P leads to positive SR. Therefore we give a dc pulse current at the V_P , which results a symmetric SR. If the load capacitance change from 250 pF to 1 nF the slew response also change from 0.325 V/µs to 0.0002 V/µs. In the case of 6-step NCM if the load capacitance change from 450 pF to 1 nF the slew response also change from 0.527 V/µs to 0.00018 V/µs. Power consumed by 5-step NCM is 6.9 µW and for 6-step NCM the power is 5.3 µW.



(An ISO 3297: 2007 Certified Organization)

	3-step NCM	4-step NCM	5-step NCM	6-step NCM
Load $C_L(nF)$	0.15 - 15	0.15 - 15	0.25 - 1	0.45 - 1
Phase $Margin(^0)$	> 80	> 60	> 70	> 75
Gain(dB)	72	84	91	98
Slew Rate(V/ μs)	0.0256 - 0.00025	0.0314 - 0.00037	0.325 - 0.00018	0.525 - 0.0002
GBW(MHz)	0.283 - 0.0027	0.35 - 0.013	0.424 - 0.137	0.841 - 0.397
Power (μW)@ V _{DD} (V)	50.44@1.2	47@1.2	6.9@1.2	5.3@1.2

Vol. 5, Issue 10, October 2016

Table 1: Comparison of 3,4,5 and 6-step NCM

Table 1 represent comparison of different topologies. From the table we can conclude that as the step size increases the performance of the single stage amplifiers improved from the previous stages.

VI. CONCLUSION

This paper introduced a NCM single-stage amplifier that has more design flexibilities with mirror steps and sub mirror ratios to optimize the performance metrics (GBW, DC gain and SR), while preserving a rail-to-rail output swing, and wide CL drivability without entailing any compensation capacitor or resistor. Both the performance limits and robustness of the NCM technique have been analytically explored. Two prototypes, 5-step and 6-step NCM amplifiers, were designed and analyzed in 180 nm CMOS technology for systematic comparison with 3-step and 4-step NCM.

REFERENCES

[1] Zushu Yan, Pui-In Mak, Rui P. Martins and Franco Maloberti, "Nested-Current-Mirror Rail-to-Rail-Output Single-Stage Amplifier With Enhancements of DC Gain, GBW and Slew Rate, "IEEE journal of solid-state circuits, vol. 50, no. 10, october 2015

[2] Y.-S. Son et al., "A column driver with low-power area-efficient pushpullbuffer amplifiers for active-matrix LCDs," in IEEE ISSCC Dig. Tech. Papers, 2007, pp. 142–143.

[3] C.-W. Lu, P.-Y.Yin, C.-M.Hsiao, M.-C.Chang, and Y.-S. Lin, "A 10-bit resistor-floating-resistor-string DAC (RFR-DAC) for high color-depth LCD driver ICs," IEEE J. Solid-State Circuits, vol. 47, no. 10, pp. 2454–2466, Oct. 2012..

[4] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," IEEE Trans. Circuits Syst. I, vol. 48, no. 9, pp. 1041–1056, Sep. 2001.

[5] Z. Yan, P.-I.Mak, M.-K. Law, R. P. Martins, and F. Maloberti, "A 0.013 mm 3.6 W nested-current- mirror single-stage amplifier driving 0.15-to-15 nF capacitive load with 62 phase margin," in IEEE ISSCC Dig. Tech. Papers, 2014, pp. 288–289..

[6] M. Ho, K. N. Leung, and K. Mak, "A low-power fast-transient 90-nm low-dropout regulator with multiple small-gain stages," IEEE J. Solid-State Circuits, vol. 45, no. 11, pp. 2466–2475, Nov. 2010.

[7] K. H. Mak and K. N. Leung, "A signal- and transient-current boosting amplifier for large capacitive load applications," IEEE Trans. Circuits Syst. I, vol. 61, no. 10, pp. 2777–2785, Oct. 2014.

[8] L. Yao, M. Steyaert, and W. Sansen, "A 1-V 140-W 88 dB audio sigma-delta modulator in 90-nm CMOS," IEEE J. Solid-State Circuits, vol. 39, no. 11, pp. 1809–1818, Nov. 2004.

[9] J. Roh, "High-gain class-AB OTA with low quiescent current," J. Analog Integr. Circuits Signal Process., vol. 47, no. 2, pp. 225–228, May 2006. [10] J. Roh, S. Byun, Y. Choi, H. Roh, Y.-G.Kim, and J.-K. Kwon, "A 0.9-V 60- W 1-bit fourth-order delta-sigma modulator with 83 dB dynamic range," IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 361–370, Feb. 2008.

[11] D. J. Allstot, "A precision variable-supply CMOS comparator," IEEE J. Solid-State Circuits, vol. 17, no. 6, pp. 1080–1087, Dec. 1982.

[12] B. Johnson and A. Molnar, "An orthogonal current-reuse amplifier for multi-channel sensing," IEEE J. Solid-State Circuits, vol. 48, no. 6, pp. 1487–1496, Jun. 2013.