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Theoretical Design of High Speed Low Power True Single-Phase Clocking D Flip-Flop and Its Self-Healing Circuit in 45-Nm CMOS Technology

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ABSTRACT*:* The D-flip flop is the basic building block for major components of a Phase-locked loop (PLL). The frequency detector and the phase-frequency detector are vital elements of the PLL and the use of D-flip flop in these modules is of prime importance. The most important challenge gazing at the designers is the scaling down, and to make the parameters meet as per the new scaled-down requirements. Decision regarding clocking, is one of them. This paper puts forth a novel design of a high-speed low power True-single-phase clocking D-flip flop, in a lower technology, i.e. 45-nm technology.

KEYWORDS: True-single-phase clocking, D-flip flop, PLL, frequency detector, phase-frequency detector.

I.INTRODUCTION

Phase-Locked Loops (PLLs) are functional circuits that generate signals phase-locked with external input signals. They are widely used for synchronization purposes and are essential in communication field. Owing to the broad use of mobile electronic systems, low-power consumption and low jitter have become the main concern in PLLs design. Besides, fast lock time is required in nearly all PLL applications.

The basic architecture of the PLL is shown in Fig. 1. A PLL consists of five main blocks:

- Phase Detector or Phase Frequency Detector (PD or PFD)
- Charge Pump (CP)
- Low Pass Filter (LPF)
- Voltage Controlled Oscillator (VCO)
- Divide by N Counter
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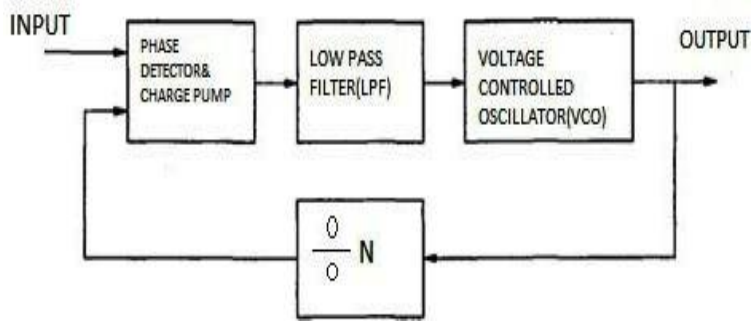

Fig. 1 Basic architecture of PLL

Over the years, the target has been the area, power consumption and jitter of the PLLs. Using self-healing technique, a wide-range PLL can be obtained. [1] Several topologies are available to choose from; Current-mode logic (CML), True

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single-phase clocked (TSPC) logic and extended TSPC (E-TSPC) logic. The conventional D-flip flops use E-TSPC logic. But, the TSPC is preferable, as it satisfies the speed requirement along with delivering low power consumption.

Self healing techniques are used to make the device work efficiently, at higher temperatures. Due to the self healing technique, the device can withstand temperature and leakage due to process variation.

II.BACKGROUND

The ICs do the clock generation and clock distribution within them. Hence, there is a responsibility of making-up for the clock signal variations, on the clocked storage element. Generally, in digital systems, the clock labels the moment when the state is changing, and even the moment when the next state is captured.

Ideally, it is considered that all the registers clock simultaneously, in a circuit. Hence, the clock signal arrival times at each register are measured with respect to a universal time reference. Practically, the clock arrival times to different registers vary, owing to various delay characteristics of the clock paths to the various points where registers are placed. [2] "This difference in clock signal arrival times between two sequentially adjacent registers is defined as clock skew T_{skew}."

Transfer of data between the data storage elements takes place during active phase of a clock. The different clocks possible, are single-phase clocking and multiple-phase clocking (Fig. 2).

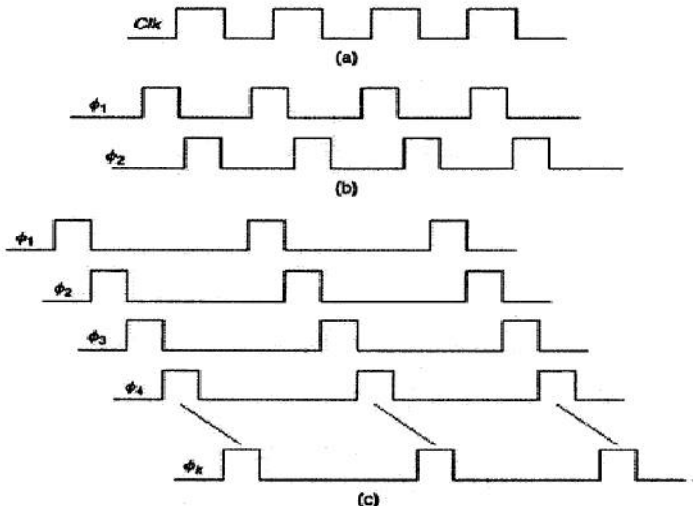

Fig. 2 (a) Single-phase clocking scheme
(b) 2-phase clocking scheme
(c) Multiple-phase clocking scheme

III.PROPOSED DESIGN

Fig 3.1 shows a dynamic ratioed logic TSPC D flip. The pseudo-MOS has much lower resistance and capacitance than series than series stacked MOS devices. Thus, the speed of the DFF with clocking pseudo-MOS could be faster than the one with CMOS logic. To consider the driver transistors and load transistors that are most critical to the delay of a particular state transition, however, it is desirable to identify those transistors not to become bottlenecked. For example, in the time for the 0 –>1, node A causes node B to discharge from high to low through transistors NM_0 and NM_1 following the pre-charge phase. The discharge node will in turn cause Q' to charge up to logic 1 via PM_2, while the output high voltage VOH closes but does not reach VDD. To consider driving capability, however, the output pseudo-PMOS should have a much larger pMOS. It would result in large gate capacitance, which affects the discharge capability. An nMOS transistor NM_4 controlled by is inserted into the output stage. NM_4 is turned off by node A via an

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added inverter before the end of the pre-charge, so that the discharge path for Q' is safely cut off before NM_3 is turned on at evaluation. This flip-flop can be used as a component of a divide-by-4/5 synchronous counter in a high-frequency dual-modulus pre-scalar but cannot be used as a flip-flop alone because of the violation of the edge-triggering characteristic.

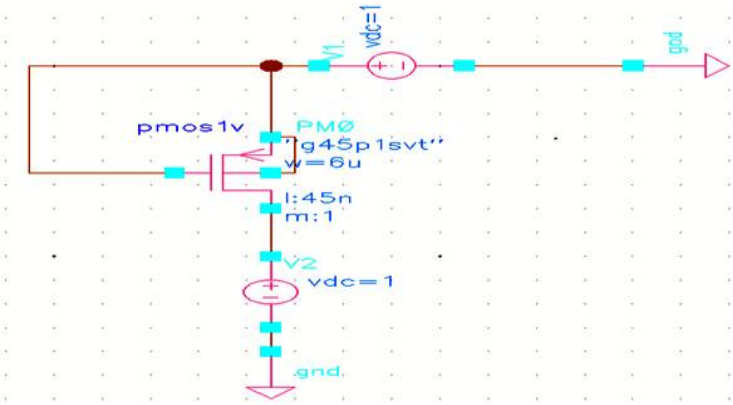

Fig 3.1 pMOS with Gate and Drain connected to 1 V supply

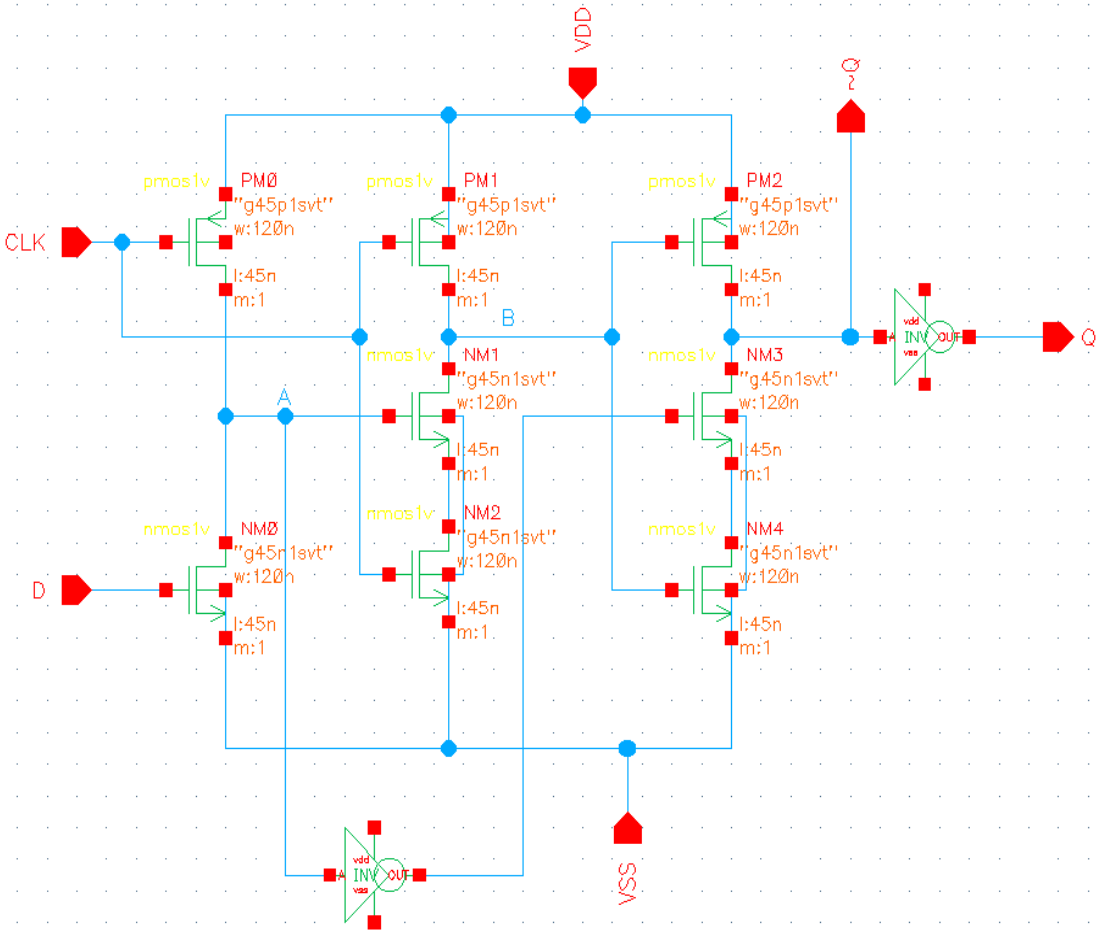

Fig 3.2 TSPC D-FF

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A. MALFUNCTION IN TSPC D-FF

The undesired leakage current may charge or discharge to alter the states of the nodes A, B, and Q' in this TSPC DFF as shown in Fig. 3.3-3.5. For example, two kinds of the malfunctions may occur at the node A as shown in Fig. 3.3 and 3.4, respectively. The first case (Fig 3.3) is that the initial state of the node A is high; however, a leakage current discharges it to ground. The second one (Fig 3.4) is that the initial state of the node A is low, but a leakage current charges it to high. To consider the node B in Fig 3.4, assume that the leakage current charges the node B to be high when CK is high. It will not affect the original state of the node Q'. Thus, the leakage problem occurred at the node B is not considered here. For a malfunction occurred at the node, the simplified circuit is shown in Fig.3.5. Assume the transistor M_1 is turned off, CK is low, and the initial state of the node is low. Since the node is floating, the leakage current from M_1 may charge the node to high and a malfunction occurs. Note that the leakage current through M_2 and M_3 is smaller than that from M1. It is because the cascode transistors, M_2 and M_3, induce a lower leakage current [3]- [4].

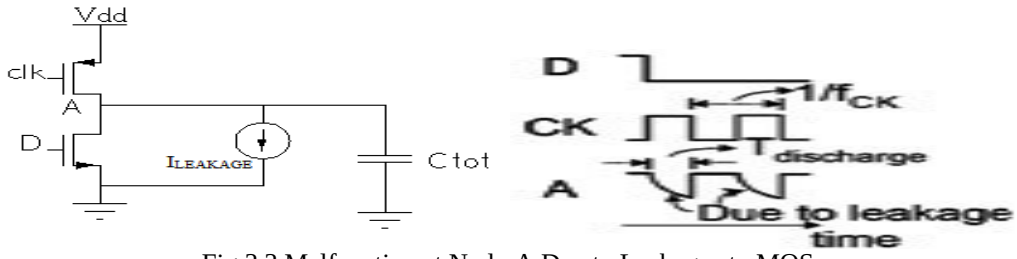

Fig 3.3 Malfunction at Node-A Due to Leakage at nMOS

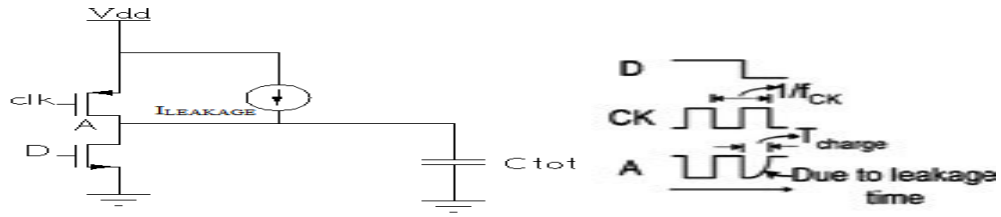

Fig 3.4 Malfunction at Node-A due to Leakage at pMOS

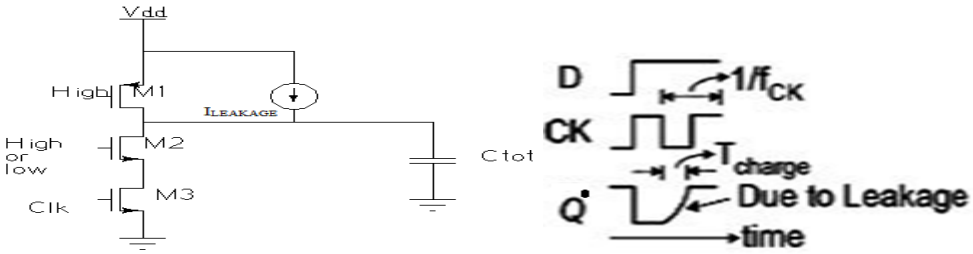

Fig 3.5 Malfunction at Node Q'

B. SELF HEALING CIRCUIT FOR TSPC D-FF

To detect and heal the above issues occurred at the nodes A and Q', the proposed self-healing circuit is shown in Fig. 3.6. This self-healing circuit consists of a detector and three compensators. By using a self-healing circuit, the timing diagrams of a TPSC DFF with and without a malfunction are shown Fig. 3.7, respectively. Assume the signal Enable in the self-healing circuit is low to disable the latch in Fig. 3.6. For a case that the malfunction is detected, the timing diagram is shown in the left side of Fig. 3.7. When the clock CK goes high, the pulse generator outputs a short pulse at the gate of M2A, which goes high to clear. When the input D of the DFF is high, the rising edge of the clock CK triggers the DFF's output Q to go high (or goes low) to turn off M3A. The pulse generator outputs a low pulse at the gate of M1A to turn off M4A. Before the next rising edge of CK arrives, is assumed to be charged to high due to the undesired leakage current. In the meantime, Q goes low to turn on M3A and enables. It indicates that the

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malfunction of this TSPC DFF occurs. The size ratio of M4A and M3A is 5 to ensure, when both M3A and M4A are turned on. It has been simulated and verified for all corners and a supply voltage variation of 10% and the temperature of C. For a case that the malfunction is fixed, the timing diagram is shown in the right-hand side of Fig. 3.7 where is always low. When the signal Enable is high and the malfunction is detected, is latched by a latch and the compensator is active. For example, assume the initial state of is low and the leakage current is charging the node. Since is low and, the transistors, M5A–M8A, in a compensator will be turned on. A minimum-sized transistor M7A is used to counteract the leakage current and repair the state of the node to be low finally. The leakage current is much smaller than that a minimum-size MOS can provide. Similarly, when a malfunction is detected, the compensators will turn on M7B or M7C to counteract the leakage current and repair the state at the node A. Pulse generator circuit and D latch used in this circuit are shown in Fig 3.8 and Fig 3.9 respectively. The whole self healing TSPC D flip flop is shown in Fig 3.9.

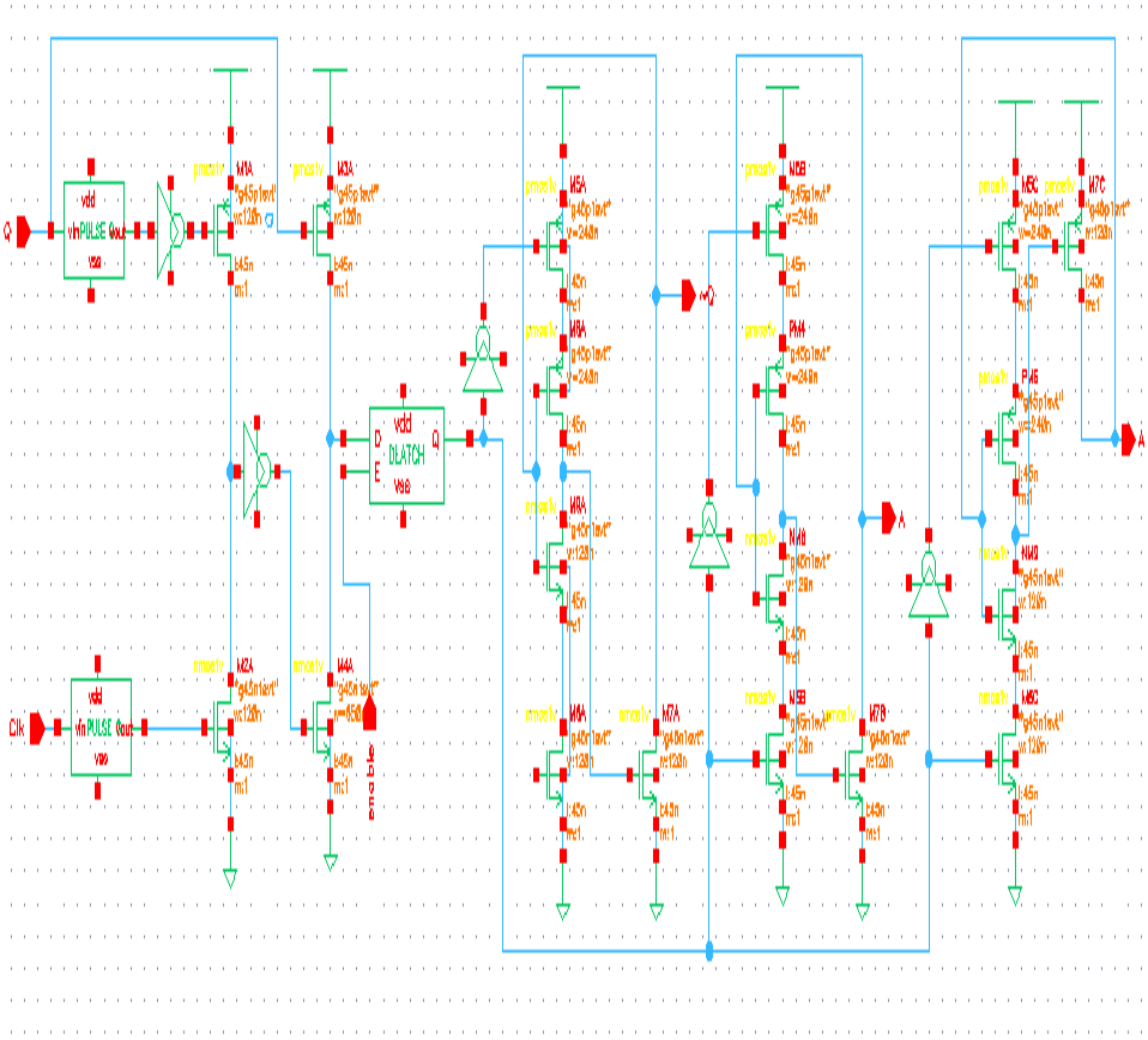

Fig3.6 A Detector and 3-compensator circuit for TSPC D-FF

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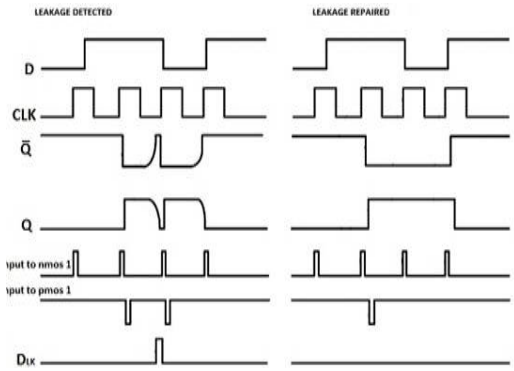

Fig 3.7 Malfunction Detected and Malfunction Healed timing graph

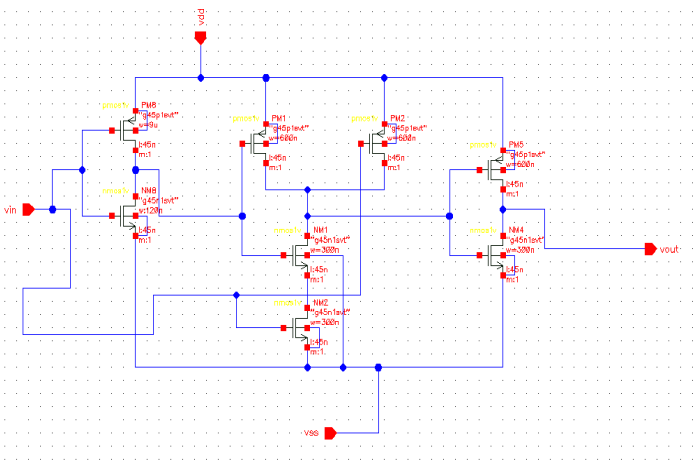

Fig 3.8 Pulse Generator circuit

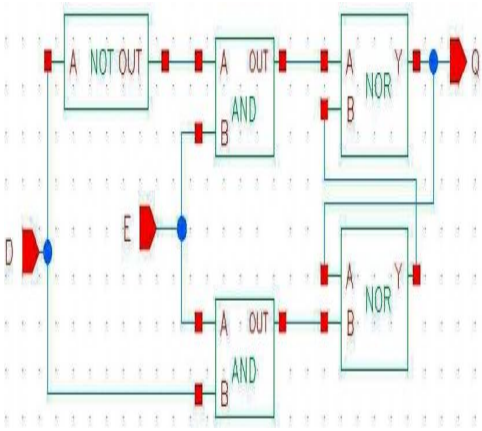

Fig 3.9 D Latch circuit

IV. RESULTS AND DISCUSSION

Using the self-healing TSPC D-flip flop, the components of a PLL can be modelled, effectively. Fig 4 shows the designed self-healing TSPC D-flip flop.

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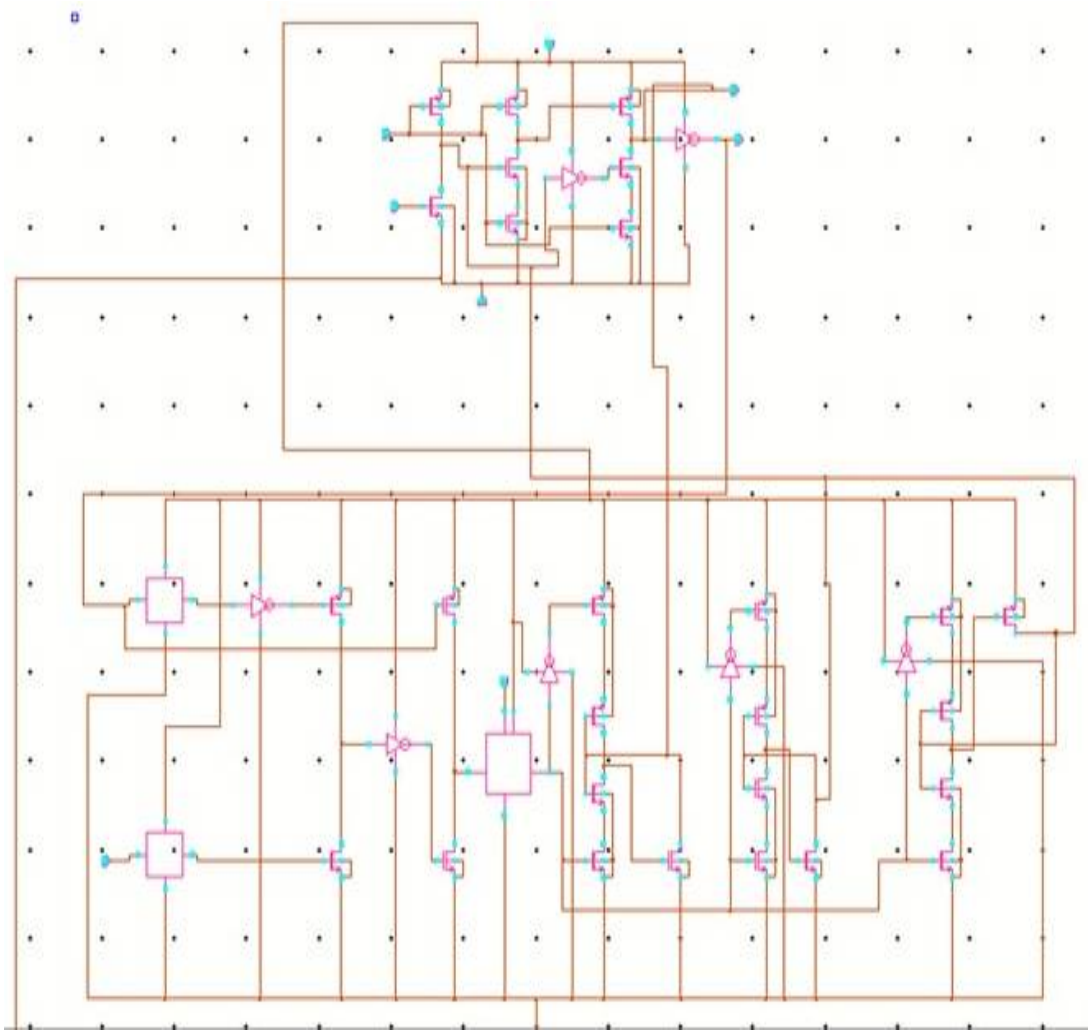

Fig 4 Self-Healing TSPC D Flip Flop

V. CONCLUSION

This is a self healing PLL in 45nm CMOS technology. Self healing techniques are used to make it work at 100°C. Due to this self healing technique, it can withstand temperature and leakage due to process variation. This can be used where the operating temperature is higher than usual (up to 100^{o}C).

But, the modeled TSPC D-FF can only be used with circuits for fast operation but it cannot be used in other applications as it violates the edge triggering principle of D FF at high frequency.

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