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Modeling and Simulation of Asymmetric Cascaded Multilevel Inverter with Reduced Switches using Multicarrier PWM Control

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ABSTRACT: This paper presents the modeling and simulation of asymmetric cascaded multilevel inverter with reduced switches using multicarrier pulse width modulation (MC-PWM) control techniques. The ultimate aim of the paper is to produce multiple output levels with minimum number of semiconductor devices. This paper uses only 11 switches along with 3 diodes and 4 asymmetrical sources to produce an output voltage of 21 levels. The modulation technique plays a major role in commutation of the switches. Multilevel inverters performance is greatly superior to that of conventional two-level inverters due to their reduced total harmonic distortion (THD), lower switch ratings, lower electromagnetic interference, and higher DC link voltages used for high-voltage and high-power applications. In this paper, a novel twenty one-level reduced switch cascaded multilevel inverter based on a multilevel DC link inverter topology with reduced switching components is proposed to improve the multilevel inverter performance and the overall cost and circuit complexity are greatly reduced. The effectiveness of the proposed system is proved with the help of simulation. The simulation is performed in MATLAB/Simulink. From the simulation results, it shows that the proposed multilevel inverter works properly to generate the multilevel output waveform with minimum number of semiconductor devices and to achieve high dynamic performance with low THD.

KEYWORDS: Multilevel inverter (MLI), Cascaded multilevel Inverter (CMLI), Pulse width modulation (PWM), Multicarrier Pulse Width Modulation (MC-PWM), Total harmonic distortion (THD).

I.INTRODUCTION

Today, the energy demand is moving on increasing toward generating power with renewable energy source that may be dispersed in a wide area, and most of them are renewable, as they have greater advantages due to their environmentally friendly nature. Photovoltaic (PV) energy has augmented interest in wide range of electrical power applications, since it is considered as a basically limitless and generally on hand energy resource with the focus on greener sources of power particularly for distant locations where utility power is engaged [1-4]. The solar can be used by all in universe which doesn't need more investigations of producing electricity [5-7]. This leads to research in multilevel inverters.

The multilevel inverters are classified into three types namely: (i) Diode clamped multilevel inverters; (ii) Flying capacitor multilevel inverter; and (iii) Cascaded H bridge multilevel inverter. Of these the cascaded H bridge multilevel inverter topologies give better results. The research goes on increasing to propose a new structure of inverter with reduced semiconductor devices with increased multilevel at the output waveform [8-9]. The study of the multi sampled multilevel inverters and their control techniques to improve the performance of the multilevel inverters. This also deals with the different control techniques to be implemented in multilevel inverters in order to reduce the total harmonic distortion (THD). But they don't concentrate on the structure of the multilevel inverters [10-11].

A way to balance the capacitor voltage to produce voltage levels of equal width. Therefore the THD is reduced. There is no change in the structure of the inverter. Only the technique has been implemented with conventional structure but they achieved better THD [12-13]. The new algorithm for producing the switching signals. Here new optimization algorithm to produce the modulation signals; the algorithm works better than the other techniques but the structure of

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cascaded multilevel inverter remains same. Hence the switching loss is more and the number of switches used is same as that of the conventional one. Therefore it is necessary to find the new structural way of producing multilevel with reduced semiconductor devices [14].

The cascaded H bridge topology to be used, to reduce THD and the multilevel inverter fed multiphase induction motor; here they use diode clamped inverter to produce multiple levels at the output and they are used to drive the five phase motor. The performance analysis is done using this. Since they use diode clamped multilevel inverter the number of semiconductor devices is high and hence the losses are heavy. On replacing it with a new structure and by increasing the number of levels can improve the performance of the system [15-16]. The closed loop control strategy implemented in multilevel inverter is explained and the control circuit is also big which again increases the circuit complexity thus reducing the effectiveness of the proposed system [17-19].

From all the above analysis, conclude that the control circuitry of the multilevel inverter. But the structure of inverter remains same. On increasing the levels the structure becomes more complex and bigger in size reducing the efficiency of the system. Here, a new structural multilevel inverter to produce multiple levels at the output voltage with minimum number of power semiconductor devices. The multi carrier level shifting PWM has also been implemented. Hence the THD is reduced lot with minimum number of devices with low switching noise.

II.PROPOSED CASCADED MULTILEVEL INVERTER TOPOLOGY

The proposed multilevel inverter uses the ladder type connection of switches and diodes along with the voltage sources. In this topology, use asymmetrical voltage sources which may obtained from battery or from renewable energy sources like biomass, solar etc. the asymmetric dc voltage sources are incrementing in nature in the order of n, $2n$, $3n$, $4n$, ⋯ Where n = lowest DC voltage source magnitude. The structure of proposed multilevel inverter is shown in Fig 1 consisting of main and auxiliary inverter. Here use the IGBT as the switching device. The anti-parallel diodes are used for the reverse current path so that the multiple levels can be obtained at the outputs. The proposed system uses less number of power semiconductor devices.

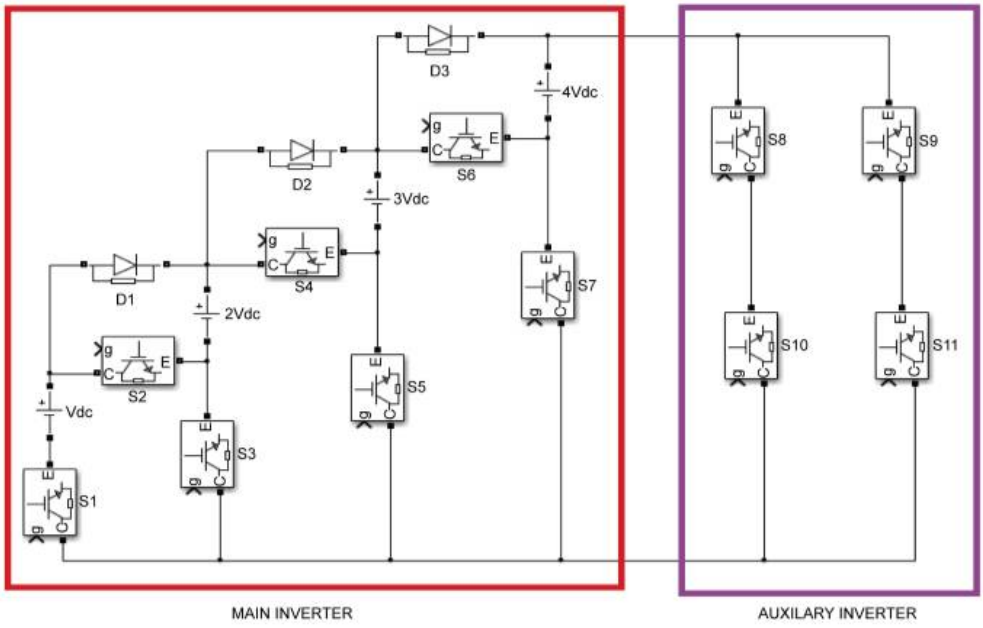

Fig. 1 Structure of proposed multilevel inverter

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The following Table 1 shows the switching sequence given to the proposed topology to generate 21 level voltage output. The operation of the proposed asymmetric multilevel inverter is explained with the help of Table 1. The switch works ON, two states ON and OFF. When the switch is ON, it is in saturation region and it starts conducting when the switch is OFF, it is in cut off region hence it does not conduct. It has 11 modes of operation to produce 11 voltage levels from zero to $10V_{dc}$. The relation between the number of output levels and number of semiconductor devices are calculated by using the formulae as shown below. Let "N_{DC}" be the number of DC sources or stages and the associated number of output voltage level can be calculated by using the equation (1),

$$M=N_{DC}(N_{DC}+1)+1 \quad (1)$$

The number of switches used in this topology is given by the equation (2),

$$NS=2(N_{DC})-1 \quad (2)$$

The number of bypassed diodes used in this topology is given by the equation (3),

$$N_{diodes}=N_{DC}-1 \quad (3)$$

Therefore if, use 4 dc sources along with 3 diodes and seven semiconductors power switches, it can capable of producing 21 voltage levels at the output. The proposed system consists of two parts namely main inverter and auxiliary inverter. From Table 1 it is clear that the proposed multilevel inverter uses only minimum number of semiconductor devices when compared to the conventional one. Since the switching devices are reduced to a great extent the switching losses is also reduced which increases the effectiveness of the system.

Table 1. Comparison of cascaded H-bridge and proposed inverter

Items	Cascaded H-bridge for 21 output levels	Proposed inverter for 21 output levels
	Single phase	Single phase
Switches	40	11
Diodes	-	3
DC sources	10	4

III.DIFFERENT MODES OF OPERATION

Mode-1: In mode the switch S_1 alone conducts. The current flows through S_1, the source V_1, the diode D_1, D_2 and D_3 to produce the voltage of $1V_{dc}$.

Mode-2: In mode the switch S_3 alone conducts. The current flows through S_3, the source V_2, the diode D_2 and D_3 to produce the voltage of $2V_{dc}$.

Mode-3: In mode the switch S_5 alone conducts. The current flows through S_5, the source V_3, the diode D_3 to produce the voltage of $3V_{dc}$.

Mode-4: In mode the switch S_7 alone conducts. The current flows through S_7 and the source V_4 to produce the voltage of $4V_{dc}$.

Mode-5: In mode the switch S_1 and S_6 conducts. The current flows through S_1, the source V_{dc}, the diode D_1 and D_2, the switch S_6 and the voltage source $4V_{dc}$. Hence it produce the voltage level of $5V_{dc}$ ($V_{dc} + 4V_{dc} = 5V_{dc}$) at the output.

Mode-6: In mode the switch S_3 and S_6 conducts. The current flows through S_3, the source $2V_{dc}$, the diode D_2, the switch S_6 and the voltage source $4V_{dc}$. Hence it produce the voltage level of $6V_{dc}$ ($2V_{dc} + 4V_{dc} = 6V_{dc}$) at the output.

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Mode-7: In mode the switch S_5 and S_6 conducts. The current flows through S_5, the source $3V_{dc}$, the switch S_6 and the voltage source $4V_{dc}$. Hence it produce the voltage level of $7V_{dc}$ ($3V_{dc} + 4V_{dc} = 7V_{dc}$) at the output.

Mode-8: In mode the switch S_1, S_4 and S_6 conducts. The current flows through S_1, the source $1V_{dc}$, the diode D_1, the switch S_4, the voltage source $3V_{dc}$, the switch S_6 and the voltage source $4V_{dc}$. Hence it produce the voltage level of $8V_{dc}$ ($1V_{dc} + 3V_{dc} + 4V_{dc} = 8V_{dc}$) at the output.

Mode-9: In mode the switch S_3, S_4 and S_6 conducts. The current flows through S_3, the source $2V_{dc}$, the switch S_4, the voltage source $3V_{dc}$, the switch S_6 and the voltage source $4V_{dc}$. Hence it produce the voltage level of $9V_{dc}$ ($2V_{dc} + 3V_{dc} + 4V_{dc} = 9V_{dc}$) at the output.

Mode-10: In mode the switch S_1, S_2, S_4 and S_6 conducts. The current flows through S_1, the source $1V_{dc}$, the switch S_2, the voltage source $2V_{dc}$, the switch S_4, the voltage source $3V_{dc}$, the switch S_6 and the voltage source $4V_{dc}$. Hence it produce the voltage level of $10V_{dc}$ ($1V_{dc} + 2V_{dc} + 3V_{dc} + 4V_{dc} = 10V_{dc}$) at the output.

Mode-11: In this mode all the switches are in off state. Therefore the output voltage is zero.

From Fig 1, the main inverter can generate only zero and positive voltage levels. The zero output voltage level is obtained when all the switches are turned OFF. The other voltage levels are obtained by proper switching between the switches. The switching is given in Table 2. The output voltage of main inverter is always zero and positive only. To operate as an inverter, it is necessary to change the voltage polarity in every half cycle. For this purpose, the output of the Main inverter is fed to the H-Bridge inverter circuit which is called as the auxiliary inverter. The auxiliary inverter converts the main inverter positive voltages into positive and negative outputs. The switches S_8 and S_{10} conducts to produce output voltage and the switches S_9 and S_{11} conducts to produce the negative output voltages. When S_8 to S_{11} are OFF it produce zero voltage. The main inverter switches S_1 to S_7 undergoes high switching frequency to produce multiple output voltage levels. The auxiliary inverter switches S_8 to S_{11} uses fundamental switching frequency.

Table 2. Switching States of 21-level inverter

Modes	Switching States							Output voltage level
	S1	S2	S3	S4	S5	S6	S7	
Mode 1	1	0	0	0	0	0	0	1Vdc
Mode 2	0	0	1	0	0	0	0	2Vdc
Mode 3	0	0	0	0	1	0	0	3Vdc
Mode 4	0	0	0	0	0	0	1	4Vdc
Mode 5	1	0	0	0	0	1	0	5Vdc
Mode 6	0	0	1	0	0	1	0	6Vdc
Mode 7	0	0	0	0	1	1	0	7Vdc
Mode 8	0	0	0	1	0	1	0	8Vdc
Mode 9	0	0	1	1	0	1	0	9Vdc
Mode 10	1	1	0	1	0	1	0	10Vdc
Mode 11	0	0	0	0	0	0	0	0

IV.MODULATION TECHNIQUES

Modulation is defined as a technique or methodology to produce the pulses for the semiconductor devices to operate them in ON and OFF states. During ON state the device is in saturation region hence the switch starts conducting and during OFF state the switch is in cut-off region hence the switch stops conducting. Since the width of the pulse computes the width and level of the output voltage, it is important to concentrate on the modulation technique. The

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PWM technique compares the reference and the carrier waveform to produce the switching pulse. The reference will be in line frequency whereas the frequency of carrier decides the switching frequency of the semiconductor device.

A. MULTICARRIER PULSE WIDTH MODULATION SCHEMES

Mostly the multilevel inverter uses the multicarrier PWM technique to generate switching signals and also the output waveform appears as close as to the sinusoidal one. The multicarrier PWM uses (*N*-1) carriers and the sine wave to produce the switching signals for the *N*-level inverter. It compares the carrier along with the sinusoidal waveform in order to produce the switching signals of the inverter. Depending upon the physical structure of the carrier waveforms they are classified into two types namely: (i) Phase Shifting PWM (PS-PWM); (ii) Level shifting PWM (LS-PWM). In PS-PWM techniques the carriers are equal in amplitude and frequency but they have phase difference with each other. In LS-PWM techniques the carriers are equal in amplitude (peak to peak amplitude), same frequency and phase but they differ in their levels of biasing.

B. MULTICARRIER LEVEL SHIFTING PWM TECHNIQUE

There are three alternative PWM strategies with different phase relationships for the level-shifted multicarrier modulation; (i) Phase disposition (PD), where all carrier waveforms are in phase, (ii) Phase opposition disposition (POD), where all carrier waveforms above zero reference are in phase and are carrier waveforms below the zero reference are 180 degree out of phase and (iii) Alternate phase disposition (APOD), where every carrier waveform both above and below zero reference are in out of phase with its neighbouring carrier by 180 degree.

C. PHASE DISPOSITION LEVEL SHIFTING PWM

The carrier-based implementation the phase disposition PWM scheme is used. Generally the sinusoidal reference signal is compared with the triangular carriers to produce switching signals to the circuit. In the carrier-based implementation, at every instant of time the modulation signals are compared with the carrier and depending on which is greater, the switching pulses are generated is shown in Fig 2.

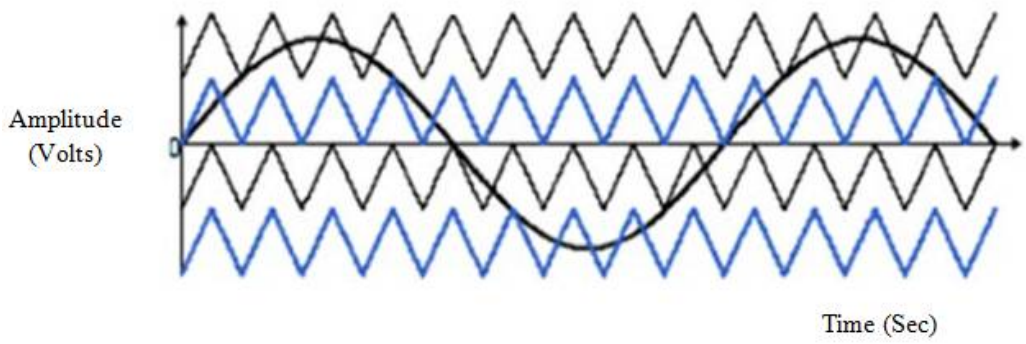

Fig. 2 Multi carrier level shifting phase disposition pulse width modulation (MC-LS-PS-PWM)

Usually for an *N*-level inverter, the system uses ($N - 1$) triangular carriers to produce the switching signals. But here our proposed system uses only ($N - 1$)/2 carriers to produce *N*-level output voltages. Therefore in this system, not only reduced the number of semiconductor devices but also we have reduced the number of carrier waveform by 50%. Hence the complexity of the control system is reduced which increases the performance of the entire system.

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V. SIMULATION RESULTS AND DISCUSSION

The proposed model of Multilevel Inverter Using MC-PD-LS-PWM uses only 11 switches and diodes with four asymmetrical voltage sources to 21 levels in the output voltage waveforms. The main inverter produces only positive voltage of levels 1 to 10. The auxiliary inverter converters it positive ten levels, negative ten levels along with one zero level to produce an output of 21 levels at their output voltage.

From the Fig 1, proposed inverter, it has 11 switches numbered from S_1 to S_{11}. The Switches S_1 to S_7, along with three diodes D_1, D_2 and D_3 with four asymmetric voltage sources V_{dc}, $2V_{dc}$, $3V_{dc}$, $4V_{dc}$ forms the main inverter whose output will be in positive regions only. It produces 11 levels of voltage from zero to $10V_{dc}$. The switch S_8 to S_{11} forms the auxiliary inverter which is a conventional H bridge inverter, when switch S_8 and S_{11} is on it produce the positive voltage levels zero to $10V_{dc}$. When S_9 and S_{10} are on it produces the negative voltage levels zero to $-10V_{dc}$. Thus the proposed inverter produces 21 voltage levels with positive and negative levels of $+10V_{dc}$ to $-10V_{dc}$. Here the V_{dc} used is 25 volts. Hence it is capable of producing amplitude of +250 to −250 volts.

The output voltage waveform with 21 voltage levels is shown in Fig 3. It indicates the single phase output voltage of proposed asymmetric cascaded multilevel inverter. The actual output of the inverter is +250 to −250 volts but due to some losses the output obtained is +240 to −240 volts. Fig 4 shows the Multicarrier level shifting pulse width modulation signals.

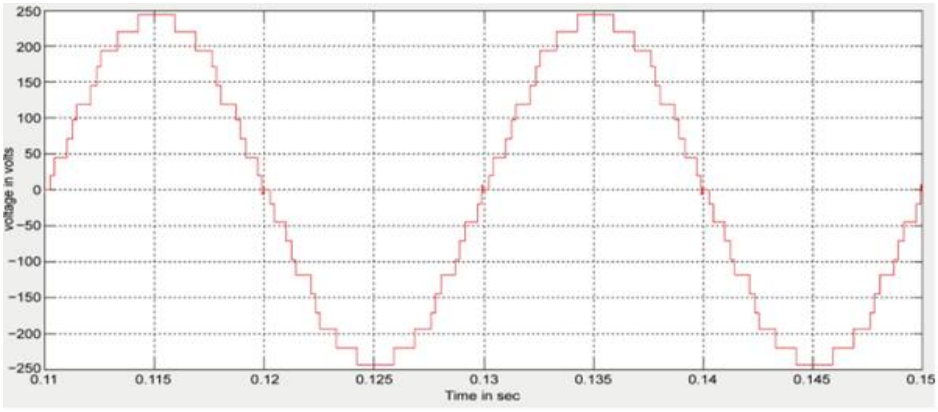

Fig. 3 Single phase 21 level Output line voltage waveform

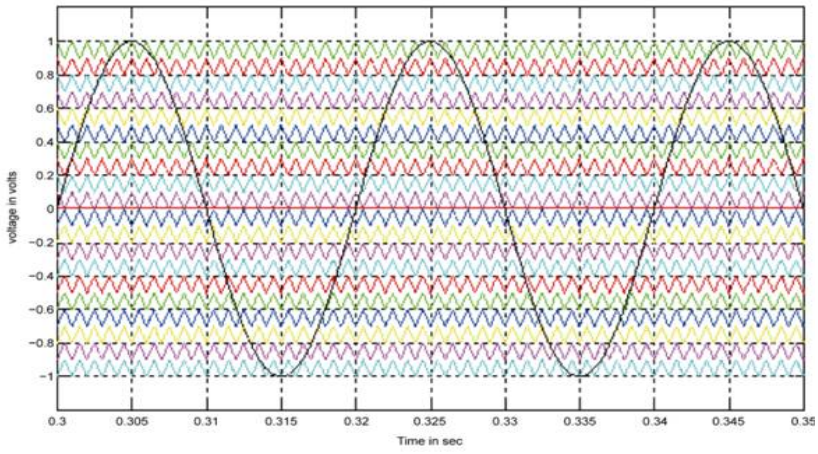

Fig. 4 Output waveform of MC-LS-PS-PWM

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Here the sine wave acts as the reference signals, the carriers are triangular signals, here we use more than one carrier so it comes under multicarrier classification, the carrier signals are equal in amplitude and phase but they differ in their level of distribution. Fig 5 shows the total harmonic distortion present in the output voltage of the proposed multilevel inverter with level shifting pulse width modulation technique

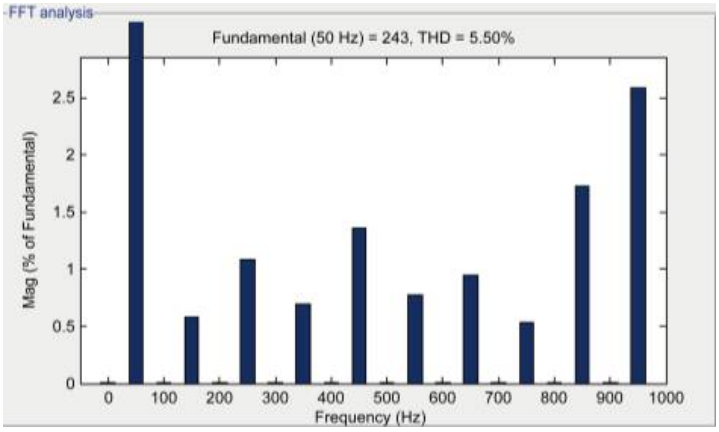

Fig. 5 THD of voltage using MC-LS-PS-PWM

VI.CONCLUSION

The modeling and simulation of asymmetric cascaded multilevel inverter with reduced switches using multicarrier PWM control techniques platform is implemented. The configuration for the proposed system is designed and simulated using MATLAB/Simulink. The MC-LS-PD-PWM technique involved to further improve the performance of the inverter by reduces the THD. This system guarantees a fast transient response, a high disturbance rejection capability, a robust performance and lower THD is obtained. The simulation also proves that if any failure occurs in any one of the switches it is still capable of producing multiple voltage levels without shunt downing the entire systems. The simulation result also proves the effectiveness of the proposed multilevel inverter which uses less number of power semiconductor devices. The results clearly show that the proposed topology can effectively work as a multilevel inverter with a reduced number of switches and carriers for PWM.

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