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Design & Analysis of Six Port Technology for Multi input Multi output and Millimeter wave Radio Receiver Applications

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ABSTRACT: With recent advances in semiconductor processing technology and the development of reconfigurable devices, high bit-rate software-defined radio (SDR) has become practical for commercial applications. This paper proposes an SDR receiver platform based on a new substrate integrated waveguide six-port structure. This SDR receiver platform operates from 22 to 26 GHz and it is designed to be robust, low cost, and suitable for different communication schemes. In this study, the receiver is demonstrated to support quadrature phase-shift keying and 16 quadrature amplitude modulation schemes. System-level sim- ulation is made and prototype circuits are fabricated to evaluate the system performance. It is found that the combination of SDR and six-port technology can provide a great flexibility in system configuration, a significant reduction in system development cost, and also a high potential for software reuse. The proposed receiver shows a possible application of universal direct demodulator for future SDR terminals in various wireless communication systems.

KEYWORDS: Digital receiver, quadrature amplitude phase- shift keying (QPSK), six-port junction, 16 quadrature amplitude modulation (QAM16), software-defined radio (SDR), substrate integrated waveguide (SIW).

I. INTRODUCTION

SOFTWARE-DEFINED radio (SDR) is an information transfer system (ITS) that combines technologies from the historically separated fields of computers and radios. Emerging from military applications, SDR has gained much attention among researchers and practitioners working in the wireless communication field and it has been identified as one potential method to enhance the flexibility and usability of Wireless communication systems.

In the past, the limited operating speed of analog-to-digital converter (ADC) and limited processing ability of reconfig- urable chips for digital signal processing were known to slow down the development of SDR towards useful commercial ap- plications. With recent advances in semiconductor processing technology and the development of reconfigurable devices such as digital signal processors (DSPs) and field-programmable gate arrays (FPGAs), SDR has now become practical in system solutions including wireless local area networks (LANs), audio, television broadcasting, and interoperability between different radio services.

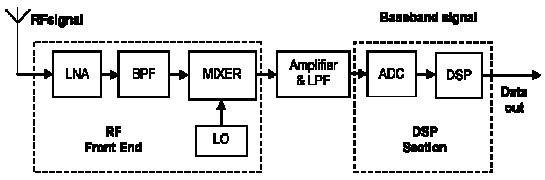

Fig. 1. Block diagram of typical SDR receiver.

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The block diagram of a typical practical SDR receiver is shown in Fig. 1. The RF signals are first down-converted, then such down-converted signals are digitized and sent to the DSP, and all of the subsequent processing is implemented in software. SDR consists of adaptable hardware components coexisting with software modules that govern the hardware behavior. Depending upon a specific application, SDRs may lso need to perform source and channel coding/decoding, multiple-access processing, frequency spreading/de-spreading, and encryption/decryption. While these basic functions are the same for SDRs and traditional radios, the implementation of these functions may be very different.

The primary distinction between SDRs and traditional radios lies in the programmability or configurability of SDRs, whereas traditional radios either do not have or have a limited capability in this respect. With SDR, software functions define the base- band and protocol elements and provide an environment for easy application development. Without introducing new hard- ware, an SDR can change operating characteristics or param- eters such as the operating frequency range, modulation type, bandwidth, maximum radiated or conducted output power, and network protocols by changing the software programs executing in processing resources. This enables a single wireless device to be reprogrammed for using different modulation, coding, and access protocols. [1]–[5]

This great flexibility of SDR provides a tremendous oppor- tunity for solving interoperability problems between the many different existing standards, implementing new standards, and minimizing the amount of hardware necessary to perform re- quired communications across these different standards. SDR also allows more efficient use of the spectrum by facilitating spectrum sharing and allowing equipment to be reprogrammed to more efficient modulation types. Its capability of being pro- grammed also enhances interoperability between different radio services.

II. PLATFORM ARCHITECTURE

One key point of SDR is to have a digital-processing kernel with almost infinite processing ability. Although DSP and semiconductor technology have been developed rapidly over the past ten years, the operating speed level of the current DSP chip cannot completely support a multichannel multimodu- lation SDR at the IF level. Therefore, certain software radio systems adopt multichip architecture and parallel algorithm, thereby increasing the design complexity and potential cost. Instead of digitalizing signals at IF, signals can also be digital- ized at baseband to reduce the processing requirement for DSP chips. As a new solution of SDR design, the direct demodu- lator architecture, based on six-port technology, or "multiport demodulator," is used in our proposed RF software receiver. Signals are down-converted from RF to baseband directly by a six-port junction.

Six-port technology has been under development for the past 30 years starting with microwave and millimeter-wave mea- surement and network analyzer applications. The vector ratio of incident waves at two input ports can be calculated using the output power readings at the remaining four ports. In doing this, there is no need of down-converting the signal to IF to make phase comparison. In 1994, the first six-port receiver was proposed as a direct digital receiver [6]. In principle, the six- port consists of linear circuits with signal dividers and com- biners (or couplers) interconnected in such a way that four or " " different vectorial combinations of the reference signal and signal to be measured (receiver signal) are obtained. The uses of different phase shifts and attenuation between the compo- nents such that the two RF input signals generate different am- plitudes and phases at four output ports. The signal levels of the four baseband output signals are detected using Schottky diode detectors or other RF quadratic detectors. By applying suitable baseband signal-processing algorithms, the magnitude and phase of the unknown received signal can be determined from the four output signal levels for the given modulation and coding scheme [6].

As we know, a wideband down-converter is not readily avail- able at millimeter-wave frequencies. In a six-port receiver, the six-port junction plus power detectors work as a down-con- verter, which offers a cost-effective approach to directly down- convert the RF signal to baseband signal. In addition, the rel- ative low-frequency baseband signals reduce the ADC's sam- pling and DSP capability requirement. On the other hand, the six-port receiver needs a set of four baseband bandpass filters (BPFs) and ADCs, which potentially increase the system cost, but with the recent development of ASIC technology, the price of these components was significantly reduced, therefore, the six-port SDR receiver structure is economically efficient. Fig. 2 shows the structure of the proposed six-port SDR receiver. The RF front-end consists of a low-noise amplifier (LNA), a BPF, a six-port junction, and four power detectors. The six-port junction works as an RF down converter in the proposed receiver. Port 2 connects to the RF signal and port 1 connects to the local oscillator (LO), the other four ports are connected to RF power detectors. The output voltages of the RF power detectors represent power levels of the four output ports of the six-port circuit. Signals from ports 1 and 2 are directly down-converted from RF to baseband frequency in the form of the output of power detectors. The signals from power detectors are then sent to the DSP section after passing

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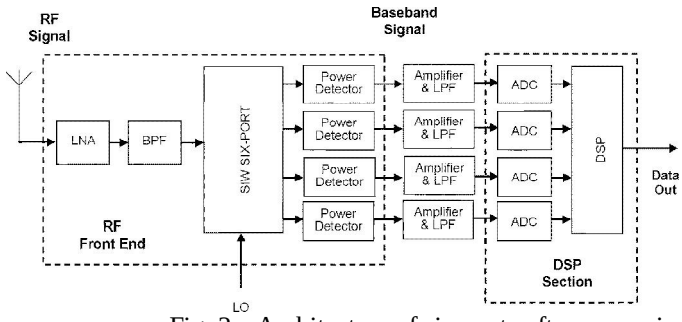

Fig. 2. Architecture of six-port software receiver.

a set of BPFs and baseband amplifiers. The DSP section is responsible for the baseband signal processing such as demod- ulation and decoding. The receiver is designed to operate at the millimeter-wave frequency and operates over a wideband for multimode schemes.

As shown in previous research, the six-port receiver approach offers wideband accommodation to ever-changing communi- cation specifications required in SDR systems. Some six-ports can offer impressive widebands, namely, 2–2200 MHz [7],
0.5–9 GHz [8], and 22–31 GHz [9]. Therefore, the six-port re- ceiver can be used in various applications such as FM radio, TV, cordless phones, paging, global positioning systems (GPSs), digital audio broadcasting (DAB), mobile satellite (MSAT), personal communications systems (PCSs), radar satellite, satellite multimedia, local multipoint communication systems (LMCSs), and so on. Compared with the traditional SDR receiver system, the six-port direct SDR receiver has wider bandwidth, low cost for RF circuits, and low DSP capability requirement.

III. SIW SIX-PORT CIRCUIT DESIGN

As a key RF component of the proposed receiver, an SIW six-port circuit [10] was designed for the proposed SDR receiver platform. The SIW technology, as a part of the substrate inte- grated circuits (SICs) family, has been proposed recently [11], [12] as an attractive technology for low-loss, low-cost and high- density integration of microwave and millimeter-wave compo- nents and subsystem. It is appropriate for the design of the six- port receiver and radar.

The SIW is a type of rectangular dielectric-filled waveguide that is synthesized in planar substrate with arrays of metallic vias to realize bilateral edge walls, and its transitions with planar structures such as microstrip and coplanar waveguide (CPW) are designed and integrated on the same substrate. In this case, the planar and nonplanar structures can be integrated within the same planar platform, which leads to the design and develop- ment of low-cost millimeter-wave integrated circuits (ICs) and systems [12].

The prototype of the SIW six-port circuit is shown in Fig. 3. The circuit is fabricated on a Rogers RT/Duroid 5880 lami- nates substrate with . It consists of two SIW power dividers, two SIW 90 3-dB hybrid couplers, and some in-line phase shifters. SIW-to-microstrip transitions are also integrated in the circuit. Unlike the other six-port junctions [6], [9] for the direct receiver system, the proposed six-port structure is a true “six-port”

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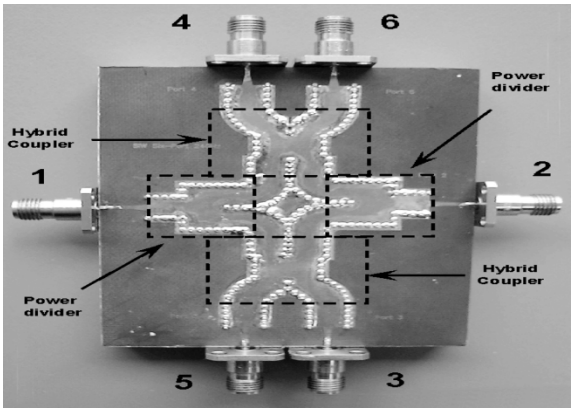
TABLE I
MEASURED AND SIMULATED S - PARAMETERS OF SIW SIX-PORT



S Parameters	Simulations [dB]	Measurements [dB]
S11	-42.7	-25.3
S22	-30.7	-21.0
S12	-39.2	-21.2
S13	-6.1	-6.6
S14	-6.0	-6.5
S15	-6.0	-8.0
S16	-6.1	-8.6
S23	-6.1	-8.3
S24	-5.9	-7.7
S25	-6.0	-7.3
S26	-6.0	-6.3

Fig. 3. Prototype of the SIW six-port junction (with K connectors).

without need for any external connecting terminals. Therefore, the structure is more compact at lower cost. The SIW six-port circuit is designed to operate over the frequency band of 22–26 GHz with the center frequency at 24 GHz.

The scattering parameters of the proposed SIW six-port circuit are summarized in Table I for the center frequency at 24 GHz. The six-port junction is simulated using Agilent's High-Frequency Structure Simulator (HFSS) 5.6, the simu- lation model includes SIW power dividers, SIW couplers, SIW phase shifters, and SIW-to-microstrip transitions. All the SIW components are modeled using the equivalent rectangular waveguide with effective width. Considering the time efficiency of simulation, the K connectors are not included in the HFSS simulation model, while the measurement results naturally involve effects of the K connectors at each port. It can be found that, at the center frequency, the reflection coefficients $S11$ and $S22$ are less than 21 Db and the

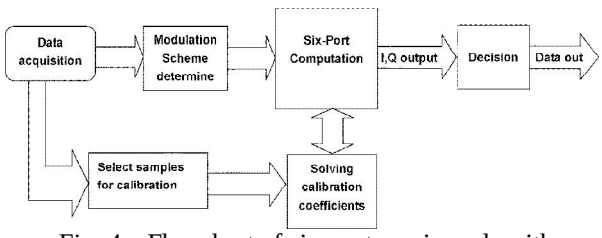


Fig. 4. Flowchart of six-port receiver algorithm.

isolation between the RF and LO ports ($S12$) is less than 21 dB. The transmission coeffi- cients are close to the theoretically predicted value (6 dB). The measured transmission losses are higher than the simulated counterparts, which might be partly because of the effects of K connectors in the measurement, and the offset of metallic holes location restricted to the fabrication limitation.

IV. RECEIVER ALGORITHMS

For an SDR receiver platform, the DSP computation algo- rithms and calibration methods are crucial. Fig. 4 shows the al- gorithm flowchart of the SDR six-port receiver. After the data acquired from the antenna, some samples are selected for cal- ibration. After calibration, the six-port calibration coefficients can be generated, the coefficients are then used in six-port com- putation to calculate the in-phase and quadrature (I-Q) data. Fol- lowing a decision algorithm,

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the signals are thus demodulated. This process is a universal demodulation algorithm for six-port receivers. Most calibration algorithms proposed for six-port reflectome- ters (SPRs) are based on the physical calibration method [13]. This method is accomplished simply by measuring a number of (usually at least nine) arbitrary, but different external physical terminations at input ports. However, for a wireless receiver, this physical calibration method is entirely impractical. It is, there- fore, necessary to develop a calibration method free from any external connection. As an application for a direct receiver, online six-port calibra- tion technologies were under development over the past years. Some calibration algorithms have been proposed. In the pro- posed receiver platform, a real-time six-port calibration method [14] is adopted and the demodulation results for different mod- ulation schemes are analyzed. For the six-port receiver, the ratio of amplitude, frequency, and phase between the LO signal (port 1) and RF signal (port 2) can be calculated from the power output at the other four ports with the complex constants known by calibration procedures. For a six-port receiver circuit, normally the leakage of the re- ceived signal to the LO reference port is small and may be ne- glected. In this case, the relationship between the output data of the SPR and the three power ratios of the detectors of the six-port become linear, and can be expressed as follows:

$$X_i=A_xp_1+A_{x2}p_2+A_{x3}p_3+C_x \quad \text{------- (1)}$$

$$Y_i=A_yp_1+A_{y2}p_2+Ay_3p_3+Cy \quad \text{------- (2)}$$

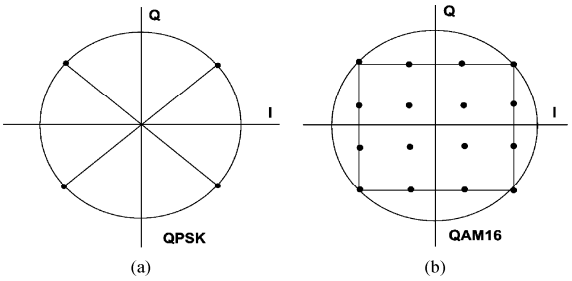

Fig. 5. Signal constellations for: (a) QPSK and (b) QAM16 modulation.

TABLE II
DEMODULATION RESULT FOR QPSK SIGNAL

Input	Output
1∠45°	1.0210∠46.75°
1∠135°	0.9614∠139.42°
1∠225°	1.0312∠225.33°
1∠315°	1.0205∠315.32°

TABLE III
DEMODULATION RESULT FOR QAM16 SIGNAL

Input	Output
4.2426∠45°	4.1745∠47.22°
3.1623∠18.43°	3.1632∠18.87°
1.4142∠45°	1.2942∠43.55°
3.1623∠71.56°	3.1931∠72.69°
3.1623∠341.57°	3.1594∠340.95°
4.2426∠315°	4.3339∠314.18°
3.1623∠288.44°	3.1254∠288.51°
1.4142∠315°	1.4151∠312.32°
1.4142∠225°	1.4320∠230.10°
3.1623∠251.56°	3.1215∠254.32°
4.2426∠225°	4.2713∠224.33°
3.1623∠198.43°	3.1922∠202.12°
3.1623∠108.44°	3.1882∠104.84°
1.4142∠145°	1.3677∠144.24°
3.1426∠161.57°	3.0657∠165.89°
4.2426∠145°	3.9823∠140.37°

where X_i and Y_i are the calculated output data, where as A_{xj},A_{yj} (j=1,2,3) and are calibration parameters be determined. p_1 p_2 and p_3 are power ratios at the output detectors of the six-port.

The simulated demodulation results of the SIW six-port junc- tion for quadrature phase-shift keying (QPSK) and 16 quadra- ture amplitude modulation (QAM16) schemes (Signal constel- lations shown in Fig. 5) are given in Tables II

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and III. With the use of MATLAB 6.5 for six-port computation, the demodulation results show that the receiver has accuracy at 5 in phase and 0.4 dB in amplitude for QPSK and QAM16 modulations.

In certain cases, for example, for some modulation scheme, the demodulation signal can be extracted directly from the re- lationship of power detectors output signal level. Therefore, the calibration procedure can be omitted and the demodulation al- gorithm could be simplified [9].

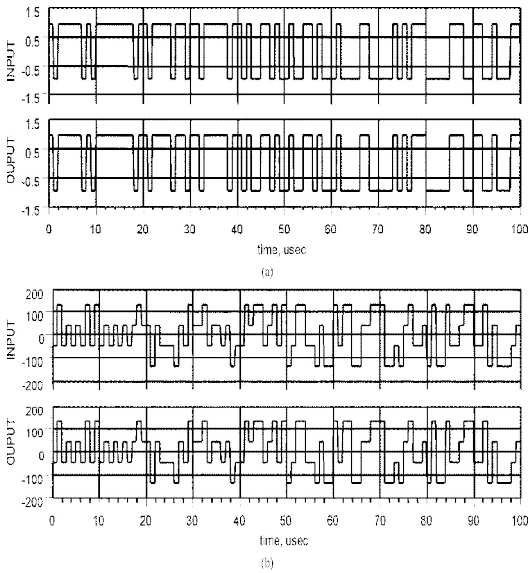

Fig. 6. Input and output waveforms of QPSK signals (a) Signal amplitude. (b) Signal phase.

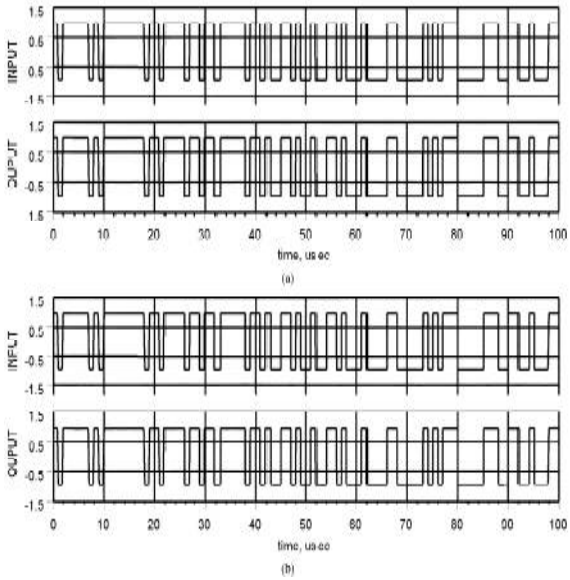

Fig. 7. Input and output waveforms of QAM16 signals. (a) Signal amplitude.

(b) Signal phase.

V. TEST RESULTS

Within the operating frequency band of the receiver (22–26 GHz), two modulation schemes (i.e., QPSK, QAM16) are selected to test performances of the proposed SDR re- ceiver. System-level simulation is made using HP-ADS and MATLAB-Simulink, and the bit error rate (BER) measurement results of the proposed receiver platform are also presented.

The simulated input and output amplitudes and phases of QPSK signals are given in Fig. 6. The INPUT is pseudorandom bit sequence QPSK signals at the input of the vector modulator. The OUTPUT is the same bit sequence, which is demodulated after six-port computation and decision. It can be seen the input signals and output signals are exactly the same, which confirms the operating principle of the proposed SDR receiver.

The simulated input and output amplitudes and phases of QAM16 signals are given in Fig. 7. In the same way as that of the QPSK signal in Fig. 6, the INPUT is a pseudorandom bit sequence QAM16 signal and the OUTPUT is the demodulated signal after six-port computation and decision. The input and output signals are matched very well.

Figs. 8 and 9 show the simulated output signal constellations for both QPSK and QAM16 with various signal-to-noise ra- tios (SNRs). A white noise is added to the input signal and the output signal constellations are presented in Fig. 8(a)–(c) for the QPSK signal with SNR equal to 25, 10, and 5 dB, respectively. Demodulation results (after decision algorithms) are presented in Fig. 8(d). Fig. 9(a)–(c) shows the QAM16 signal with SNR equal to 30, 15, and 8 dB, respectively. Demodulation results (after decision algorithms) are presented in Fig. 9(d). It is found that the output constellation is definitely stable. The signal is correctly demodulated if the SNR has an acceptable value.

The block diagram of the BER measurement setup is de- scribed in Fig. 10. A 1-Mbit/s pseudorandom bit sequence is generated from an Anritsu MP1630B BER analyzer and the signal is then fed to vector signal modulator for modulation. QPSK/QAM16 modulated signals and reference signals are

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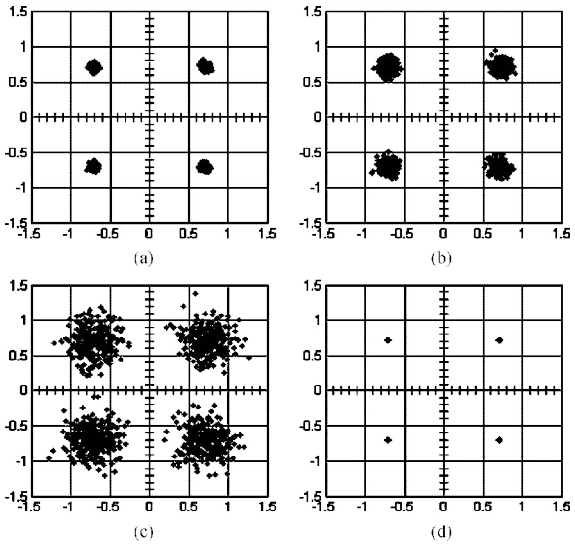

Fig. 8. Simulated output signal constellations for QPSK with different SNR.

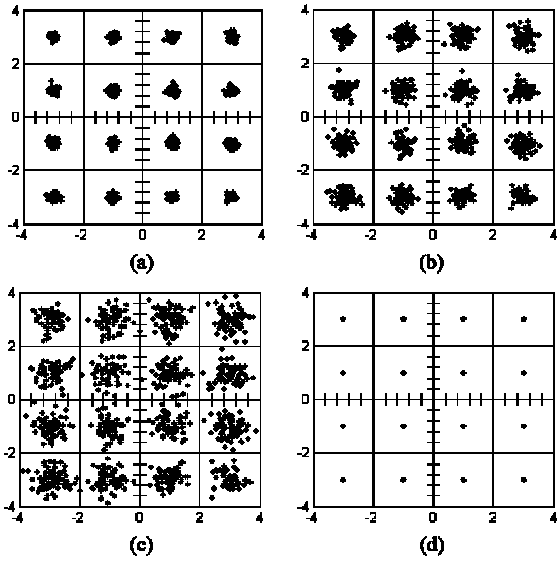

Fig.9.Simulated output signal constellations for QAM16

generated using an HP-8782B vector signal modulator. The modulated signals and reference signals are up-converted to 24 GHz by an Anritsu MG3694A signal generator and two SU26A21D sideband up-converters and then connected to the SIW six-port circuit. The output signals from the six-port circuit are sent to four Wiltron 75KC50 RF power detectors and the RF signals from the six-port output ports are then down-converted to baseband. The baseband signals from power detectors are then sent to two synchronized Altera FPGA DSP boards passing through a Texas Instruments Incorporated four-channel THS7002 programmable-gain amplifier evalua- tion module where the signals are 20 dB amplified and 20 MHz low-pass filtered. The signals are digitalized by four AD9433

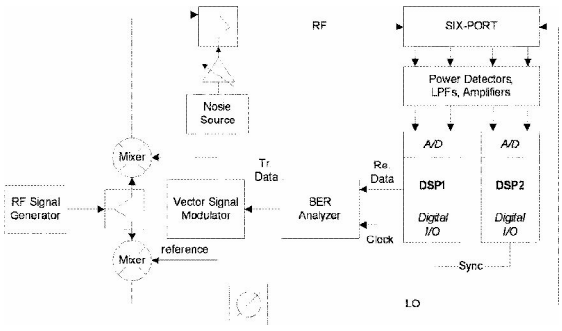

Fig. 10. Block diagram of BER measurement setup.

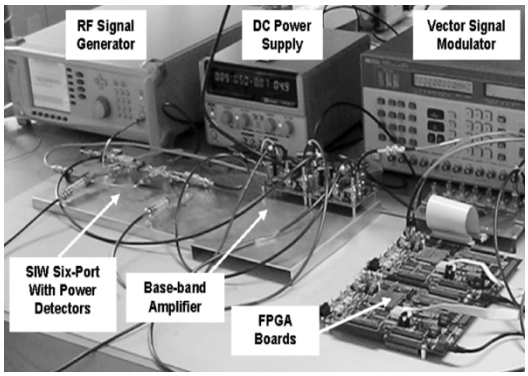

Fig. 11. Test-bed setup for receiver performance evaluation.

ADC integrated in two FPGA boards. The receiver algorithms are implemented in the two FPGA processors. The BER ana- lyzer receives the demodulated signal from DSP board1 and evaluates the BER values of the receiver system. An additional white noise generator Agilent N8975A is used for the adjacent signal interference or noise measurements. Fig. 11 shows a photograph of our test setup. It consists of one RF signal generator, one vector signal modulator, one dc power supply, one 3-dB power divider and two RF up-converters, an SIW six-port with RF power

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detectors, one baseband amplifier evaluation module board, and two FPGA development boards. Simulated and measured BER versus for the two mod- ulation schemes are presented in Figs. 12 and 13, where E_b is the average energy of a modulated bit and N_0 is the noise power spectral density. The QPSK and QAM16 signals are generated from a vector modulator without coding. The simulated BER re- sults are obtained from MATLAB-Simulink with carrier RF fre- quency from 22 to 26 GHz, considering the same conditions of power inputs and interferences. The measured BER curve is ob- tained at the center frequency (24 GHz) of the receiver platform. It can be seen that the simulated and measured BER curves are in excellent agreement. It is observed that the receiver

BER is less than 1E-6 for E_b/N_0 higher than 10.5 dB (QPSK) and 15 dB (QAM16).

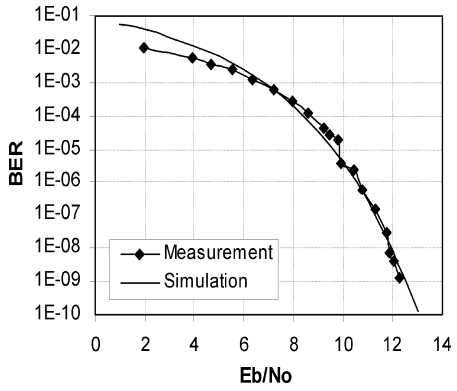

Fig. 12. Simulated and measured BER for QPSK signal.

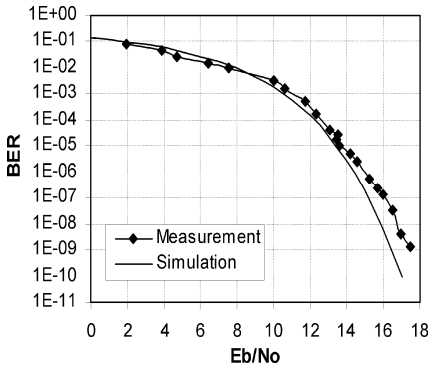

Fig. 13. Simulated and measured BER for QAM16 signal.

VI. CONCLUSION

This paper has presented recent results obtained on the anal- ysis of SDR technology in a direct six-port receiver designed for multimode RF and millimeter-wave communications. A six-port SDR receiver platform has been analyzed and imple- mented [15]. This platform adopts a new SIW six-port structure at the RF front-end, which realizes wideband direct down con- version for low-cost and mass-producible SDR applications. Based on the six-port front-end, the demodulation algorithms have been designed and the demodulation results and BER performance of the SDR receiver for two different modulation schemes (QPSK, QAM16) have been described. The simula- tion and measurement results are very encouraging, showing a possible universal receiver solution for future software-defined radio applications in various wireless communication systems. Our current effort is to implement orthogonal frequency divi- sion multiplexing (OFDM) demodulation in this SDR receiver platform.

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