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Design and Implementation of Image Enhancement using Low Power VLSI

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ABSTRACT: To process and to capture the images we will be using the smart phones and other simple monitoring systems in this modern era of the technology. The limits will be there in some specific applications like low power,low areaor in any high performance.This shows how the image quality can be improvisied. As we all know,power consumption will play the major part in the processing images in most of the portable electronics. Here, In this work we are proposing the full adder in the fir filter with the less power consumption with better image quality.The concept is explained by the Xilinx tool and the less power is explained by the cadence tool. As we can see in the results the power is consumed. From this consumption, leakage power also reduced in the proposed full adder. The area, power ,timing is reduced in the proposed technology.

KEYWORDS: Contrast enhancement, Image processing, Datapath, VLSI and Low power.

I.INTRODUCTION

The process of altering the quality of any image is termed as the Image Enhancement. whereas, in the digital processing system it is enhance the digital data of an image with the assistance of computer. The digital image processing helps in maximising the clarity of an image and also the sharpness of an image, and enhancing the blurring of an image. Towards the information extraction and the further analysis, the details of the features of image is carried out.In 1960, the image enhancement has begun with a limited number of researchers who are analysing the digitised aerial photographs and airborne multispectral scanner data. In 1972, after the launch of the Landsat-1 the digital data of an image become broadly available for the sensing of remote applications. During those period, the theory and the implementation and the practice of both the digital computers and the digital image processing is apparently very high in the cost and also in there efficiency was very less compare to the other applications such as other than the image processing.

Nowadays, the admittance to low cost and the computer software and the hardware is common place for the source of the digital data of any image verified. We have some of the digital image sources which ranges from the airborne solid state camera, airborne scanner, scanning of the micro-densitometer and also the earth resource to the high resolution of the video camera.Digital image processing have very wide range of advantages and also it is one of the very wide ranging subject to study for fresher and also for the experience researchers and it also includes the procedures which are mathematically very complex to solve any digital data problems.

The central idea of the processing of the digital data is quite very simple, but if we try to solve that issue it will become a big problem to solve it. The procedure for dumping the digital data to the computer is that initially we need to import the digital data which we are taking it as input and it fed into the computer and then the computer will solve it.Because we already programmed the computer to manipulate the input data using the equations or the series of equations and then store the result in the computation for each pixel of an image.Low pass filtering and enhancement are the only two stages of Adaptive contrast enhancement. The increasing of the contrast around edges using Finite Impulse Response (FIR) or Infinite impulse response filters (IIR) is the Filtering of the image.This work illustrates the methods related to contrast enhancement are explained with low power VLSI architectures to reduce the power consumption.

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II.RELATED WORK

In the Existing method, the consumption of the power is so high for the computational circuits which is applied to the images. So, reducing the consumption of the power using the FIR filter for the process. The process will have the large stack length which results in the more power consumption. So, reducing the power in the proposed technology. Develop low power architectures based on Image Enhancement systems. In this Modern world the system on chip is demand fo the more power. The power consumption is increasing rapidly. If the semiconductor integration of the system continues to follow the Moore's law, the power density inside the chips will be one of the primarily design constraint for the process. A solution to this problem requires architectures which consume low power when compared to state of the art devices. So, from this we can reduce the power constraints of the proposed method.

III.IMPLEMENTATION

The methodology can be shown by the below diagram, where we will take input as an image for the process to be carried out. Then the image is passed to the matlab code to get respected results i.e enhanced image and the quality measurements of the taken input image and then it is passed to the HDL and the input vectors are carried out and then it is given for the ASIC(Application specific integration concept) analysis. The image which is taken from the test vectors are subjected to that ASIC for the analysis and then again to the matlab for the output vectors and then again to the matlab for the enhanced image and the quality measurements and the output is taken out.

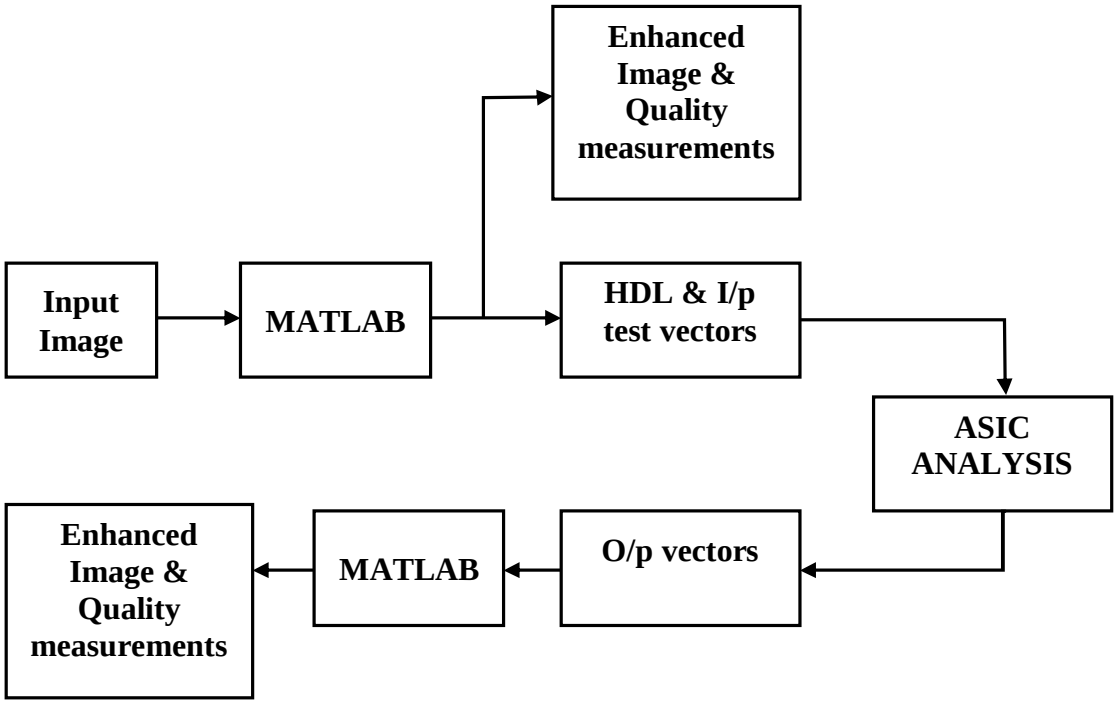

Fig.1: Implementation Methodology ([8])

Fig.1 represents the block diagram shows how the image can be enhanced through the implementation of the below filters which we proposing for the power consumption. The filter for the above implementation is showed in Fig.2

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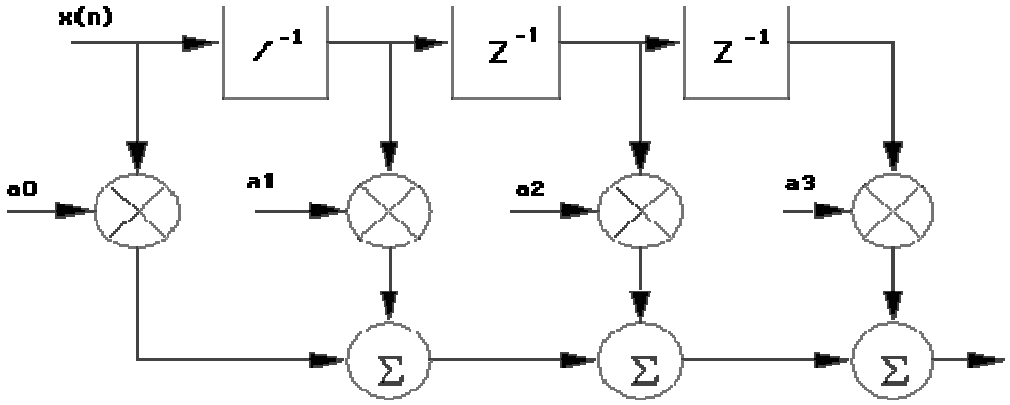

Fig.2: FIR filter

The filter which we designed for the purpose of the power consumption is shown in the above figure.the input is consists of the delays and also the multipliers and also the full adders.here we are rplacing the existing full adders with the proposed full adders.

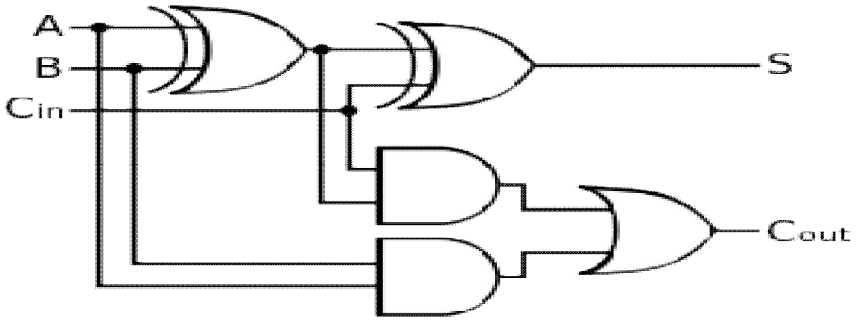

Fig.3:Existing Full adder

The above figure shows the existing full adder with respect to the filter which we are using for the image enhancement process.For the process of low consumption of power, area, timing we will be introducing the another full adder that is which we have shown below.

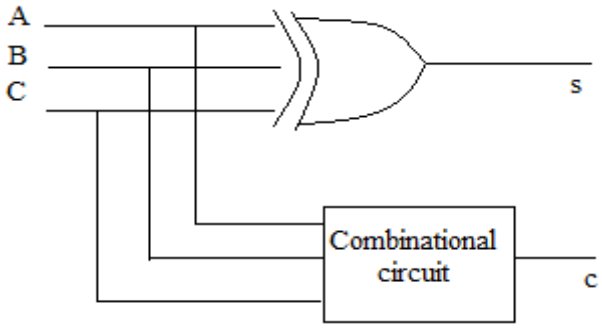

Fig.4:Proposed full adder

Fig.4 shows the proposed full adder for the process and then it is implemented in the cadence tool and the Xilinx for the better results of this proposed full adder.
The proposed full adder is shown in the above figure which consists of the combinational circuit which we can see in the below diagram. This proposed one is used in the filter for the consumption through the cadence tool to show it.

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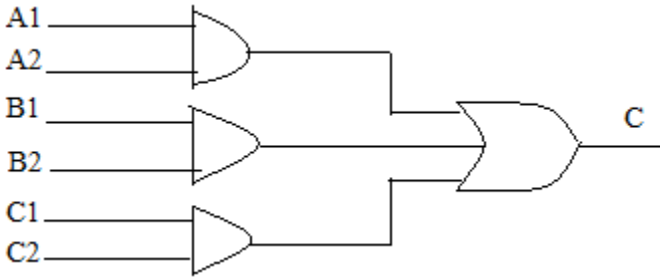

Fig.5: Combinational circuit

Fig.5 shows the combinational circuit, which is proposed in the full adder for this process. Where it consists of the above gats as shown in the diagram.

V. RESULTS

The results of the system is consists of two process i.e simulation and the synthesis.Initially we will simulate the proposed full adder of the fir filter in the Xilinx software tool and from that we will get the timing of the filter but we can see the power of the existing and the proposed full adder.Then we synthesis through the cadence tool to see the power consumption and the area of the existing and the proposed full adder.

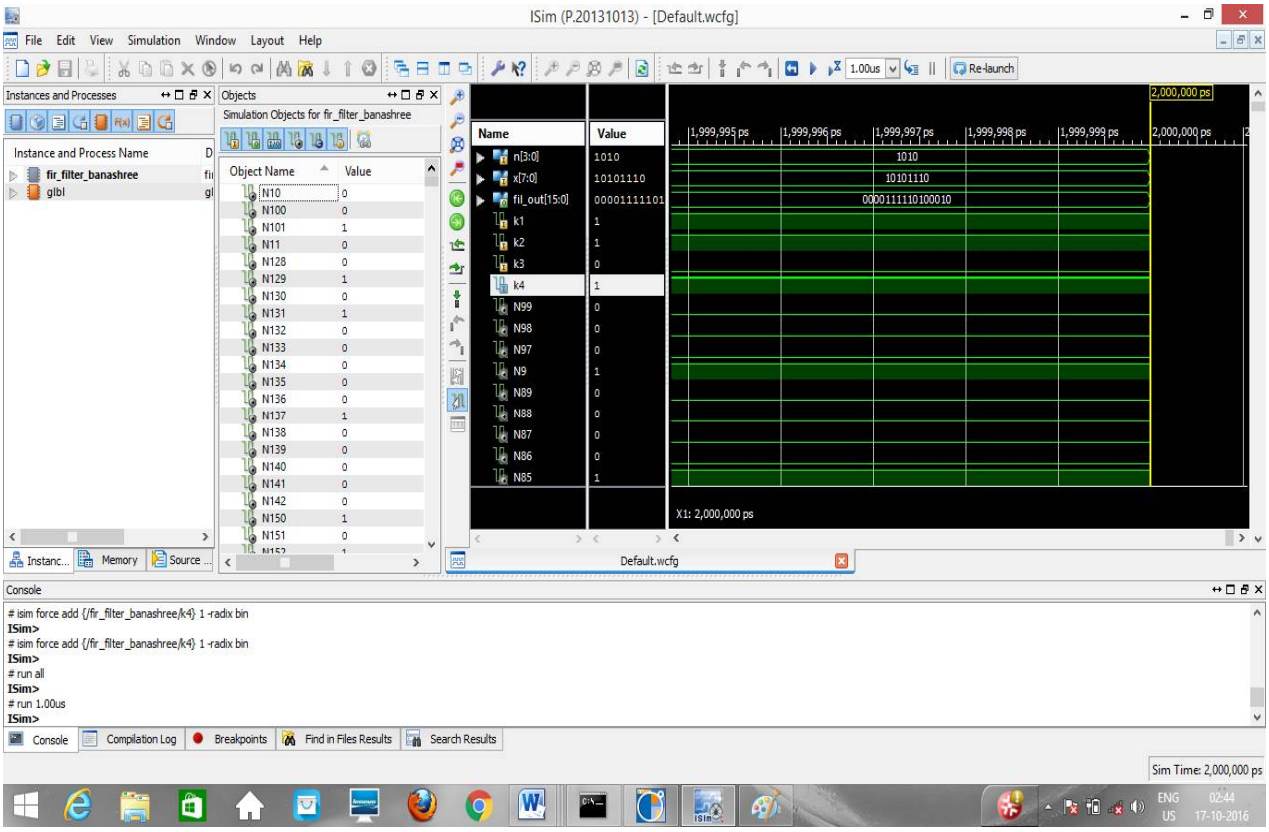

Fig.6:Screenshot of the simulation in the Xilinx

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The above screenshot shows simulation of the filter which we have proposed with the full adder.The input for the system has given and the output for the sum and carry has taken out.The synthesis of the system has given from the cadence tool which we have shown in the below table.

Results	Leakage power	Dynamic power	Total Power	Area	Timing
Existing	26470.162nw	429981.589nw	456451.751nw	6225	280F
Proposed	25134.849nw	305108.971nw	330243.819nw	5708	271F

Table 1.Report of the existed and the proposed system

VI.CONCLUSION

Here, in this paper we are mainly concentrating on the power consumption of the full adders which we are using for the fir filter for the reduction of it.Since we reducing the power, the other components like area, timing of the adders which we are using are also reduced for the better performance of the system.The simulation of the process is carried out by the Xilinx tool and the power report can be found in the cadence tool and it is shown in the above results.

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