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Design and Analysis of Improved Recycling Folded Cascode OTA with Gain and Phase Margin Enhancement

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ABSTRACT: In this paper, Gain boosted improved Recycling folded cascode Operational Transconductance Amplifier with phase margin enhancement architecture is described. The proposed Operational Transconductance Amplifier (OTA) is designed using cadence tool in 180 nm technology. This amplifier delivers an appreciably enhanced performance over that of conventional folded cascode. This is achieved by using previously idle in the signal path. This circuit achieves higher gain,unity gain bandwidth and Phase margin. The gain of the amplifier is enhanced by increasing the output impedance of the circuit with the addition of a cascoded gain stage which will further enhance the different parameters within the same area and power budget. A complete analysis of the circuit is presented in this thesis which shows how this circuit leads to a high gain and resistance at output. A brief comparison of different OTA architectures is described and the completed layout of the proposed OTA is also included.

KEYWORDS: OTA, Amplifiers, Gain, Phase Margin, Unity Gain Bandwidth, OTA architectures.

I. INTRODUCTION

In todays industry the low power and low voltage supply is becoming one of the important research area due to the developing market of battery operated mobile and portable electronic devices. The power consumption is becoming an important parameter as speed, gain and GBW. Operational Transconductance Amplifier (OTA) is an integral part of many analog and mixed signal systems. OTA is an amplifier whose differential input voltage produces an output current. The topology of OTAs plays an important role in the design of low power system. The design of OTA continues to face challenge as the supply voltage and transistor length scale down with each newer generation of CMOS technologies. To address the issue of power efficiency, proposed Recycling Folded Cascode (RFC) amplifier which recycles the tail current back to the input differential pair and boost the input transconductance to achieve large increase in unity gain frequency and moderate improvements in DC gain,phase margin and input referred noise. Taking into account this wide scale applicability of RFCs this particular topic is chosen as the area of research. The OTA is the most adaptable building block of analog processing system. Designing these building blocks in terms of power consumption, gain and gain bandwidth product effectively is still a challenging task. Operational Transconductance Amplifiers are mainly grouped into Single ended output OTAs and Differential ended output or Fully Differential OTAs .

II. OTA ARCHITECTURES

A. FOLDED CASCODE OTA (FC OTA)

Folded cascode OTA is mostly used architecture for its high gain and large signal swing. OTA is an amplifier,whose differential input voltage produces an output current[1],[2]. So, it is a Voltage Controlled Current Source (VCCS).

$$I_{out} = (V_{in+} - V_{in-}) \square g_m \quad (1)$$

where V_{in+} is the voltage at the non-inverting input, V_{in-} is the voltage at inverting input, g m is the transconductance of the amplifier. The output current is a function of input differential voltage and transconductance of the circuit. The gain is described by the product of effective transconductance and output impedance of the circuit[3],[4],[5].

$$A_o = g_{m,eff} \square R_{out} \quad (2)$$

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where Ao is the gain, R_{out} is the output impedance. Although the Folded Cascode (FC) OTA is providing a good improvisation in term of performance parameters like gain, GBW, output voltage swing, slew rate, power consumption as compare to a Two stage OTA and Telescopic Cascode OTA. The recycling technique has become prominent to improve the performance of conventional Folded Cascode OTA with the same area and power budget[6],[7].

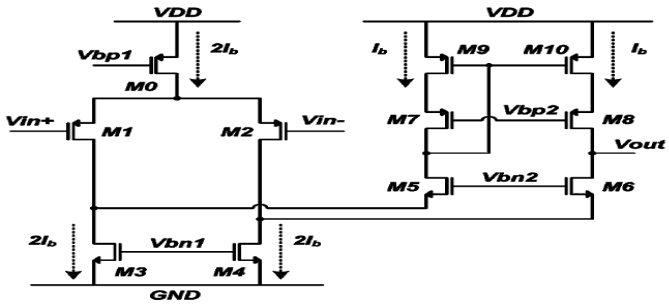

Fig 1: Folded Cascode OTA

B. RECYCLING FOLDED CASCODE OTA (RFC OTA)

In the conventional FC transistors M_3 and M_4 conduct the most current, and in many designs have the largest transconductance. However, their role is limited to providing a folding node for the small signal current generated by the input drivers M_1 and M_2 . To address this inefficiency, a modified FC is presented. The proposed modifications are intended to use M_3 and M_4 as driving transistors[8]. First, the input drivers M_1 and M_2 are split in half to produce transistors M_{1a} , M_{1b} , M_{2a} and M_{2b} , which now conduct fixed and equal currents I_b /2. Next, M_3 and M_4 are split to form the current mirrors M_{3a} : M_{3b} and M_{4a} :M_{4b} with a ratio of K:1. The cross-over connections of these current mirrors ensure the small signal currents added at the source of M_5 and M_6 are in phase. Finally M_{11} and M_{12} are sized similar to M_5 and M_6 , and their addition helps maintain the drain potentials of M_{3a} : M_{3b} and M_{4a} : M_{4b} equal for improved matching. The amplifiers transconductance, Gm , by Finding the short circuit current at the output with respect to the input. The results for RFC and FC.

$$G_{mRFC} = g_{m1a}\,[(1 + K)] \quad (3)$$

$$G_{mFC} = g_{m1} \quad (4)$$

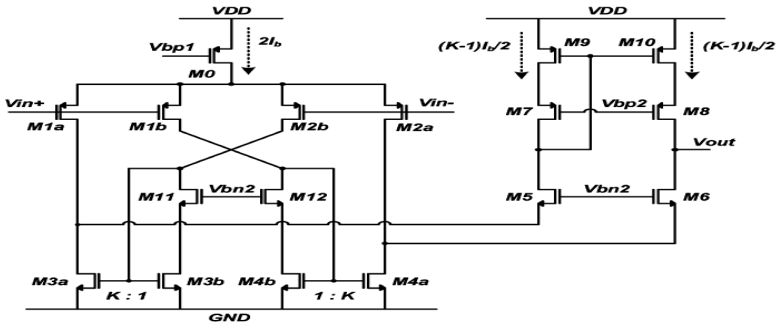

Fig 2: Recycling Folded Cascode OTA

By taking into account that M_1 is twice the size of M_{1a} and conducts twice the amount of current[9] (ie, $g_{m\,1} = 2g_{m1a}$) , and substituting for the value of K, the transconductance of the RFC is demonstrated to be twice that of the FC for the same power consumption. It shows that the RFC has twice the gain bandwidth (GBW) as that of the FC for the same power, and consequently twice the speed. The low frequency gain of OTAs is frequently expressed as the product of the small signal transconductance Gm , and low frequency output impedance,R_o. It was demonstrated that $G_{mRFC} = 2G_{mFC}$, which results about an 6 dB gain enhancement for the same output impedance. However, is also enhanced over . The expressions for R_{oRFC} and R_{oFC} are

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$$R_{oRFC} = g_{m6} r_{ds6} (r_{ds2a} \| r_{ds4a}) \| g_{m8} r_{ds8} r_{ds10} \quad (5)$$

$$R_{oFC} = g_{m6} r_{ds6} (r_{ds2} \| r_{ds4}) \| g_{m8} r_{ds8} r_{ds10} \quad (6)$$

The gain enhancement seen in R_{oRFC} is attributed to the increased r_{ds} of M_{2a} and M_{4a} ,as they conduct less current compared to their counterparts M_2 and M_4 of the FC. Therefore, an overall low frequency gain enhancement of 8 to 10 dB can be seen in the RFC compared to the FC. This added gain has two fundamental benefits. First one, static settling errors are reduced because of the increased gain. Second one, the power supply rejection ratio (PSRR) of the RFC is improved over its FC counterpart.

C. IMPROVED RECYCLING FOLDED CASCODE OTA (IRFC OTA)

To improve the swing of the signal at the current mirror nodes X + and X − , the DC and AC path are separated in IRFC proposed is shown in Fig 3. To achieve this, the transistors M_{11} ,M_{3b} ,M_{12} and M_{4b} are divided into two parts M_{11a}, M_{11b}, M_{3b1}, M_{3b2} and M_{12a}, M_{12b}, M_{4b1}, M_{4b2} respectively. The paths M_{11b}, M_{3b2} and M_{12b}, M_{4b2} have high impedance. The paths M_{11a}, M_{3b1} and M_{12a}, M_{4b1} and have low impedance. The small signal current flows through the low impedance path. The ratio of DC current flowing through the high impedance and low impedance paths is a:b and the transconductance of M_{11a}, M_{3b1} is scaled by a where a < 1. The signal flowing through the current mirror node becomes larger compared to that of the RFC because of the increase in the resistance of the small signal path.

The recycling and improved recycling techniques is used to boost the transconductance of OTAs by multiple times and achieve very high GBW values in power efficient way. However, DC gain is not enhanced by similar amount on dB scale.

The output impedance R_{out} of the IRFC OTA is given by

$$R_{outIRFC} = g_{m5} r_{05} (r_{01a} \| r_{03a}) \| g_{m7} r_{07} r_{09} \quad (7)$$

The Gain A_v of the IRFC OTA is given by

$$A_v = g_{m1a} (k/a + 1) \approx g_{m5} r_{05} (r_{01a} \| r_{03a}) \| g_{m7} r_{07} r_{09} \quad (8)$$

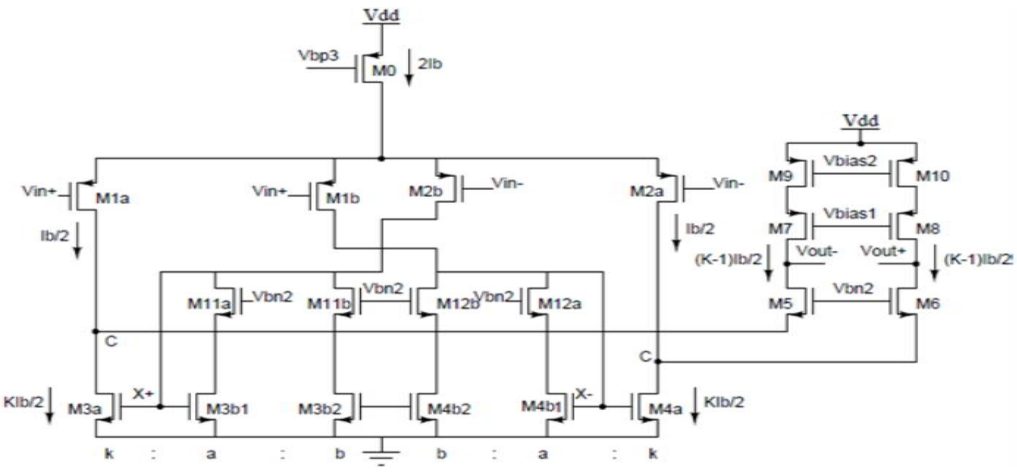

Fig 3: Improved Recycling Folded Cascode OTA.

III. GAIN BOOSTED IRFC OTA WITH PHASE MARGIN ENHANCEMENT

The ineffectiveness of folded cascode OTA was overcome by recycling folded cascode OTA in which we are reusing or recycling the devices or currents to perform additional task speed but the voltage swing is reduced at the output. And also the multistage amplifiers may be used for high gains but such kind of high gain amplifiers are generally difficult to compensate. So we have to implement some compensation techniques to achieve the stability and significant phase margin. So here a Single Miller Compensation Nulling Resistor (SMCNR) is used in which we put a compensation capacitor between input and output nodes of the second inverting stage of the amplifier and the dominant pole is created due to Miller feedback and it will helps us to increase the phase margin and to achieve stability. In the proposed GB RFC OTA the gain is enhanced by improving the output impedance because the output resistance increases in proportion to the decrease in bias current. So it make the circuit power efficient to increase the output

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impedance by lowering the currents. The cascode gain boosting stage is attached to enhance the performance parameters. The output impedance R_{out} of the IRFC OTA is given by

$$R_{outIRFC} = g_{m5} r_{05} (r_{01a} \| r_{03a}) \| g_{m7} r_{07} r_{09} \quad (9)$$

The output impedance of GB-IRFC is given by

$$R_{outGB-IRFC} = g_{m23} r_{023} r_{024} (R_{outIRFC}) \quad (10)$$

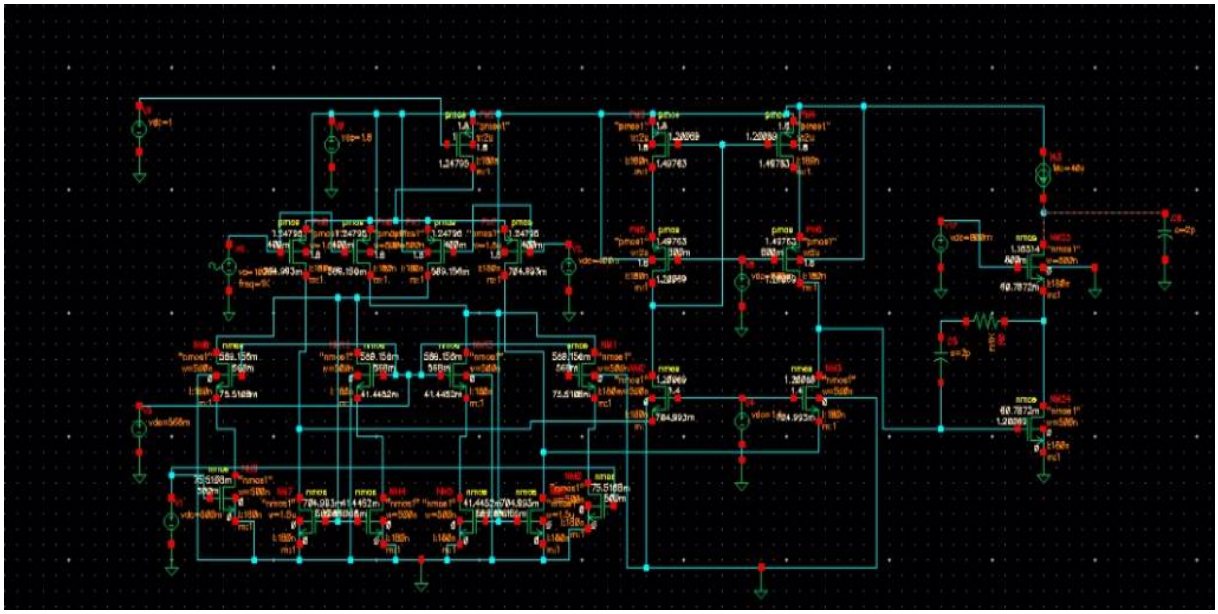

Fig 4: GB-IRFC OTA with phase margin enhancement

A. GAIN BOOSTING

In the IRFC operational transconductance amplifier the gain is enhanced by increasing the output impedance of the circuit by providing a cascoded gain stage. The higher gain often causes to instability so to achieve the stability and better phase margin the miller compensation is used. In order to increase the gain either the Transconductance or the output impedance can be enhanced. But the transconductance increases as square root of increase in bias current which cause to increase in power consumption[12],[13].

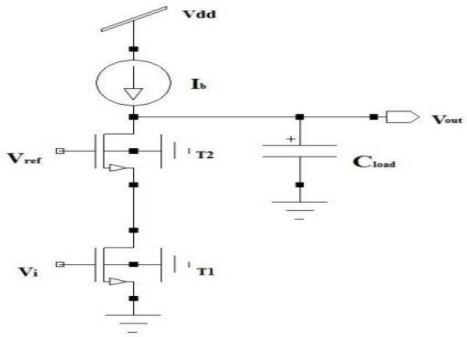

Fig 5: Gain boosting stage

The cascoded structures as shown above are widely used to boost the gain. The output voltage V_{out} is given by

$$\Delta V_{out} = \Delta I_o R_{out} \quad (11)$$

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Where R_{out} is the output impedance of the whole circuit and is given by

$$R_{out} = (g_{m2} r_{02} + 1) r_{01} + r_{02} \quad (12)$$

$$R_{out} = g_{m2} r_{02} r_{01} \quad (13)$$

It produces the following expression of DC gain A_o

$$A_o = g_{m1} r_{01} (g_{m2} r_{02} + 1) \quad (14)$$

B. MILLER COMPENSATION

However the multistage amplifiers may be used for high gains but such kind of high gain amplifiers are generally difficult to compensate. So we have to implement some compensation techniques to achieve the stability and significant phase margin. So here Single Miller Compensation Nulling Resistor (SMCNR) is used in which we place a compensating capacitor in between the input and output nodes of the second inverting stage of the amplifier and the dominant pole is created due to Miller feedback and it will helps us to increase the high midband gap without affecting its dc response[14].

Sometimes if the transistor gain of second stage increases the dominant poles decreases and non dominant pole increases and poles are split aside to stabilize the amplifier but this method also introduces a Right Half Plane (RHP) zero which causes a negative phase shift and stability decreases. This zero arises because of the direct feed through of input to output through Miller capacitor. So in order to increase the phase margin the RHP should be eliminated, a lead compensation technique in which the nulling resistor in series with the compensation capacitor is used to increase the impedance of feed through path.

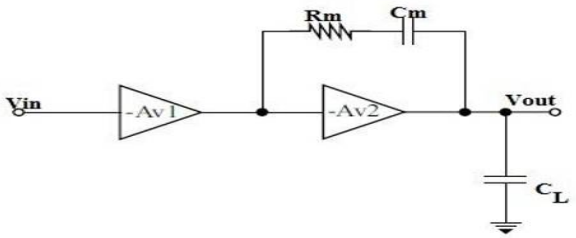

Fig 6: SMCNR

IV. RESULT AND DISCUSSION

A. FOLDED CASCODE OTA

While analyzing gain and phase margin the following results are found.

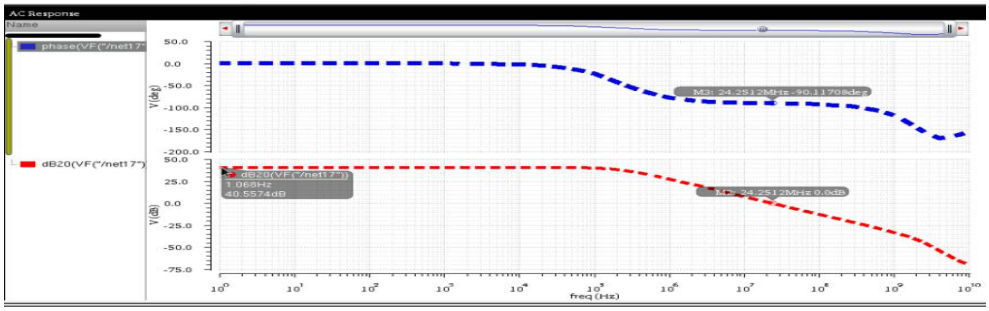

Fig 7: Output waveform of Folded Cascode OTA

From analysing the output waveform of the folded cascode circuit shown in Fig 7, it got a gain of 40.5 dB and a phase margin of 89.785 degree.

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B. RECYCLING FOLDED CASCODE OTA

From analysing the output waveform of the Recycling folded cascode circuit shown in Fig.8, it got a gain of 52.79 dB and a phase margin of 82.04 degree.

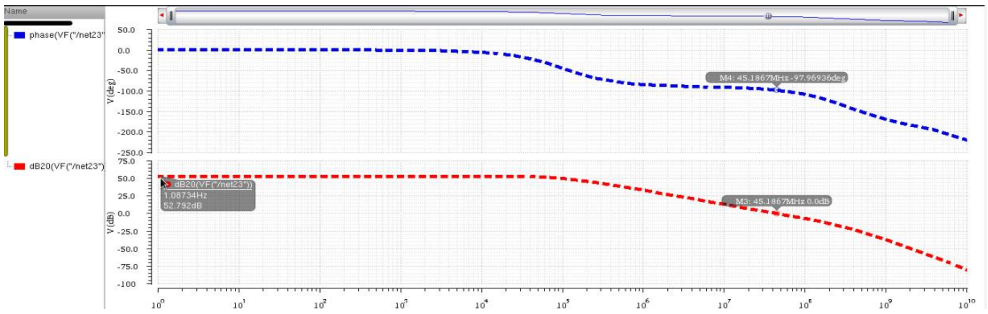

Fig 8: Output waveform of Recycling Folded Cascode OTA

C. IMPROVED RECYCLING FOLDED CASCODE OTA

From analysing the output waveform of the Improved Recycling folded cascode circuit shown in Fig.9, it got a gain of 61.97 dB and a phase margin of 81.37 degree.

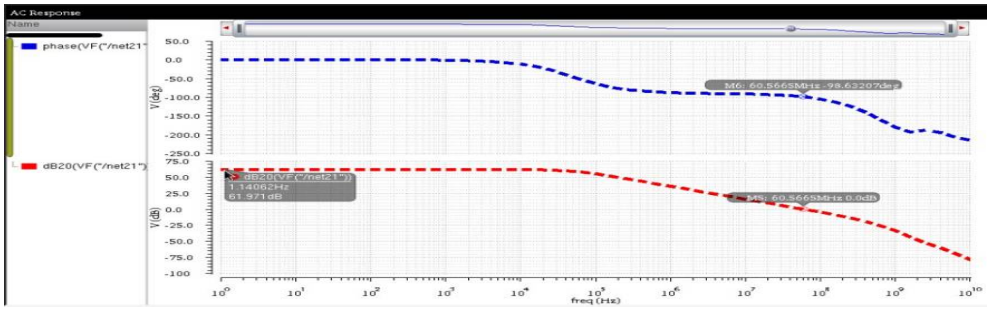

Fig 9: Output waveform of IRFC OTA

D. GB-IRFC OTA

From analysing the output waveform of the Gain boosted Improved Recycling folded cascode with phase margin enhancement circuit shown in Fig.10, it got a gain of 71.168 dB and a phase margin of 84.05 degree. The layout of the circuit is shown in Fig.11. The GB-IRFC OTA showing significant performance over the existing configurations like FC , RFC , IRFC. The performance comparison is shown in the Table I.

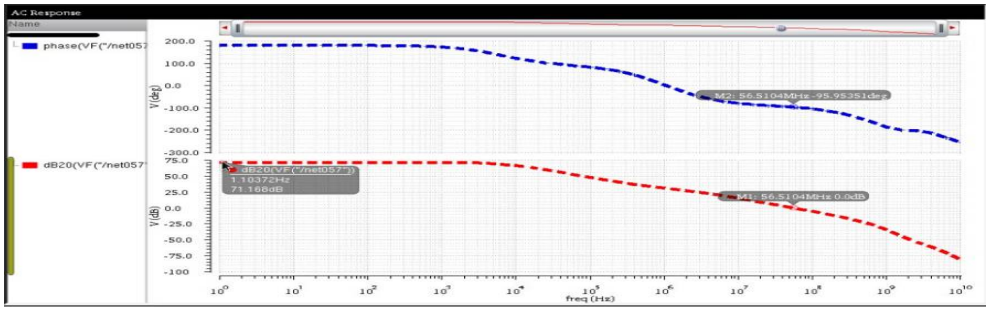

Fig 10: Output waveform of GB-IRFC OTA with phase margin enhancement

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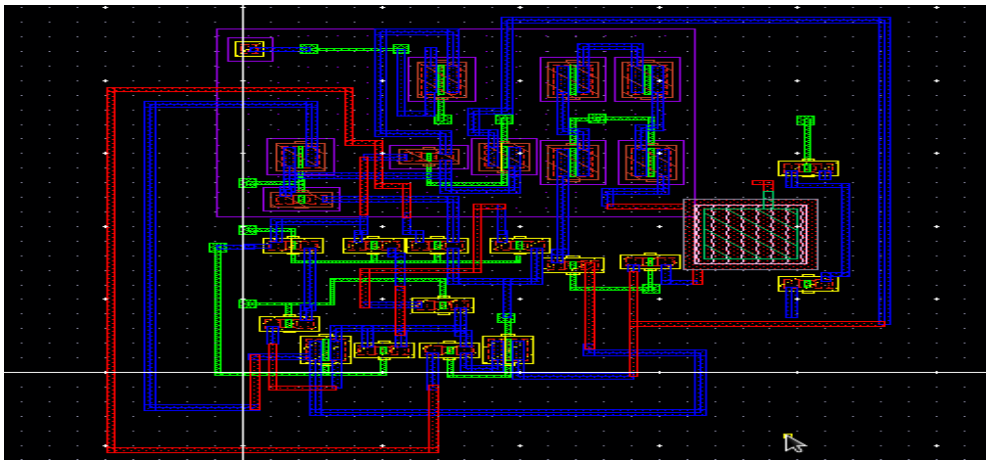

Fig 11. Layout of GB-IRFC OTA with phase margin enhancement

Parameter	FC	RFC	IRFC	GB-IRFC
Gain(dB)	40.55	52.79	61.971	71.168
Phase Margin(deg)	89.785	82.04	81.37	84.05
GBW (MHz)	24.251	45.186	60.56	56.51
Supply Voltage(V)	1.8	1.8	1.8	1.8
capacitive load(pF)	2	2	2	2

Table I. Performance Comparison

V. CONCLUSION

It has been demonstrated that the gain-boosted recycling folded cascode amplifier with phase margin enhancement achieves superior performance when compared to three other topologies namely Folded Cascode (FC), Recycling Folded Cascode (RFC) and Improved Recycling Folded Cascode (IRFC) OTAs. For a better comparison, the four amplifiers have been realised in gpdk 180 nm CMOS technology process using the same power and area budget. The output impedance of the circuit is enhanced by adding a cascode gain stage at the output. A significant increase in Gain and GBW is achieved within the same area and power budget. The Miller compensation technique is used to increase the phase margin of the circuit.

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