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Analysis and Design of Capacitive DAC Array Switching Scheme for SAR ADC in Low Power Applications

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ABSTRACT: Successive-approximation ADCs (SA-ADCs) have found a wide range of applications requiring low speed and moderate resolution, very-high speed and low resolution or even high speed and high resolution Low-power SA-ADCs have been widely used in low-speed biomedical applications with a limited power budget.Several attempts have been reported in order to reduce the power consumption of the ADC with an emphasis on the employed capacitive DAC. In this paper, both the capacitive digital-to-analog converter (DAC) and the comparator are modified from the typical structure. The conventional structure of an SA-ADC, consists of a sample-and-hold (S/H) circuit, a comparator, a successive approximation register (SAR), and a digital-to-analog converter (DAC).Among them DAC has greater importance, which consumes major power in the ADC module.So by careful designing of DAC module its possible to reduce the power consumption to a great extend. By modifying the existing Conventional DAC architecture, ,its found that the power consumption of the DAC is significantly reduced.In the exsiting Conventional DAC power consumption is found to be about 12mW. But in modified architecture power consumption is reduced to 7mW.So it is stated that by using modified DAC module its possible to work the ADC in low power applications

KEYWORDS: ADC, DAC, Comparator, Switch, DAC architectures.

I.INTRODUCTION

Successive approximation analog-to-digital converters (SA-ADCs) have recently become very attractive in low-power moderate-resolution/moderate-speed applications such as wire-less sensor nodes or implantable biomedical devices due to their minimal active analog circuit requirements and low power consumption.[2]

The conventional structure of an SA-ADC,consists of a sample-and-hold (S/H) circuit, a comparator, a successive approximation register (SAR), and a digital-to- analog converter (DAC).This is shown in Fig. 1. From the diagram itself its clear that a ADC module has four main components, among them DAC has greater importance because the major power consumption of this ADC module is due to the DAC. So a special attention should be taken while designing the DAC module.

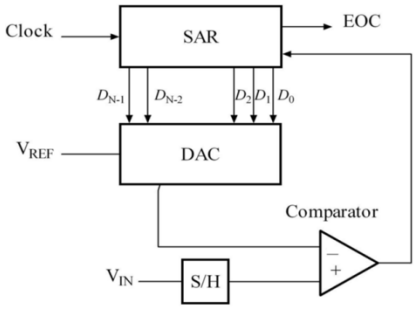

Fig.1 SAR-ADC

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II.DAC ARCHITECTURES

The DAC required in the SA-ADC can be realized in various ways; e.g., capacitor-based DAC , switched-current DAC or R-2R ladder DAC.Among these architectures, the capacitor-based DAC has become more popular because of its zero quiescent current. Furthermore, in most technologies resistor mismatch and tolerance are greater than capacitor mismatch and tolerance. Several structures have been proposed to implement capacitor based DACs for SA-ADCs for both radix-2 and non-radix-2 architectures[10] [11]. In radix-2 capacitive array DACs, the digital circuit is simple, yet the matching of capacitors in the array is essential; on the other hand, in non-radix-2 architectures, the matching requirement in the capacitive array can be more relaxed but the digital circuit has a larger complexity.Several methods have been proposed in literature for implementation of radix-2 capacitive-array DACs, such as conventional binary-weighted capacitive-array DAC, binary-weighted capacitive array DAC with attenuationcapacitor , split binaryweighted capacitive-array DAC , SA-ADC with dual binary-weighted capacitive-array DAC [5] and C-2C capacitive-array DAC. All of these radix-2 capacitorarray architectures are based on three fundamental structures, i.e., conventional binary-weighted (CBW) capacitive array, binary-weighted capacitive array with attenuation capacitor (BWA) and split binary-weighted (SBW) capacitive-arrayDAC.As the energy consumed in charging the capacitors of these capacitor-based DACs is one of the main sources of energy consumption in the ADC.

ADC energy consumption, the main purpose of this paper is to present a comprehensive yet accurate analysis about the power consumption of the capacitive-array DACs due to capacitor switching supplied by the reference voltage source. In order to be able to analyze the power consumption of these structures, one should note that the capacitor switching power consumption is directly proportional to the size of the unit capacitor in the capacitive array[13] [14]. In practice, the smallest possible value for unit capacitor is determined by one of the followings: kT/C noise requirement, capacitor matching, design rules and the size of the parasitic capacitances . The capacitor matching and parasitic capacitances which directly affect non-linearity parameters of the ADC such as integral non-linearity (INL) and differential non-linearity (DNL) are the dominant factors for medium resolutions. Therefore, any comparison between different architectures from power consumption viewpoint can-not be fairly accomplished without comparing their linearity performances. The standard deviations of the INL and the DNL determine the parameters of INL-yield and DNL-yield, important in many applications[9].

A. CONVENTIONAL BINARY WEIGHTED DAC(CBW DAC)

The conventional structure of an SA-ADC with a binary-weighted capacitive-array DAC, as shown below, consists of a S/H circuit, a comparator, an SAR, and a binary-weighted capacitive-array DAC.

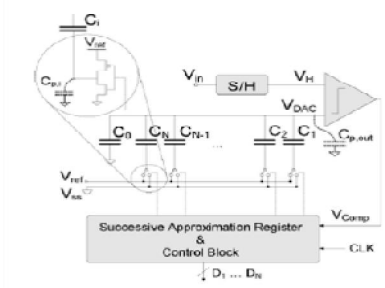

Fig.2 CBW DAC

In the sampling phase, the analog input signal is fed through a S/H circuit, so that the sampled voltage does not change during the entire conversion phase[13]. In the conversion phase, during the first clock cycle, the MSB capacitor is connected to with the remaining capacitors connected to ground. The comparator determines if the sampled voltage (V_H) is larger or smaller than the output voltage of the capacitive-array DAC (i.e. V_{DAC} that equals $0{:}5V_{ref}$ in this clock cycle). Therefore, the MSB bit (D_1) is determined and stored in the SAR. During the second clock cycle, (C_2) isconnected to V_{ref} ; C_1 is connected to D_1V_{ref} (C_1 connected to ground if D_1=0, else C_1 remains connected to V_{ref})and the remaining capacitors will be connected to ground. Therefore, V_H iscomparedwithV_{DAC}=0.25*V_{ref} (if D_1= 0) or V_{DAC}

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= 0:75 V_{ref} (if D_1=1) and the second significant bit(D_2) is determined. This procedure is repeated until all Nbits are found.
The power consumption of an SA-ADC due to capacitor switching is proportional to the total capacitance of the capacitive-array DAC. In addition, the major speed limitation of an SA-ADC is often related to the RC time constant composed by the value of the capacitance of the capacitor array and the resistance of the reference ladder and switches. On the other hand, in the CBW structure, the total capacitance rises exponentially with the ADC resolution leading to an exponential increase in the power consumption and RC time constant.

B. BINARY-WEIGHTED CAPACITIVE ARRAY WITH ATTENUATION CAPACITOR (BWA) DAC

One of the most popular solutions is to employ an attenuating capacitor in the binary-weighted capacitor array to split the capacitor array[5] into K MSBs and m=N-K LSBs. Therefore, the values of the capacitors related to the MSBs are decreased by a factor of 2^m in comparison to the conventional architecture.
Thus, the power consumption and the RC time constant of DAC will be decreased. Note that the switching sequence of this architecture is similar to that of the CBW structure.

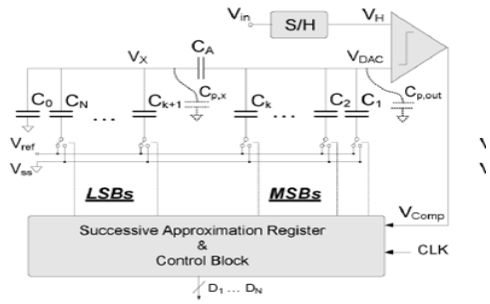

Fig.3 BWA DAC

C. SPLIT BINARY-WEIGHTED (SBW) CAPACITIVE-ARRAY DAC

Another structure and switching sequence has been proposed for the capacitive-array DAC to reduce the power consumption due to capacitor switching is Split binary weighted capacitive array. The structure is a split binary-weighted (SBW) capacitive-array DAC is shown.

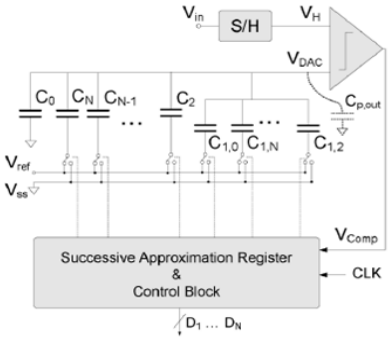

Fig.4 SBW DAC

In this structure, the MSB capacitor of the CBW architecture has been realized as a capacitive binary-weighted sub-array (to be called MSB sub-array) exactly similar to the rest of the main array[1]. The switching algorithm of this structure is modified as follows. In the first clock cycle of the conversion phase, all capacitors of the MSB sub-array are connected to Vref and the other capacitors are connected to ground. Hence, the input sampled signal(VH) is compared with Vdac and the result is stored in the SAR. In the second clock cycle, based on D1 , the output of the DAC must be increased to 0:75Vref if D1=1(up transition) or decreased to 0:25Vref if D1=0 (down transition). In the up transition,

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similarly as for the CBW structure, the main sub-array remains connected to Vref and also C2 is connected to Vref . But the difference inthe switching sequence appears in the down transition where, in the CBW structure, all capacitors of main sub-array or are discharged to ground and C_2 is connected to V_{ref} but in this modified structure, half of the MSB sub-array capacitors are connected back to ground leaving other capacitors of the MSB sub-array connected to V_{ref} and rest remains unchanged. And this procedure is repeated until all N bits are found.

III.SIMULATION RESULTS

A. CBW DAC

While analysingtiming and power the following results are found.

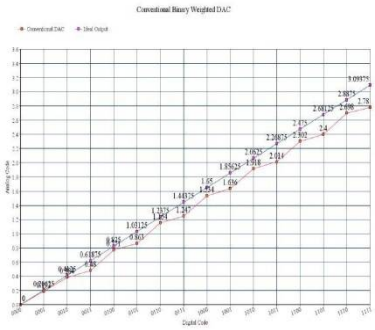

Fig.5 CBW Output

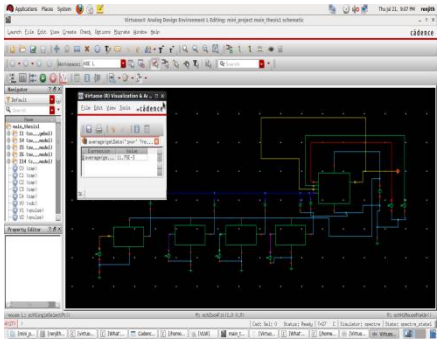

Fig.6 CBW Power Analysis

The power of DAC will be about 12mW. So the CBW architecture is not suitable for designing DAC in low power applications.

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B.BWA DAC

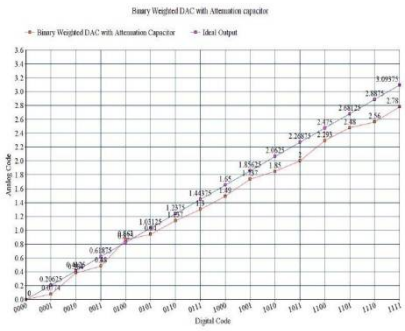

Fig.7 BWA Output

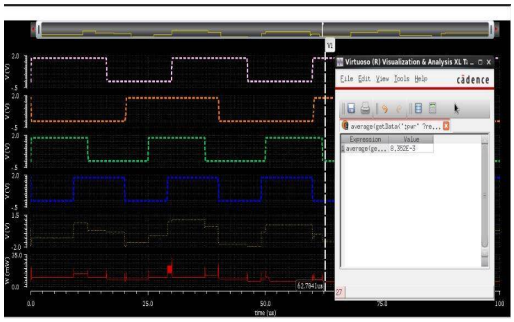

Fig.8 BWA Power Analysis

So here from the analysis its well clear that this architecture is also has a non-linear characteristics and it consumes power of about 9mW. To overcome these disadvantages, a new topology i.e SBW architecture is used.

C.SBW DAC

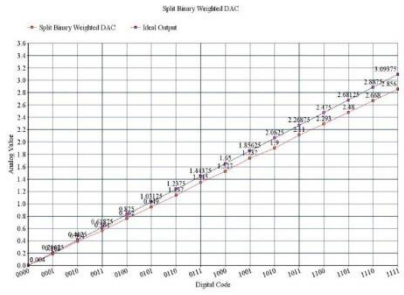

Fig.9 SBW Output

While analyzing power and output characteristics of SBW architecture its clear that it has linear characteristics and also has low power consumption of about 7.2mW.

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The layout and power of this SBW architecture is shown below :

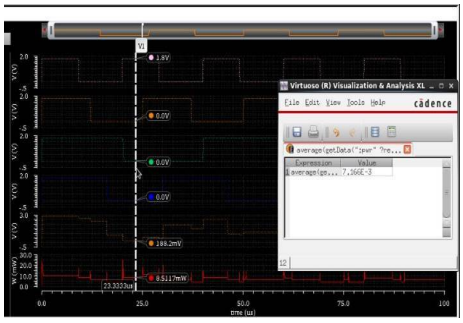

Fig.10 SBW Power Analysis

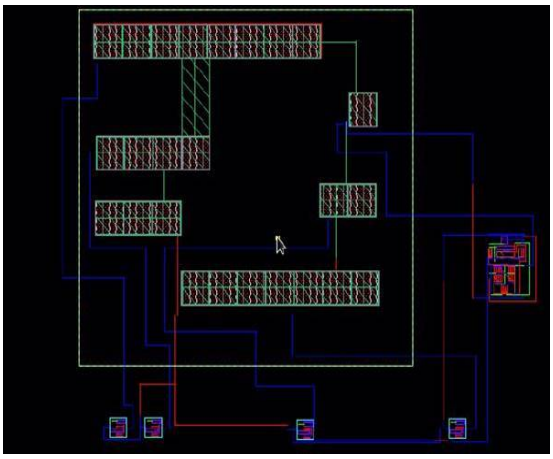

Fig.11 SBW Layout

IV.CONCLUSION

The power consumed by switching the capacitors of a capacitive array DAC employed in successive-approximation ADCs and its linearity behavior have been analyzed and verified by simulations for three commonly-used architectures i.e., the CBW, BWA and SBW structures.It is clear that with similar values for the sampling frequency, resolution, reference voltage and specifically the size of the unit capacitor, the average reference power consumption of the CBW array is around 12mW, for BWA array has 9mW and that of SBW array is around 7mW.From these analysis its well clear that SBW DAC has greater advantage compared to other architectures i.e., this modified architecture has low power consumption and greater conversion speed. So while coming to conclusion its clear that by using Split Binary Weighted DAC has low power consumption compared to other DAC architectures.Here I'm concluding that this SBW architecture is suitable for low power biomedical applications.

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