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# An Efficient Ultra Low Power Circuit by Using Subthreshold Adiabatic Logic

S.Srishanmugapriya[1], R.Nishanthi[2]

Assistant Professor, Department of Electronics and Communication Engineering, V.S.B Engineering College, Karur, India[1]

PG Student, Department of Electronics and Communication Engineering, V.S.B Engineering College, Karur, India[2]

**ABSTRACT**: This paper proposes a characteristic of adiabatic logic in week inversion the transistor is also called sub threshold adiabatic logic (SAL). Operation of Half adder and Full adder is considered in this work. This proposed system is used for ultra low power on application. Comparison shows power analysis of existing with proposed one gives that reduced average power. The proposed system can save adequate energy by using the SAL CMOS implementation. Observations are validated through the extensive simulation in 180nm CMOS technology using HSPICE.

## I. INTRODUCTION

Now days, requirements for implementation of low power application devices such as cellular system, notebook, wireless sensor network, especially biomedical applications like peacemaker has exponentially increased. Power consumption is very important factor in VLSI designers. For reducing the power usage from Vdd, harvesting power supply from environment is mostly used, but it doesn't reduce the leakage power from the CMOS implementation. In adiabatic logic leakage power is reduced and reused to the power clock as a Vdd. There are many types of adiabatic logic is used to restoring the efficient energy such as, efficient charge recovery logic (ECRL), energy efficient adiabatic logic (EEAL), positive feedback adiabatic logic (PFAL), and modified positive feedback adiabatic logic (MPFAL).

This paper explained sub threshold logic, circuits operated with the power clock Vdd, below than the threshold voltage (Vth) of the transistor, and it employ the sub threshold leakage current as a guiding current. Conventional CMOS logic circuit uses the sub threshold adiabatic logic can normally operate with the ultra low power consumption. In general design of sub threshold adiabatic logic, need in depth knowledge of power dissipation, leakage current, temperature variation, operating frequency and noise immunity. The main concept of sub threshold adiabatic logic is, if the hidden voltage between the source and drain of the transistor is lower than the threshold voltage, leads to the transistor being off. However, in naturally the transistor still keep it on off capability theses low levels, for the reason that the current doesn't totally turned off, it is shrink very fast. However the transistor will not reach at the level it was designed it will still perform similarly.

## II.PREVIOUS WORKS

In the previous method is uses the modified positive feedback adiabatic logic (MPFAL) to design a low power circuit. This work is based on the positive direct current (DC) ranges from 0.1V to 0.3V. The basic MPFAL inverter is constructed by two cross coupled inverter with a DC supply, and NMOS transistor is parallel connected with PMOS transistor for minimizing the degradation at end of the output.

This MPFAL is based on the level shifting technique, which has single power clock (pwr) and a single positive DC supply (Vdc). MPFAL doesn't pursue the lower level at the output, lower limit of the MPFAL is depends on the Vdc. If the Vdc is enlarged then lower limit of the output waveform is diminished. Both rise time and fall time of the MPFAL is depending up on the voltage between the source and drain. The circuit conveyance has four phases: *evaluate (E), hold (H), recovery(R), and wait (W).* In evaluation phase the supply voltage is growing from 0 to Vdd.

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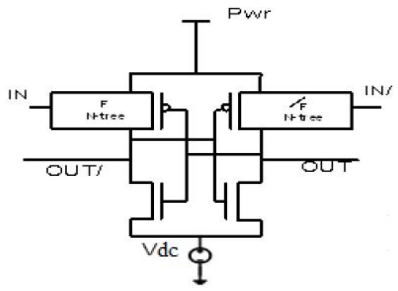


**Fig.1 Modified PFAL inverter circuit.**

In hold phase the supply voltage is remains stable to Vdd, and output keep their respective values. In recovery phase the charge is retrieved, the supply voltage ramps coming down from high to low and power supply retrieve stored value from the capacitor. In the wait phase the supply power is kept 0V.

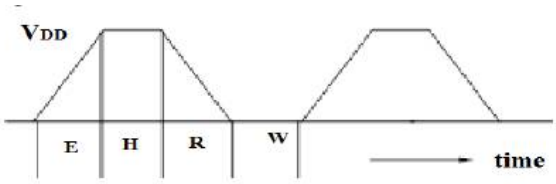


**Fig.2 Four phase power clock waveform.**

Level shifting technique is used to decreasing the Vgs at the output of the transistor, gate and leakage current. This circuit achieves low power operation for the reason of low DC source is serially connected to the circuit. However it operates only above the threshold limit of the circuit, it doesn't performing their operation below their threshold level. So the power dissipation is high in their region. For reducing power dissipation various logic is used. One of the best logic is sub threshold adiabatic logic (SAL).

## III.PROPOSED METHOD

In sub threshold adiabatic logic the design and analysis of half adder and full adder is given shown in output figure. Commonly all the digital gates are verified and implemented with their respective input. In SAL digital gates of the library are implemented with the ramp type of the input supply power.

***Subthreshold adiabatic logic***

An SAL inverter circuit and their outputs are shown in fig3. Inverter circuit ramp type of the input signal is used for energy saving purpose. This circuit contains a single transistor, and a load capacitor. When the threshold voltage is less than the Vds, the transistor act a resistor. When the threshold voltage is greater than the Vds, the transistor act as current source.

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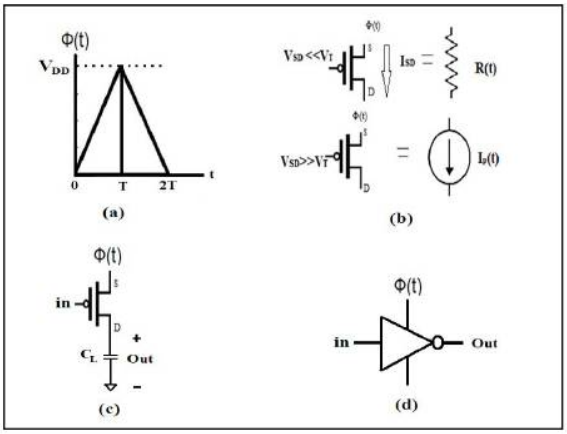


**Fig.3 SAL inverter circuit.**

In the event of SAL inverter circuit, if in=0, then the transistor act like a resistor for the reason that small amount of voltage flow across the source and drain terminal of the transistor. When ramp $\phi$ *(t)* going up from 0 to Vdd, the load capacitor as output capacitor will charge up to high output voltage (VOH). When the power clock is down from Vdd to low level, that the load capacitor hold their values is send back to the supply voltage.

When the supply voltages in charging phase or discharging phase the gate capacitance is deviate. According to principle few amount of energy is negligible and it is send from supply voltage to the inputs, this causing no adiabatic loss.

## IV. SIMULATION RESULTS

### *A.OUTPUT- SUB THRESHOLD ADIABATIC LOGIC*

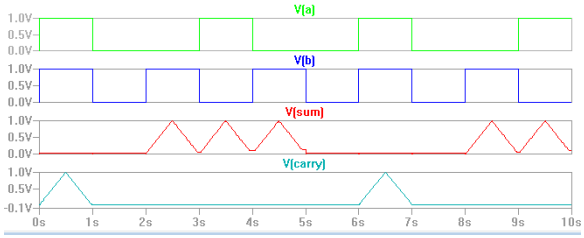


**Fig.4 Half adder SAL output**

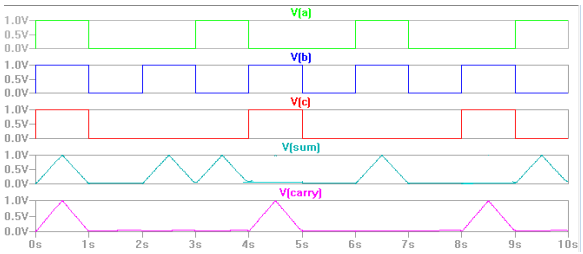


**Fig.5 Full adder SAL output**

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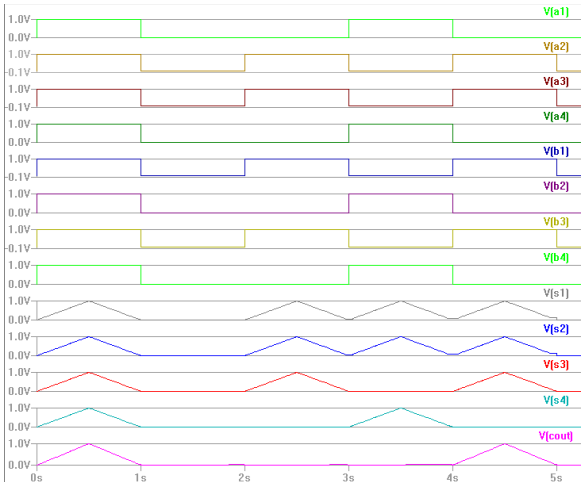


**Fig.6 Ripple carry adder SAL output.**

***B.POWER - PROPOSED METHOD:***

```
avgpower= 3.2744E-06  from= 1.0000E-09    to= 1.0000E-07
peakpower= 1.3603E-05   at= 1.0000E-09
        from= 1.0000E-09   to= 1.0000E-07
avgcurrent= -1.8884E-06  from= 1.0000E-09    to= 1.0000E-07
peakcurrent= 8.6401E-05   at= 1.6743E-09
        from= 1.0000E-09   to= 1.0000E-07
```

**Fig.7.2: Power calculation Screen shot –half adder SAL circuit.**

```
avgpower= 5.2023E-05  from= 1.0000E-09    to= 1.0000E-07
peakpower= 5.9425E-05   at= 1.0000E-09
        from= 1.0000E-09   to= 1.0000E-07
avgcurrent= -4.3081E-05  from= 1.0000E-09    to= 1.0000E-07
peakcurrent= 2.8429E-04   at= 1.1332E-09
        from= 1.0000E-09   to= 1.0000E-07
```

**Fig.7.4: Power calculation Screen Shot – Full adder SAL circuit.**

```
avgpower= 1.3142E-04  from= 1.0000E-09    to= 1.0000E-07
peakpower= 1.3142E-04   at= 3.8600E-09
        from= 1.0000E-09   to= 1.0000E-07
avgcurrent= -9.6907E-05  from= 1.0000E-09    to= 1.0000E-07
peakcurrent= -9.6907E-05   at= 1.0000E-07
        from= 1.0000E-09   to= 1.0000E-07
```

**Fig.7.6: Power calculation Screen shot –Ripple carry adder SAL circuit.**

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### *C. COMPARISON TABLE*

| S.No | Adders | Existing method | Proposed method |
|---|---|---|---|
| 1. | Half adder | 0.14306mw | 0.003274mw |
| 2. | Full adder | 0.16968mw | 0.052023mw |
| 3. | Ripple carry adder | 0.25442mw | 0.13142mw |

## V. CONCLUSION

Sub threshold adiabatic logic is an efficient method, to completely avoid the power dissipation. By using this method, half adder, full adder and ripple carry adder is compare with the existing method in which they used, Modified Positive Feedback Adiabatic logic. In this comparison power dissipation is reduced compare with the existing method. This implementation is done by 180nm CMOS sub threshold adiabatic logic.

## V. FUTURE WORK

In sub threshold adiabatic logic is mainly used to save the dissipated power. Further operation is operated by using this dissipated power, but the disadvantage of the adiabatic logic is cannot use the power to the circuit yet. By using the controlling device can save and use the dissipated power.

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