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Design of Digital Controller and it's Implementation on FPGA for Single Phase PWM Inverter

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ABSTRACT: In this paper the design of control law to calculate width of PWM pulse to generate the desire output voltage is described. Design of hardware and control law is carried out by considering 100 Watt application(load). This design is carried out with state space variable using digital control technique. Digital controlier is design using pole placement technique to achive desire transient response. Also the design of hardware required for single phase PWM inverter is described. The equation for Control law is implemented on FPGA device SPARTAN- III . The parallel processing capability of SPARTAN- III is used to reduce the total time to calculate control law. Also ADC interface circuit ,pulse generating circuit are implemented on FPGA device

KEYWORDS: FPGA ,Digital controller ,single phase ,PWM ,inverter,pole placement technique

I.INTRODUCTION

Inverter is one of important device in power electronics. It convert DC power into variable AC power. Output voltage waveform and frequency can be control by designing controller within inerter system . it is useful for those AC load which require variable AC power. In UPS system ,Inverter play important role. UPS system provide Emergency AC power when utility power system fail. It is require that THD (total harmonic distortion) in output waveform must be low and transient response of system fast enough[1].

Generally PWM technique is used to control the output voltage of inverter. Width of output pulses is is varied so as to minimize certain harmonics in the output waveform of inverter there are different technique which are used to generate PWM pulses which are used to turn ON and turn OFF switching device of full bridge inverter e.g. i) by comparing triangular waveform with sinusoidal waveform(SPWM) ii) programmed Pwm technique with Microprocessor. These control technique have following disadvantage i) the response time of voltage regulation is usually a few cycle because only average voltage is control ii) the phase difference between reference sine wave and the filter output varied with load. One of well known technique for PWM pattern is deadbeat digital controller. This technique is unique feature of digital control system. Deadbeat means placing all the poles of system of system at origin in Z-domain. In deadbeat control any nonzero error vector will be driven to zero in at most n sampling period if the magnitude scalar.

control U(K) is unbound. Settling time of system depends on sampling period. If sampling time is very small then settling time will also be very small. In deadbeat control ,the sampling period is only the design parameter so if deadbeat response is desire ,designer must choose sampling period carefully so that extremely large control magnitude is not require in normal operation of system the switching device need to handle[7].

Digital controllers are implemented by microprocessor, DSP processor or Microcontroller. Because of attractive feature of FPGA devise such as low power consumption and high speed complex functionality microprocessor are being replace by FPGA device in digital control system. In proposed system ADC interface circuit, PWM pulse generating circuit, Arithmetic circuit all are implemented on SPARTAN-III device. Parallel programming feature of FPGA system is utilized and hence total calculation time is reduce drastically which result in improvement in transient response of overall system[3].

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The organization of this paper is given as follow i) first section describe general block diagram of system. ii) Second section describes mathematical modeling of system. Iii) Third section describes FPGA implementation of Control system iii) forth section describes the simulated result of control system.

II. SYSTEM DESCRIPTION

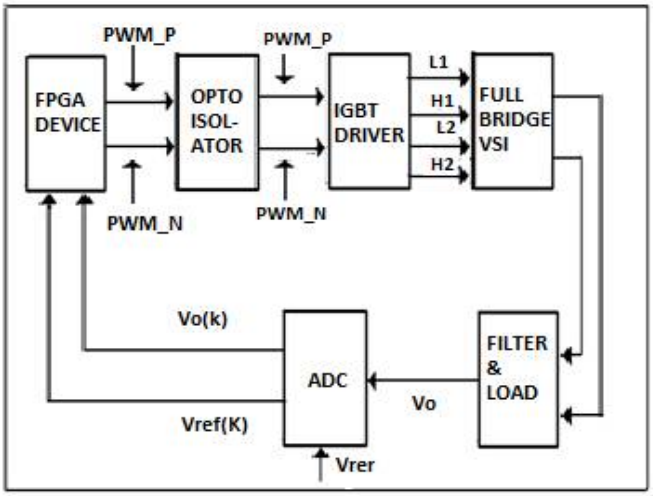

Fig. 1 Block diagram of proposed system

Proposed system is schematically described if fig. 1 full bridge VSI is power unit of system. It is responsible for the conversion of DC power to AC power. Turn ON and turn OFF of various switching device is control by digital controller which is implemented on SPARTAN-III. Width of pulse for +ve Vdc or –Vdc output depend on require voltage by Application(load). This width is calculated by control law. We require sample of output voltage and reference signal for calculation purpose. ADC7891 is used for this purpose. Its working is control by Spartan-III. Digital control law , ADC interface circuit , PWM generating circuit, Arithmetic unit all are synthesized on SPARTAN-III. FPGA device is very dedicate device (low power device) which need to be protected from power section unit (VSI) of system. Optocoupler is used for this work pulse signal from fpga device are applied to optocoupler. Output signal from optocoupler is then connected to gate circuit of IGBT.

III. MATHEMATICAL MODEL OF SYSTEM

VSI unit along with LC filter and load register Rl(plant) is shown in fig. 2

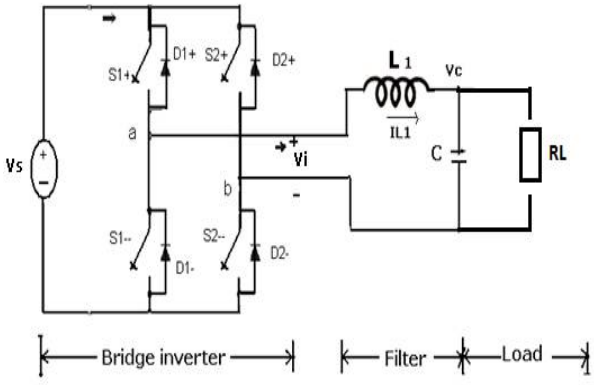

Fig. 2 Full bridge VSI with filter and load (plant)

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This circuit can be represent by its equivalent circuit as shown in fig 2 output of full bridge VSI circuit is +Vdc or –Vdc which is appliy to LC filter . the equivalent circuit of plant is shown in fig 3. The Gain of this system is given by

$$\frac{Vo}{Vi} = \frac{1/CL}{S^2 + \frac{1}{RC}S + \frac{1}{LC}} \quad (1)$$

$$\frac{Vo}{Vi} = \frac{w_n^2}{S^2 + 2\S w_n S + w_n^2}$$

By solving above equation we will get following equation

$$\ddot{V_o} = -w_n^2 V_o - 2\S w_n \dot{V_o} + w_n^2 * V_i \quad (2)$$

This is differential equation of VSI system. This equation decides the dynamics of system. If we select Vo and $\dot{V_o}$ as a state variable the state equation will be given by

$$\frac{dX}{dt} = AX + BV_i \quad (3)$$

$$Vc = C^T * X \quad (4)$$

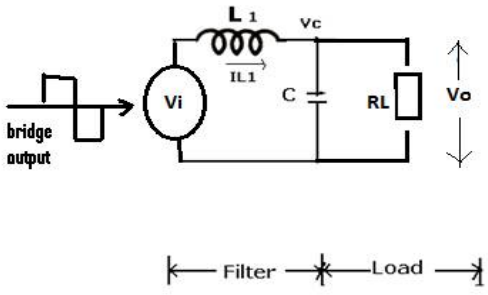

Fig. 3 Equivalent circuit of plant

Where,

$X = \begin{bmatrix} Vo \\ \dot{V_o} \end{bmatrix}$, $A = \begin{bmatrix} 0 & 1 \\ -w_n^2 & -2\S w_n \end{bmatrix}$, $B = \begin{bmatrix} 0 \\ w_n^2 \end{bmatrix}$ and $C^T = [1\ 0]$;

Equation 3 and 4 represent analog system. if we want its equivalent discrete time system , these equation need to be descritised as follow [7]

$$X(k+1) = G\,X(k) + H*U(k) \quad (5)$$

$$Y(k) = C\,X(k) \quad (6)$$

Where $G = \begin{bmatrix} q_{11} & q_{12} \\ q_{21} & q_{22} \end{bmatrix} = e^{AT}$

$H = \left(\int_0^T e^{At}\,dt\right)B$

Proposed system can be represented by state space modeling as shown in fig 4.

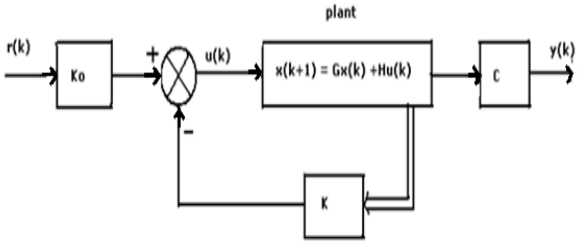

Fig. 4 State space modeling of system

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Now for a given system input reference signal is applied and hence system equation will become as follow

X(k+1) =G X(k) + H*U(k) (7)

Y(k) =C X(k)

And
U (k) =Ko *r (k) –KX (k)

In above equation K matrix is state feedback matrix and Ko is forward gain matrix . K matrix is design to place the available pole of system at desire location in Z-domain. Matrix K is calculated by [7] following equation

$K = [\alpha_n - a_n \quad \alpha_{n-1} - a_{n-1} \quad \alpha_{n-2} - a_{n-2} \quad \text{-------} \quad \alpha_1 - a_1]\, T^{-1}$

(8)

Where a_n are coefficient of original system characteristic equation and α_n are the coefficient of desire characteristic equation

Now transfer function of system describe by equation is given by

$F(z) = \frac{V_0(z)}{V_i(z)} = C(zI - G)^{-1} * H$

Where I is unity matrix and

Characteristic equation of F(z) is given by

$|(zI - G)| = z^n + a1\, z^{n-1} + \text{----- an} = 0$ (9)

Characteristic equation with state feedback system

$|(zI - G + HK)| = z^n + \alpha_1\, z^{n-1} + \text{----- } \alpha_n = 0$ (10)

And matrix T is given by

Where T = M W ;

M = [H GH] ;

$W = \begin{bmatrix} a_1 & 1 \\ 1 & 0 \end{bmatrix}$

Now given system is design for 60Watt load as an example

We will find Rl =

And L ,C component of low pass filter can be found by using equation

$Fo = \frac{1}{2\pi\sqrt{LC}}$

In proposed system fundamental frequency (fm) is 50 Hz and switching frequency is 20KHz. Based upon these frequencies, lower order frequency of filter will be 2000Hz [6] Suppose we select high cut-off frequency of low pass filter is 2 kHz then

$2000 = \frac{1}{2\pi\sqrt{LC}}$

Select L =1mH then C = 5.6 µF . now based on calculated value of Rl = ,L = , C = ,Ts = we will find following

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$G = \begin{bmatrix} 0.787 & 45.86 * 10^{-6} \\ -8.1855 * 10^{3} & 0.7668 \end{bmatrix}$

$H = \begin{bmatrix} 0.2 \\ 8.3663 * 10^{3} \end{bmatrix}$,

$M = \begin{bmatrix} 0.2 & 0.541 \\ 0 & -17.852 * 10^{3} \end{bmatrix}$

$F(z) = \frac{0.2\,z + 0.2304}{z^2 + 1.5\,z + 0.9783}$

Available pole are

p1 = 0.775 +j0.615 and p2 = 0.775 – j0.615

Characteristic equation of F(z) is given by

$|(zI - G)| = z^2$ - 1.55 z +0.9783

Hence a1 = -1.55 and a2 = 0.9783

Desired pole location

Dp1 = 0.5 +j0.5 and Dp2 = 0.5 – j0.5

Characteristic equation of desired closed loop system

$|(zI - G + HK)|$ = (z - 0.5 – j0.5)(z -0.5 +j0.5)

$= z^2$ - z + 0.5 (11)

We find α_1 = -1 and α_2 = 0.5

Matrix K is given by

K =[$\alpha_2 - a_2$ $\alpha_1 - a_1$] T^{-1}

= [-0.4783 0.55] T^{-1}

We will find matrix K as

K = [0.079 $6.0617 * 10^{-5}$]

Feedback gain matrix K is determined to yield the desired closed loop poles. State feedback through Matrix K changes the characteristic equation for the system, but in doing so the steady state gain of the entire system is changed. Therefore, it is necessary to have an adjustable gain Ko in the system. This gain Ko should be adjusted such that the unit step response of the system at steady state is unity In fig 2.9

U(k) = Ko r(k) –Kx(k)

Then, X(k+1) =(G- HK)x(k) +HKo *r(k)

X(k+1) =G1*X(k) + H1 *r(k)

$\frac{Y(z)}{R(z)}$ =G(z) = $C(zI - G1)^{-1} * H1$

$\frac{Y(z)}{R(z)} = \frac{0.2Ko\,z + 0.2301\,Ko}{z^2 - 1.03z + 0.498}$ (12)

$\lim_{k\to\infty} y(k) = \lim_{z\to 1}(1 - z^{-1})^{-1} Y(z)$ we will find

Ko =1.088

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Derivation of Control law

From fig 5 U(K) is given by,

U (k) =Ko *r (k) –KX (k)

=1.0881*r(k) - 1.079*v(k) – 6.0617*10^{-5}*$V_o\dot{(k)}$

Now $V_o\dot{(k)}=\frac{V_o(k)-V_o(k-1)}{T}$ & T = 50µs Hence

U (k) =1.0881 *r (k) -2.291 *$V_o(k)$ +1.212 $V_o(k-1)$ (13)

Thus pulse width is calculated[7]. This pulse width is require is to control Vc(k) hence I0(K)

IV. FPGA IMPLEMENTATION

In propose system SPARTAN-III 3s400 is used for the implementation of control law. Block diagram of FPGA implementation is shown in fig 6 main controller , ADC interfacing unit ,PWM unit , Arithmetic unit are all implemented on FPGA system

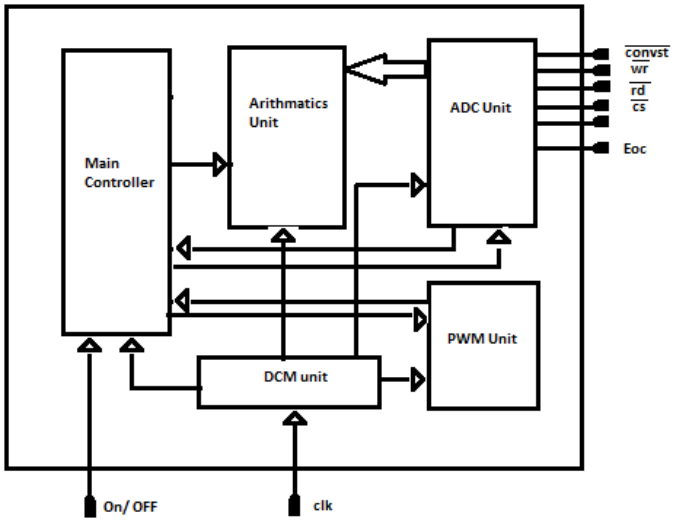

Fig. 6 Block diagram of internal modeling of system in FPGA

V. SOFTWARE DESIGN

Hardware is designed on FPAGA device SPARTAN III (xc 3s 400) to perform following task

1) To get the discrete value of state space variable V_o , $\dot{V}_o$ at K^{th} instant using AD7891
2) To calculate pulse width U (K) using a arithmetic unit
3) Block to generate PWM_P or PWM_N of width U(K)

A MAIN FLOW CHART

Flow chart of main controller is shown in fig7. In main controller signal to start the function of ADC section, Arithmetic unit, PWM unit and Timer are generated. Output voltage and reference voltage are connected to channel 1 and 2 of AD7891 respectively. ADC takes about 16 cycles to take the sample of output voltage and reference voltage. ADC unit and Timer unit both start at the same time. Counter is set for 80µS. End of this time will switch the main controller to reset state. Now clock frequency of main program is set to T =20µs which generate the blanking time for IGBT of

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VSI. End of ADC start working of arithmetic unit which calculate pulse width. End of arithmetic unit start PWM unit which generate the pwm_p or pwm_n of width given by U (k). End of timer jump to restart cycle.

B. FLOWCHART TO CONTROL AD7891

Flow chart of controller for AD7891 is shown in fig.8. Controller of ADC unit generate the various control signal to control the functionality of AD7891.ADC is set to work in parallel mode. Hardware start conversion is used. In the first step chip enable output is set to logic 1 and control word is written to control resister of AD7891. Control word consist address of current channel and format of converted data (binary or 2s complement). Then start conversion output is set to logic 1. This initiate conversion process. By the end of 1.6 µs EOC(end of conversion)pulse of 90ns will generated by AD7891. After this data is read by setting logic 1 to RD output, Counter is increment by 1 which gives address of next channel for conversion if this data is less than 2 then process will repeat.

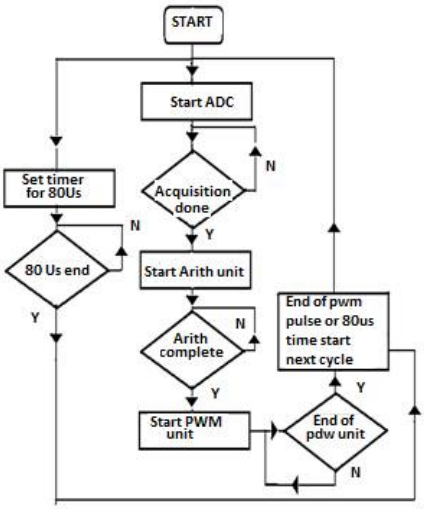

Fig.7. Main flow chart of VHDL program

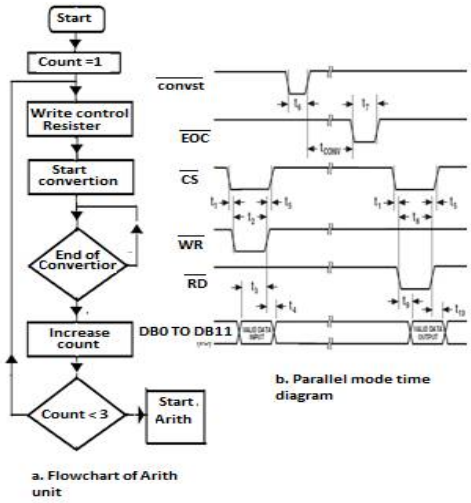

Fig.8 Flowchart to control AD7891 and parallel mode timing diagram

C. FLOWCHART OF PWM UNIT

This unit generates the pulse pwm_p or pwm_n depending upon the sign of U (K). Width of this pulse depends upon the magnitude of data U (K) depends upon the magnitude of data U (K)

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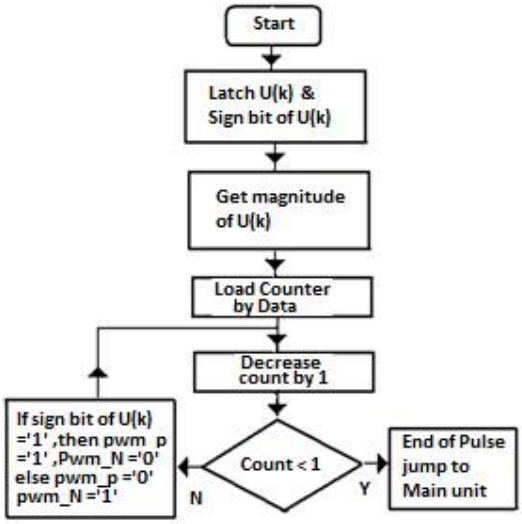

Fig. 9. Flowchart of PWM unit

VI. SIMULATION RESULT

A. MAIN FLOW CHART WAVEFORM

In main controller signal to start the function of ADC section, Arithmetic unit, PWM unit and Timer are generated.

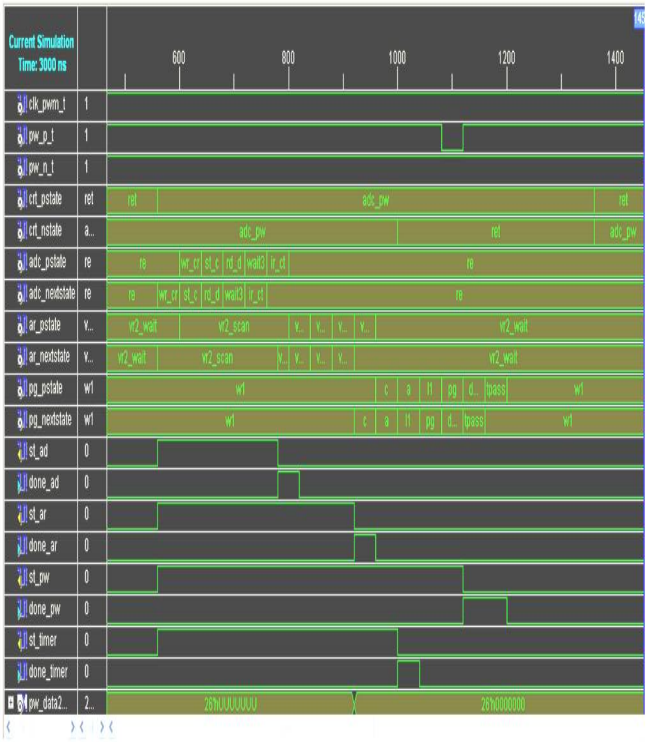

Fig.10 Control signal generated by main control unit

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B. ADC UNIT WAVEFORM

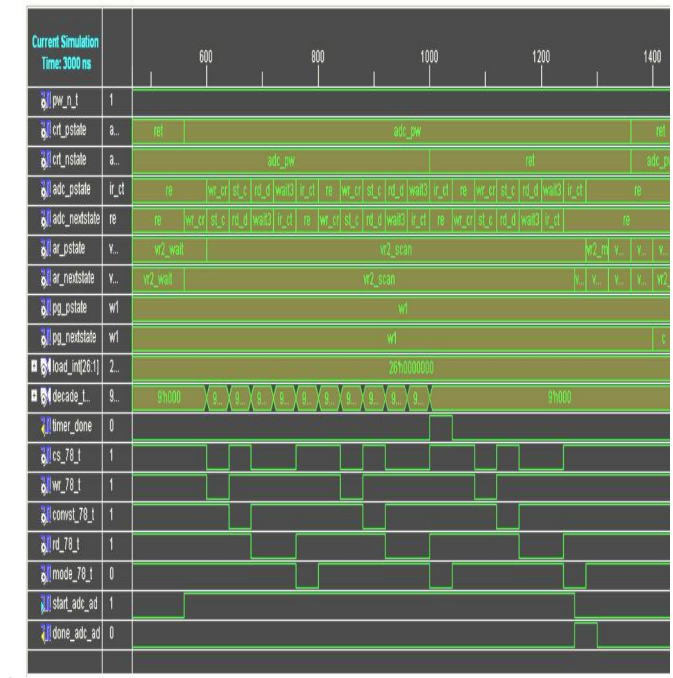

Fig.11 Control signal generated by ADC block

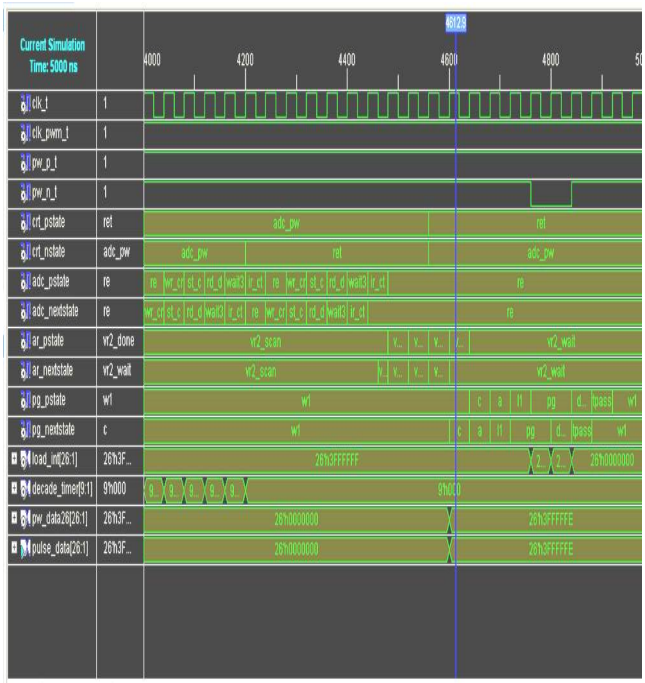

Fig.12. Arithmetic unit calculate pulse width U(K) =PWM_data = 3FFFFFE

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D PWM Unit Waveform

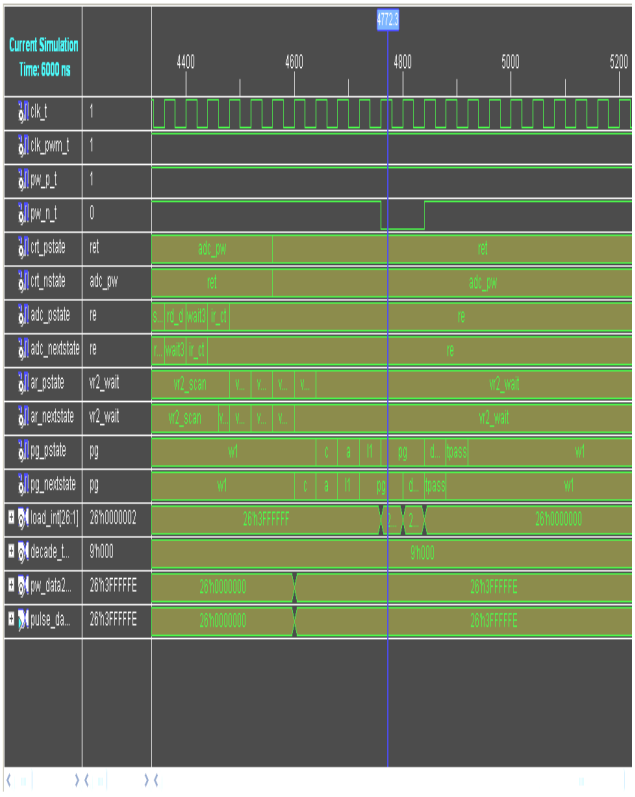

Fig.13. PWM pulse generated by PWM unit for negative output voltage

VII. CONCLUSION

New approach of real time digital feedback control method which is based on instantaneous control using FPGA (Spartan III) based hardware controller is proposed .A concept FPGA based digital controller is described. control law is design using pole placement technique to achieve desire transient response, total calculation time is approximately using 2MHz crystal freq. which is very less as a result performance of the system improved

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