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Design and Simulation of Fast and Power Efficient Voltage Level Shifter with Sleepy Keeper

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ABSTRACT: A voltage level shifter is a circuit which converts low level input voltages to a desired higher level voltage or vice versa as desired, depending upon the system requirements. The major application of a voltage level shifter is in resolving mixed voltage incompatibility. The integrated circuits which are widely used nowadays may have different parts within, which operate at different voltage levels. Most of these circuits were provided with different supply voltage levels which prove to be difficult when the number of supply voltages increases within a single circuit increasing its complexity. Energy efficiency is a primary concern in modern CMOS circuits. Thus level shifters which are capable of converting a single low level voltage to other voltage levels have become useful in circuits having parts operating in multiple voltage domains. In the proposed design, the major aim is to lower the power dissipation and make the circuit faster.

KEYWORDS: Level shifter**,** sleepy keeper, power, delay, noise, voltage incompatibility

I.INTRODUCTION

The voltage level shifter or converter is a circuit which converts low level input voltages to a desired higher level or vice versa as and when required. The integrated circuits which are widely used nowadays may have different functional blocks within, which operate at different voltage levels. When different supply voltages are provided to these functional blocks for their operation, it becomes difficult as the complexity of the circuit increases. Thus level shifters which are capable of converting a single voltage to other voltage levels have become useful in circuits having parts operating in multiple voltage domains.

Power consumption in VLSI circuit consists of dynamic and static power consumption. Energy efficiency is a primary concern in modern CMOS circuits A standard method to reduce power consumption is to lower the supply voltage due to the quadratic dependence of dynamic power on voltage. The static power of CMOS circuits is determined by the leakage current through each transistor and also the direct path between the supply and ground. Power consumption of VLSI circuits can be reduced by scaling supply voltage and capacitance. Speed of a circuit depends on its delay factor which is the length of time which starts when the input to a logic gate becomes stable and valid to change, to the time that the output of that logic gate is stable and valid to change. Delay can be reduced by stacking technique and proper ratioing of width and length of the transistors.

II.RELATED WORKS

Conventional level shifters [10] are the simplest and basic type of level shifters which were used for voltage level conversion. It is basically a circuit comprising ten transistors with low voltage supply V_{DDL} and high voltage supply V_{DDH} . The single supply level shifter allows communication between modules without adding any extra supply pin [10]. Single supply level shifters have advantages over dual supply in terms of pin count, congestion in routing and overall cost of the system. Another benefit of single supply is flexible placement and routing in physical design. With increase in operating frequency and number of level shifters in data driver's circuits, power consumption has become major performance metrics. It has been proved that stacking of two nmos devices reduces the sub-threshold leakage [10] as compared to single nmos device. So, to reduce the leakage power consumption of level shifter circuits, the approach using the concept of stacking technique without compromising the outputs levels has been initiated.

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Conventional level shifter with stacking uses three additional nmos transistors and single supply level shifter with stacking technique uses two additional nmos transistors. Contention between nodes would lead to pulling up and down a particular node simultaneously. One approach to solving this problem is to increase the current of the pull-down transistors by enlarging their widths [3]. To overcome the limitations of the level shifter with enlarged nmos width, a solution is to reduce the strength of the pull-up devices by limiting their currents. The process of limiting the current through the pull-up devices is carried out effectively by using a current mirror [4]. Thus, the usage of a current mirror widely helps in obtaining the desired conversion of low level input to high level supply.

The limitations such as static power dissipation which is a major factor affecting the performance of the entire circuit can be overcome to a greater extent by the implementation of an energy-efficient level converter [5] capable of converting an input signal from subthreshold voltages up to the nominal supply voltage. One method for reducing power is using a supply voltage below the device voltage threshold V_T, which is referred to as subthreshold operation. Reducing the supply voltage can have up to a quadratic reduction of energy. Hence this becomes an energy-efficient level converter.

In order to reduce the static power dissipation, a level shifter with logic-error correction, LSLEC [6] is designed. It uses a distinctive current generator that works only during the transition times. The LSLEC employs a logic error correction circuit in which the logic level of the input signal is not corresponding to the output logic level. The logic error correction circuit works by detecting the input and output logic levels.

III.PROBLEM DOMAIN

Voltage level shifters are needed in VLSI systems which employ low-power design technique using multiple supply voltages to correctly communicate with other circuit blocks within the system. In low-voltage VLSI systems, subthreshold circuits have attracted much attention for use in power-aware VLSI. The major advantage of level shifters operating in subthreshold region is its ability to generate higher voltages from the subthreshold voltage. Taking into account this wide scale applicability of voltage level shifters, this particular topic is chosen as the area of research.

IV.MOTIVATION

The key motivation for utilizing level shifters in such applications is its ability to handle extremely low-input voltage and generate higher voltages. Power efficiency and speed are major factors of performance of all the circuits. Various techniques have been adopted to reduce static and dynamic power. Some of the most commonly used techniques are dynamic voltage scaling operating down to near threshold voltage levels and supporting multiple voltage domains. The subthreshold digital LSIs will be implemented with conventional circuits that operate at high supply voltages. Because the supply voltage of the subthreshold VLSI is lower than the threshold voltage of a MOSFET and that of the peripheral circuits is still high, communication with other peripheral circuits becomes difficult.

In emerging multiple-supply systems, battery-less VLSI systems have been reported. Such systems are expected to expand the market greatly over next decade. They have to obtain the necessary energy from energy harvesters. However, because the output voltages of the harvesters are too low for VLSIs to operate, voltage boost converters are used to generate higher voltages. Therefore, the systems are inherently multiple-supply systems. To achieve highly efficient energy harvesting systems, they have to handle extremely low-input voltage. Thus, a voltage level shifter is required.

With the growing demand of handheld devices like cellular phones, multimedia devices, personal note books and so on, low power dissipation has become major design consideration for VLSI circuits and systems. With increase in power consumption, reliability problem also rises and cost of packaging goes high. Power consumption in VLSI circuit consists of dynamic and static power consumption. Energy efficiency is a primary concern in modern CMOS circuits A standard method to reduce power consumption is to lower the supply voltage due to the quadratic dependence of dynamic power on voltage.

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Dynamic power has two components as switching power due to the charging and discharging of the load capacitance and the short circuit power due to the non-zero rise and fall time of the input waveforms. The static power of CMOS circuits is determined by the leakage current through each transistor and also the direct path between the supply and ground. Power consumption of VLSI circuits can be reduced by scaling supply voltage and capacitance. Static power component of power consumption must be given due consideration if current trends of scaling of size and supply voltage need to be sustained.

Speed of a circuit depends on its delay factor which is the length of time which starts when the input to a logic gate becomes stable and valid to change, to the time that the output of that logic gate is stable and valid to change. Delay can be reduced by stacking technique and proper ratioing of width and length of the transistors.

V. PROBLEM CAPTURE

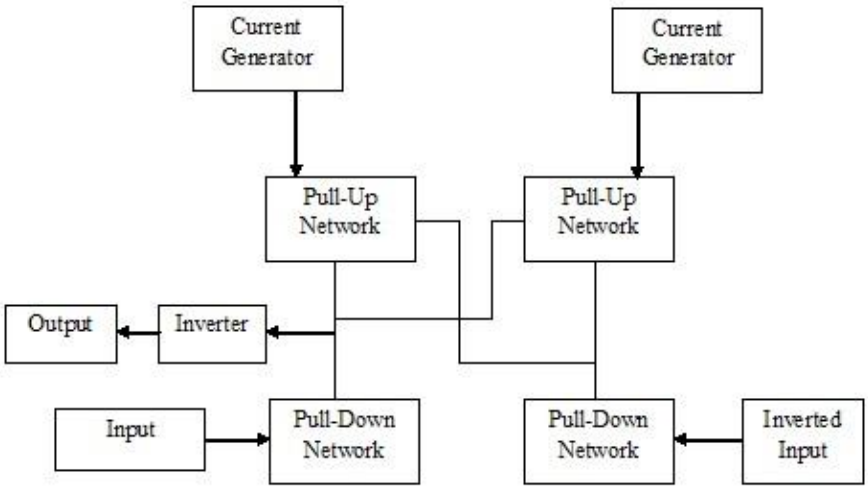

Fig. 1 Block diagram of Voltage Level Shifter

Fig. 1 shows the block diagram of voltage level shifter. The block diagram consists of four sections as:

1) Pull-up network
2) Pull-down network
3) Inverter
4) Current Generator

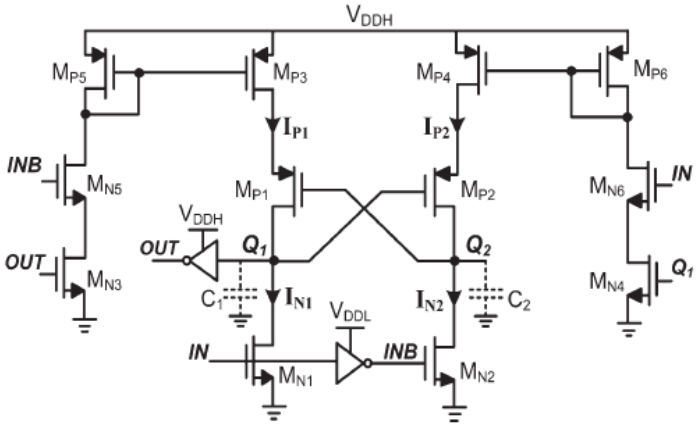

Fig. 2 Present Design of Level Shifter

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Fig 2 shows the present design of the voltage level shifter circuit [1]. In the present circuit, in order to reduce the strength of the pull-up devices, two current generators, limit the currents applied to the pull-up transistors, MP1 and MP2. Consequently, by decreasing the strength of the pull-up devices, the pull-down transistors, MN1 and MN2 would be able to overcome the mentioned contention at the nodes Q1 and Q2 and therefore discharge the output nodes to VSS even for the input voltages lower than the threshold voltage. In order to avoid the static power dissipation, the current generators are turned on only during the transition times, in which the logic level of the input signal is not corresponding to the output logic level.

When the input signal IN is going from V_{SS} to V_{DDL}, MN1 is turned on and MN2 is turned off. Therefore, similar to the conventional counterpart, MN1 tries to pull down the node Q1, and consequently, MP2 is gradually turned on to pull the node Q2 up to V_{DDH}. When IN changes from V_{SS} to V_{DDL}, there is an interval during which Q1 does not correspond to the logic level of IN. During this period, both MN4 and MN6 turn on, and therefore, a transition current flow through MN4, MN6 and MP6.

This transition current, which is mirrored to MP4, flows into MP2 and then charges the node Q2. At the same time, MN5 turns off because INB is V_{SS}, and therefore, there is no current flowing through MP1, meaning a weak pull up device. This causes that MN1 be able to pull down the node Q1 even for the input voltage lower than the threshold voltage of MN1. Finally, when the node Q1 is pulled down to V_{SS} and Q2 is pulled up to V_{DDH}, MN4 is turned off, and therefore, no static current flows through MN4, MN6 and MP6. This means that the current generator structures are turned on only during the transition times, reducing the static power dissipation. Similarly, when the input signal IN is switched from V_{DDL} to V_{SS}, the operation is forced to reverse states. Apart from the level shifters which exhibit contention at the nodes between the pull-up and the pull-down transistors, the present design of the level shifter significantly reduces or almost completely eliminates contention in the nodes by a specified procedure of operation of the circuit.

The operation of the circuit is designed in such a way that at the transition times, the dynamic current generator applies the transition current into either MP3 or MP4 identifying the transistor which is supposed to pull up the related output node, either Q1 or Q2 respectively. Thus, it can be ensured that in contrast to the LSLEC structure, there is much less or probably no contention between the pull-up and the pull-down devices of the proposed structure. Thus, the proposed level shifter not only is capable to convert extremely low levels of the input voltages, but also improves the performance of the circuit.

VI.SLEEPY KEEPER INVERTER

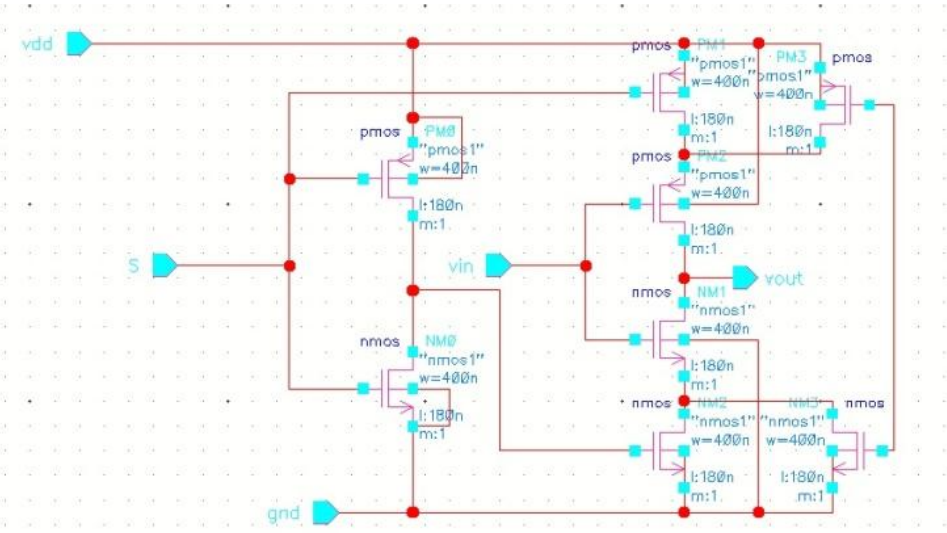

Fig. 3 Schematic Diagram of Sleepy Keeper Inverter

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Sleepy keeper [14] uses leakage feedback technique. The pmos transistors are not efficient at passing GND and nmos transistors are not efficient at passing V_{DD}. In this technique, a pmos transistor is placed in parallel to the sleep transistor (S) and an nmos transistor is placed parallel to the sleep transistor (S'). The sleep transistors are turned off during sleep mode and transistor in parallel to sleep transistor keep the contact with the appropriate power rail.

Sleepy keeper inverter consists of the normal inverter, to whose gates which are shorted, the input is given and from whose drains tied up together the output is taken. Two sleep transistors are accommodated in the inverter circuit, a pmos with input S and an nmos with input S'. The major advantage of using sleepy keeper technique [14] is that it improves the performance by reducing noise, power dissipation and delay of the circuit.

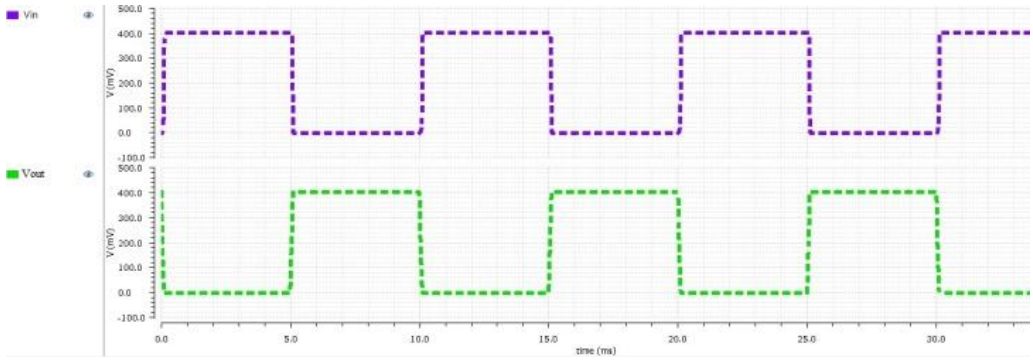

Fig. 4 Output of Sleepy Keeper Inverter

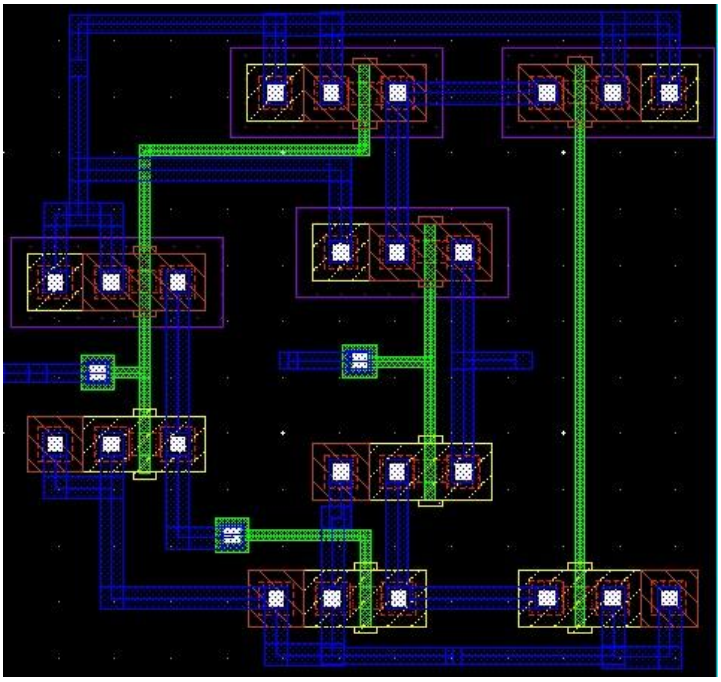

Fig. 5 Layout of Sleepy Keeper Inverter

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VII.VOLTAGE LEVEL SHIFTER WITH SLEEPY KEEPER INVERTER

The basic level shifter consists of two normal inverters, one the V_{DDH} inverter and other the V_{DDL} inverter. In case of the modified level shifter, the only difference from the basic level shifter is that it employs sleepy keeper inverters in place of normal inverters. It also employs two current generators on either of the pull-up devices which achieve various enhancements as compared to the existing level shifters [1] so as to avoid contention. The design can be implemented in 0.18µm technology using Cadence Virtuoso tool. Further, the circuit can be analysed by varying widths of the transistors used with a finite length so as to reduce the power dissipation and at the same time reduce the propagation delay.

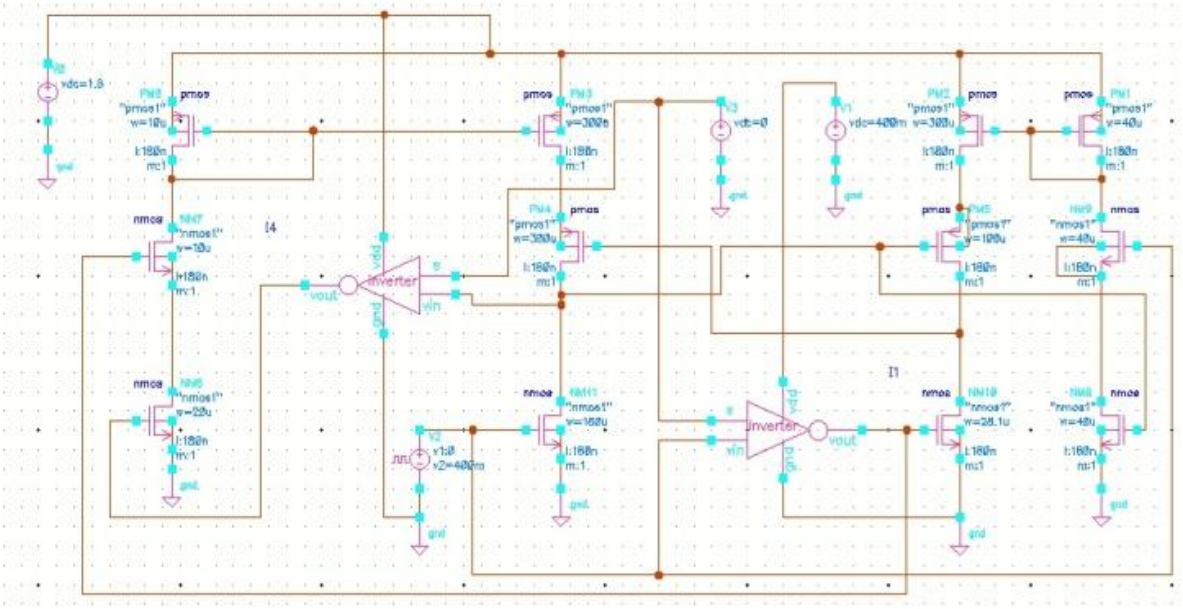

Fig. 6 Schematic Diagram of Level Shifter with Sleepy Keeper Inverter

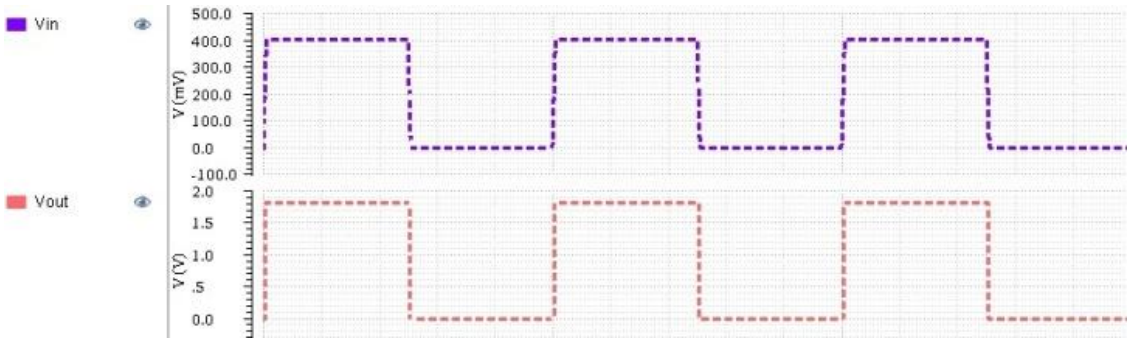

Fig. 7 Output of Level Shifter with Sleepy Keeper Inverter

The output is obtained and it is observed that apart from the output waveform of the normal level shifter which appeared to be noisy, the output of the voltage level shifter with sleepy keeper inverter has a much lower noise. The power dissipation and delay value can further be calculated from the output waveform which is obtained. So, one of the factors has been improved by modifying the basic level shifter accommodation of sleepy keeper inverters in place of normal inverters.

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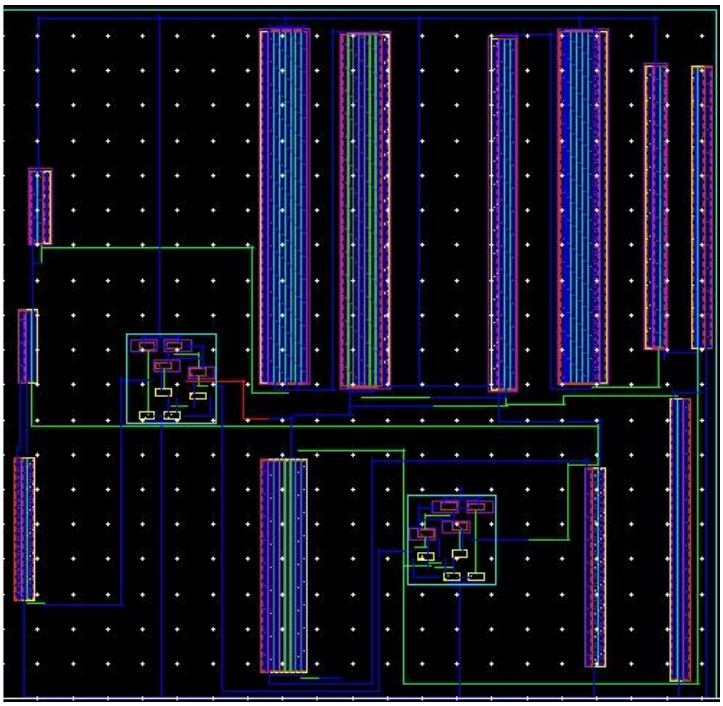

Fig. 8 Layout of Level Shifter with Sleepy Keeper Inverter

VIII.RESULT AND PERFORMANCE ANALYSIS

Average power of level shifter with sleepy keeper inverter is 19.97nW. The delay obtained is 2.839ns. The basic design of a voltage level shifter converts the low level input of 0.4V to high level output of 1.8V. But the output is noisy and has a delay of 32.38μs and power dissipation of 10.68μW. Sleepy keeper approach is incorporated in inverters to improve circuit performance. As a result of this technique, the noise in the output is lowered. The delay reduces to 2.839ns and the power dissipation reduces to 19.97nW. Thus the modified level shifter has improved performance.

CHARACTERISTICS	LEVEL SHIFTER (NORMAL)	LEVEL SHIFTER (SLEEPY KEEPER)
Power Dissipation	10.68μW	19.97nW
Delay	32.38μs	2.839ns
Noise	High	Low

Fig. 9 Summary of Results

IX.CONCLUSION AND FUTURE WORKS

The goal of the thesis was to design and simulate a voltage level shifter in 180 nm CMOS technology at transistor level. The basic design of a voltage level shifter converts the low level input of 0.4V to high level output of 1.8V. But the output is noisy and has a delay of 32.38μs and power dissipation of 10.68μW. Sleepy keeper approach is incorporated in inverters to improve circuit performance. As a result of this technique, the output has a very low noise. The delay reduces to 2.839ns and the power dissipation reduces to 19.97nW.

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Level shifters are essential to adjust resultant voltage differences between internal blocks and between the internal core and I/O circuits. In the past, DRAMs and flash memories have required such voltage converters to ensure stable operations and retention characteristics of memory cells, and they will continue to need such converters. In future, SRAM cells may adopt such level shifters for ensuring low sub threshold current and stable operation. Also, in future, the proposed level shifter can be implemented in flip-flop circuit for further reducing the power and to achieve the voltage conversion from subthreshold to above threshold.

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