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High Speed Multiplier Using Vedic Sutra

Rodabasannavar S. R. [1], Kallimani S. B.[2]

Assistant Professor, Dept. of E&TC, Sanjay Ghodawat College of Engg., Atigre, Maharashtra, India[1]

M. E Scholar [VLSI Design & Embedded System], Sanjay Ghodawat College of Engg., Atigre, Maharashtra, India[2]

ABSTRACT: A 4-bit High Speed multiplier design based on Urdhva Triyakbhyam technique is presented in this paper. The Vedic Multiplier is designed with the help of Brent Kung Adder. In this design 4-bit Brent Kung adder is used. Vedic mathematics is derived from the ancient Vedas, it is based on sixteen word-formulae. Urdhva Triyakbhyam(U-T sutra) is one of sixteen formulae, which mean Vertically and Crosswise. The Urdhva Triyakbhyam formula helps to reduce delay in multiplication thereby increase overall speed of the system. The code is written using VHDL language and is implemented on Xilinx Digilent Nexys 3 Spartan 6, xc6slx16-3csg324 FPGA device kit.

KEYWORDS: Vedic Mathematics, Urdhva Tirabhyam Sutra, Brent Kung Adder , FPGA Device Kit.

I.INTRODUCTION

The vedic formulae are based on natural principles on which the human mind works and it reduces typical calculations. Nowadays power consumption is a major concern in the VLSI circuit design, high power consumption leads to reduction in battery life like movable phones, laptops etc. and affects the reliability of the system. Vedic multiplier using vedic sutras is quicker and consumes lesser power. The multipliers are vital fundamental arithmetic functional units in many transform, the concert of these transforms strongly depends on the multiplication. Power conservation is a key concern in the VLSI circuit design. In this paper using Urdhva Triyakbhyam sutra from vedic mathematics a 4bit high speed binary multiplier is designed. The parallel prefix 4-bit Brent Kung Adder is also designed, Brent Kung adder gives fast addition results which makes multiplier more faster.

In this paper using brent kung adder is designed which makes this multiplier more faster than conventional multiplier. Brent-Kung adder is a widely used adder. It actually gives an excellent number of stages from input to all outputs but with asymmetric loading of Intermediate stages. It is one of the parallel prefix adders where these adders are the best class of adders that are based on the use of generate and propagate signals. The code is written in using VHDL language and simulated in ISE Design Suite 14.2 and implemented on Xilinx Digilent Nexys 3 Spartan 6, xc6slx16-3csg324 FPGA device kit. Maintain minimum delay and get faster result is the key factor in proposed multiplier.

II.VEDIC MATHEMATICS

"Vedic Mathematics" is a system of reasoning and mathematical working based on ancient Indian teachings called Veda. It is fast, efficient and easy to learn and use. Vedic mathematics, which simplifies arithmetic and algebraic operations. Vedic Mathematics provides answer in one line where as conventional method requires several steps. It is an ancient technique, which simplifies multiplication, divisibility, complex numbers, squaring, cubing, square and cube roots. The basis of Vedic mathematics, are the 16 sutras, which attribute a set of qualities to a number or a group of numbers. Out of these sixteen sutras the Urdhva Tiryakbhyam sutra is especially used for multiplication.

1. Urdhva Tiryakbhyam algorithm

"Urdhva Tiryakbhyam" (Vertical and Crosswise) sutra (Algorithm). It is a general multiplication formula equally applicable to all cases of multiplication. The algorithm generates all partial product and sum in one step. The algorithm is generalized for nxn bit number .This Multiplier has advantage that when we increase the number of bits ,gate delay and area increases very slowly compared to other multipliers. Due to its regular structure, Multiplier processing power increase by increasing the input and output data bus widths. The digits on the two ends of the line are multiplied and the result is added with the previous carry. When there are more lines in one step, all the results are added to the previous carry. The least significant digit of the number thus obtained acts as one of the result digits and the rest act as the carry for the next step. Initially the carry is taken to be as zero.

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III.ADDER

Addition is most commonly used arithmetic operation and plays important role in microprocessor, digital signal processing and data processing applications. In proposed dissertation work half adder and 4-bit Brent Kung adder is used, which gives high performance arithmetic structure and increase the speed of operation. Half adder perform two bit addition, it has two input say A and B and it generate two bit output which are SUM and CARRY. On the other hand Brent Kung adder is parallel prefix adder which also called as tree adder. This adder is based on use of generate and propagate signal. In case of this adder the wiring complexity is less and adder performs fast addition of four bit numbers.

IV.MULTIPLIER METHODOLOGY

High speed vedic multiplier using vedic sutra is designed using half adder and 4-bit Brent Kung adder. Using Urdhva Tiryakbhyam sutra multiplication is performed, this sutra makes calculations more easy and fast. The half adder is used to perform 2-bit addition and Brent Kung Adder is used to perform 4-bit addition operation. Brent kung adder is parallel prefix adder which perform more fast addition operation, because it performs parallel addition of binary numbers.

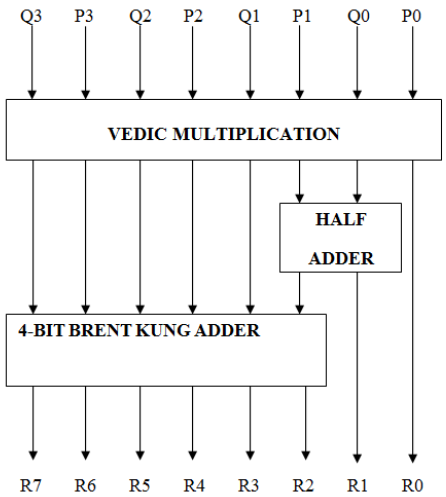

Fig. 1 Block Diagram of 4-bit High Speed Multiplier Using Vedic Sutra

The 4x4 bit multiplier is designed by using Half Adder and 4-bit Brent Kung adder. Here, the multiplicands are having the bit size of 4 where as, the result is of 8 bit in size. As mentioned earlier with the example 2 bit multiplication using vedic sutra include four steps, here in this 4 bit multiplication design include six steps. The block diagram of vedic multiplier is contains multiplier block where vedic multiplication is carried out with the help of AND gate. AND gate is basic gate which perform logical multiplication operation. Half adder block is used to perform the 2-bit addition operation, half adder designed using X-OR gate and AND gate. 4 bit brent kung adder performs the 4 bit addition operation.

Urdhva Triyakbhyam means Vertically & Crosswise, the name gives the method of multiplication using this sutra. Figure 3 shows the steps involved in performing the 4-bit multiplication using vedic sutra. Here the cross multiplication of digits from both multiplicand is performed and the results of each steps are added together, from each step if carry generates then it is added in next step.

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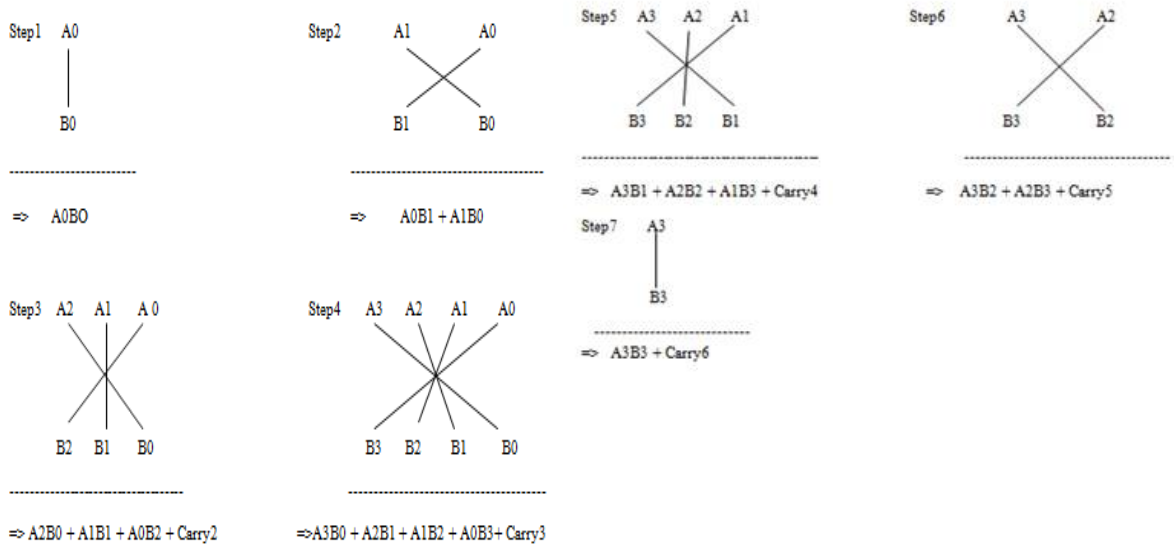

Fig. 2. Vedic Multiplication Steps for 4x4 bit multiplication

Above Fig. 2 shows the steps involve in Urdhva Tiryakbhyam sutra. For 4 bit multiplication total seven steps involved. Step 1 involve multiplication of unit place number of both multiplicand. Step 2 involves cross multiplication unit place and tens place numbers of both multiplicand and addition of them. Step 3 involve cross multiplication of unit, tens and hundred place numbers of both multiplicand and addition of them plus the carry generated in step 2. Step 4 involve cross multiplication of unit, tens, hundred and thousand place numbers of both multiplicand and addition of them plus the carry generated in step 3. Step 5 involve cross multiplication of unit, tens and hundred place numbers of both multiplicand and addition of them plus the carry generated in step 4. Step 6 involves cross multiplication hundred place and thousand place numbers of both multiplicand and addition of them plus carry generated from step 5. Step 7 involve multiplication of thousand place number of both multiplicand and addition of them plus carry generated from step 6. For multiplication of each pair of number AND gate used in proposed work. There are total sixteen AND gates are used to cover all seven steps. The logic diagram of proposed work in given in next session.

V.LOGIC DIAGRAM

The logic diagram of High Speed Vedic Multiplier is as shown in Fig. 3. The Urdhva Tiryakbhyam sutra is used to perform the multiplication process, which includes easy steps to perform the multiplication and gives fast results. Here in dissertation to perform this multiplication the two input AND gates are used. Here as it 4-bit multiplication, the total number of steps need to perform multiplication is seven. Hens totally 16 two input AND is designed here. After multiplication further addition operation is carried out using Half adder and 4-bit Brent Kung adder. Half adder perform 2-bit addition and generates two output, one is sum and other is carry. 4-bit Brent Kung adder performs parallel addition of 4 binary digits.

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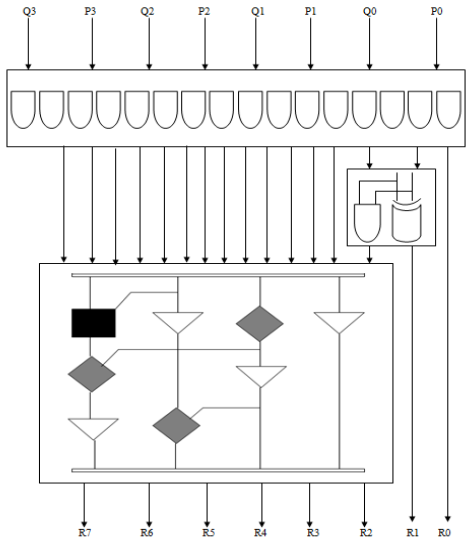

Fig. 3. Logic Diagram of Vedic Multiplier

The Brent Kung adder contain preprocessing unit, black cell, gray cell, buffer and post processing unit. With all these unit this adder performs parallel way addition, hence the this adder gives more faster result than other conventional adders. All the units of Brent Kung adder are designed with the logic gates. The half adder also constructed using logic gates.

VI. RESULTS

1. RTL Schematic & Simulation Result of High Speed 4-bit Multiplier Using Vedic Sutra

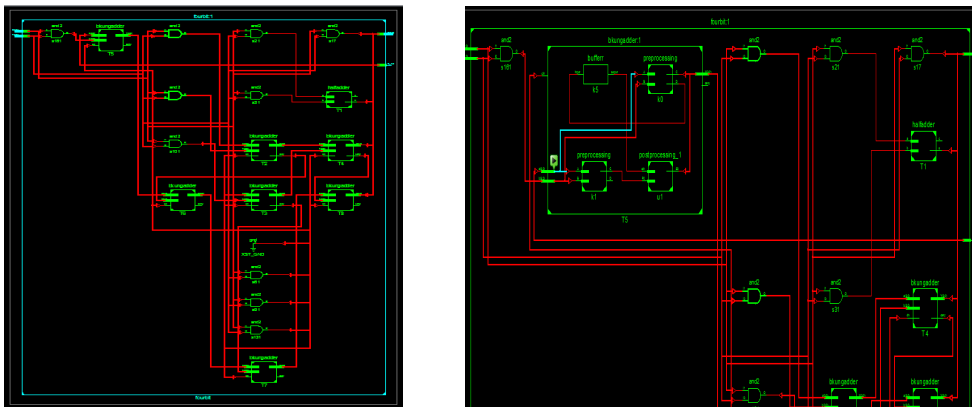

Fig. 4 RTL schematic of 4-bit multiplier

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Fig. 5 Simulation result

Register Transfer Level schematic of 4-bit High Speed Multiplier Using Vedic Sutra is as shown in Fig. 4. In the simulation result Fig. 5, P is one 4-bit multiplicand, Q is second 4-bit multiplicand, R is 8-bit multiplication result and C_out is carry generated from the multiplication.

Description-

1. P > 4-bit Input Data > 1101
2. Q > 4-bit Input Data > 1111
3. R > 8-bit Output Data > 11000011
4. C_out > carry > 1

2. Design Summery

In dissertation work 4-bit binary vedic multipler is designed using Urdhva Tiryakbhyam sutra. The 4-bit Brent Kung adder is also designed to perform the addition. The coding written in VHDL language, simulated on Xilinx software and implemented on Xilinx Digilent Nexys 3 Spartan 6 (Family), xc6slx16-3csg324 FPGA device.

From design summery we come to know the total delay of Vedic Multiplier is 9.113nsec. The number of slice LUT's are 17 out of 9112 and also the number of IOB's are 17 out of 232. Table 1 shows comparison proposed work with Vedic Multiplier designs using ripple carry adder and look ahead adder in terms of No. of Slices, No. of LUT's, No. of IO's and Computational Delay.

Parameters	In Proposed design(4-bit)	Vedic Multiplier with ripple carry adder[7]	Vedic Multiplier with carry look ahead adder[8]
1. No. of Slice LUT's	17	31	59
2. No. of IOB's	17	16	108
3. No. of IO's	17	16	64
3. Delay	9.113nsce	12.825nsec	13.786nsec

Table 1. Device Utilization Summery

Table 1 shows comparison proposed work with Vedic Multiplier designs using ripple carry adder and look ahead adder in terms of No. of Slices, No. of LUT's, No. of IO's and Computational Delay.

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VII. CONCLUSION

In this paper, implementation of High Speed Multiplier Using Vedic Sutra is presented. The Urdhva Tiryakbhyam sutra from vedic mathematics is used to implement this multiplier. The Brent Kung adder is used to improve the performance of multiplier. The path delay for proposed 4x4 bit vedic multiplier is found to be 9.113nsec. Our primary purpose is reduce delay is finally fulfilled. Higher bit Vedic binary multiplier can be implemented using Urdhva Tiryakbhyam sutra. The coding written in VHDL language, simulated on Xilinx software and implemented on Xilinx Digilent Nexys 3 Spartan 6 (Family), xc6slx16-3csg324 FPGA device.

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