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High Gain DC-DC Converter with Dual Coupled Inductors

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ABSTRACT - High voltage gain dc–dc converters are required in many industrial applications such as photovoltaic and fuel cell energy systems, high-intensity discharge lamp (HID), dc back-up energy systems, and electric vehicles. This paper presents a novel input-parallel output-series boost converter with dual coupled inductors and a voltage multiplier module. On the one hand, the primary windings of two coupled inductors are connected in parallel to share the input current and reduce the current ripple at the input.On the other hand, the proposed converter inherits the merits of interleaved series-connected output capacitors for high voltage gain, lowoutput voltage ripple, and lowswitch voltage stress. Moreover,the secondary sides of two coupled inductors are connected in series to a regenerative capacitor by a diode for extending the voltage gain and balancing the primary-parallel currents. In addition, the active switches are turned on at zero current and the reverse recovery problem of diodes is alleviated by reasonable leakage inductances of the coupled inductors. Besides, the energy of leakage inductances can be recycled.

KEYWORDS*:* DC–DC converter, dual coupled inductors, high gain, input-parallel output-series

I. INTRODUCTION

Nowadays high voltage gain DC-DC converters are required in many industrial applications.Photovoltaic energy conversion systems and fuel-cell systems usually need high step up and large input current dc-dc converters to boost low voltage (18-56 V) to high voltage (200-400 V) for the grid-connected inverters.High-intensity discharge lamp ballasts for automobile headlamps call for high voltage gain DC-DC converters to raise a battery voltage of 12 V up to 100 V at steady operation. Also, the low battery voltage of 48 V needs to be converted to 380 V in the front-end stage in some uninterruptible power supplies and telecommunication systems by high step-up converters.Theoretically, a basic boost converter can provide infnite voltage gain with extremely high duty ratio. In practice, the voltage gain is limited by the parasitic elements of the power devices, inductor and capacitor. Moreover, the extremely high duty cycle operation may induce serious reverse-recovery problem of the rectifer diode and large current ripples, which increase the conduction losses. On the other hand, the input current is usually large in high output voltage and high power conversion, but low-voltage-rated power devices with small on resistances may not be selected since the voltage stress of the main switch and diode is, respectively, equivalent to the output voltage in the conventional boost converter.Many other converter topologies have developed for high step up gain. Here a high gain input-parallel output-series DC-DC converter with dual coupled inductors is designed.This confguration inherits the merits of high voltage gain, low output voltage ripple, and low voltage stress across the power switches.Moreover, the converter is able to turn ON the active switches at zero current and alleviate the reverse recovery problem of diodes by reasonable leakage inductances of the coupled inductors.

II. OPERATION OF THE CONVERTER

Equivalent circuit of the converter is as shown in Figure 2.1.The converter is operated in continous conduction mode(CCM).The duty cycles of the power switches are interleaved with 180^0 phase shift,and the duty cycles are greater than 0.5.Therefore the two switches can only be in one of three states as S_1 : ON, S_2 : ON; S_1 : ON, S_2 : OFF; S_1: OFF, S_2 : ON.This ensures normal transmission of energy from the coupled inductor's primary side to the secondary one.
The converter is operated in continous conduction mode.Operation of the converter can be explained through eight modes.

Mode 1 [$t_0 - t_1$] :

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At time t = t_0 , the power switch S_1 is turned on with zero-current switching (ZCS) due to the leakage inductance L_{K1},while S_2 remains turned ON, as shown in Figure 3.1. Diodes D_1,D_2 , and D_r are turned OFF, and only output diode D_3 is conducting. The current falling rate through the output diode D_3 is controlled by the leakage inductances L_{K1} and L_{K2},which alleviates the diode's reverse recovery problem. This stage ends when the current through the diode D_3 decreases to zero.

Mode 2 [$t_1 – t_2$] :

During this interval, both the power switches S_1 and S_2 are maintained turned ON, as shown in Figure 3.2. All of the diodes are reversed-biased. The magnetizing inductances L_{m1} and L_{m2} as well as leakage inductances L_{K1} and L_{K2} are linearly charged by the input voltage source V_{in}.This period ends at the instant t_2 , when the switch S_2 is turned OFF.

Mode 3 [$t_2 – t_3$] :

At time t = t_2 , the switch S_2 is turned OFF, which makes the diodes D_2 and D_r turned ON. The current flow path is shown in Figure 3.3. The energy that magnetizing inductance L_{m2} has stored is transferred to the secondary side charging the capacitor C_r by the diode D_r , and the current through the diode D_r and the capacitor C_r is determined by the leakage inductances L_{K1} and L_{K2}.The input voltage source, magnetizing inductance L_{m2} and leakage inductance L_{K2} release energy to the capacitor C_2 via diode D_2.

Mode 4 [$t_3 – t_4$] :

At time t = t_3 , diode D_2 automatically switches OFF because the total energy of leakage inductance L_{K2} has been completely released to the capacitor C_2 . There is no reverse recovery problem for the diode D_2 . The current flow path of this stage is shown in Figure 3.4. Magnetizing inductance L_{m2} still transfers energy to the secondary side charging

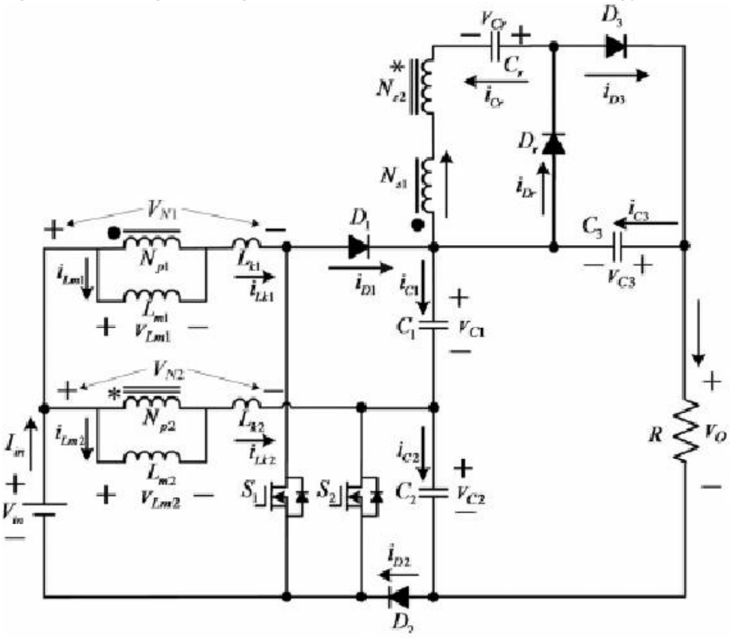

Fig. 2.1 The equivalent circuit of the converter

the capacitor C_r via diode D_r . The current of the switch S_1 is equal to the summation of the currents of the magnetizing inductances L_{m1} and L_{m2}.

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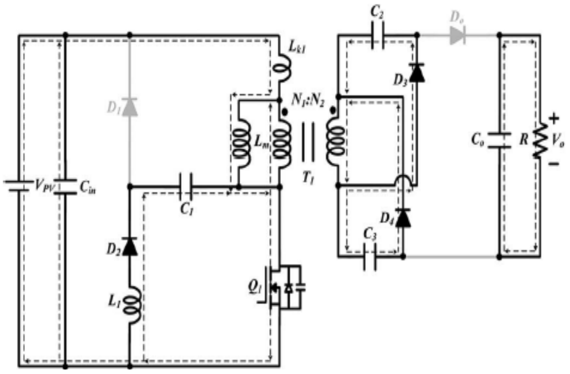

Fig 3.1 : mode 1

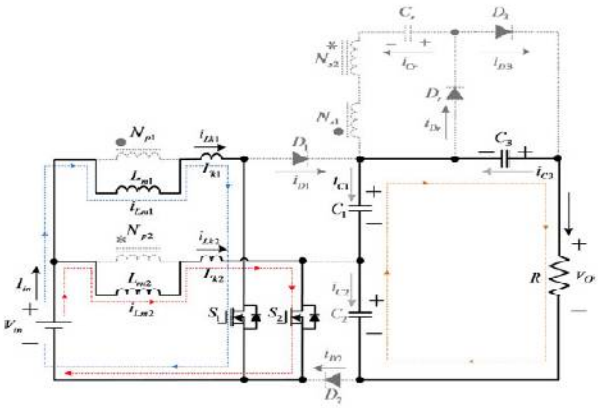

Fig 3.2 : mode 2

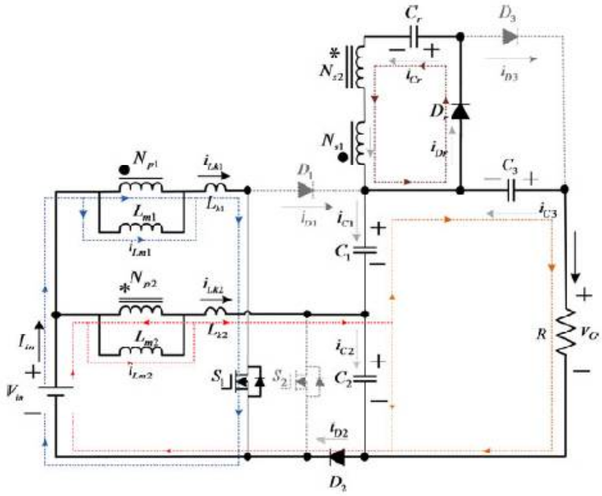

Fig 3.3 : mode 3

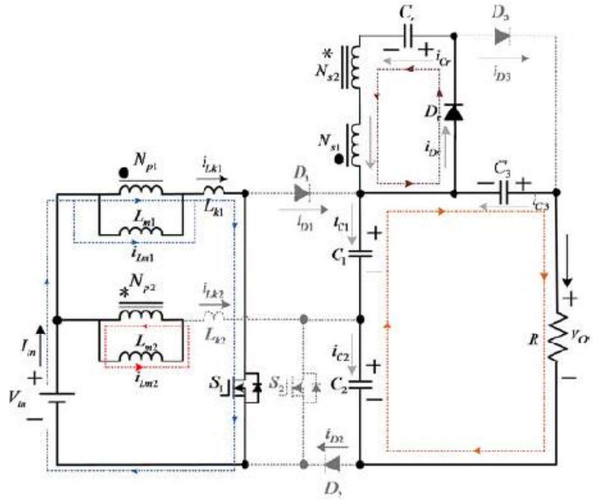

Fig 3.4 : mode 4

Mode 5 [$t_4 – t_5$] :
At time t = t_4 , the switch S_2 is turned ON with ZCS soft-switching condition.Due to the leakage inductance L_{K2} and the switch S_1 remains in ON state.The current flow path of this stage is shown in Figure 3.5. The current falling rate through the diode D_r is controlled by the leakage inductances L_{K1} and L_{K2},which alleviates the diode reverse recovery problem. This stage ends when the current through the diode D_r decreases to zero at t = t_5.
Mode 6 [$t_5 – t_6$] :
The operating states of stages 6 and 2 are similar as shown in Figure 3.6. During this interval, all diodes are turned OFF. The magnetizing inductances L_{m1} and L_{m2} , and the leakage inductances L_{K1} and L_{K2} are charged linearly by the input voltage. The voltage stress of D1 is the voltage on C1 , and the voltage stress of D2 is the voltage on C2 . The voltage stress of D_r is equivalent to the voltage on C_r , and the voltage stress of D_3 is the output voltage minus the voltages on C_1 and C_2 and C_r .
Mode 7 [$t_6 – t_7$] :
The power switch S_1 is turned OFF at t = t_6 , which turns ON D_1 and D_3 , and the switch S_2 remains in conducting state. The current flow path of this stage is shown in Figure 3.7. The input voltage source V_{in} , magnetizing inductance L_{m1} and leakage inductance L_{K1} release their energy to the capacitor C_1 via the switch S_2 . Simultaneously, the energy stored in magnetizing inductor L_{m1} is transferred to the secondary side. The current through the secondary sides in series flows to the capacitor C_3 and load through the diode D3.

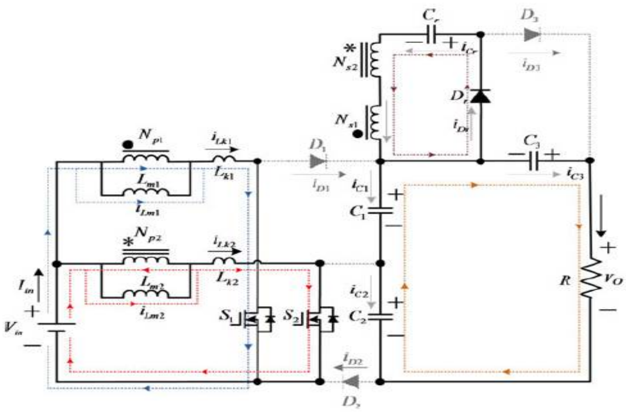

Fig 3.5 : mode 5

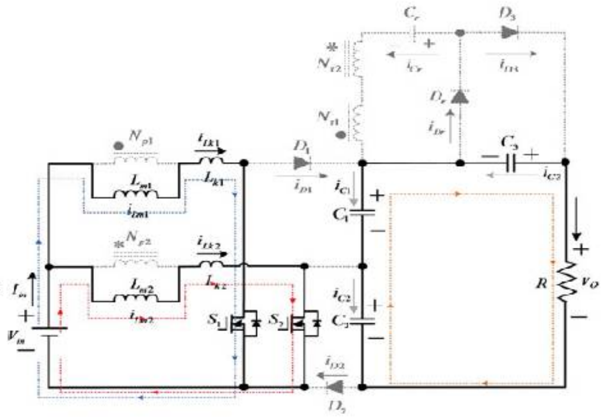

Fig 3.6 : mode 6

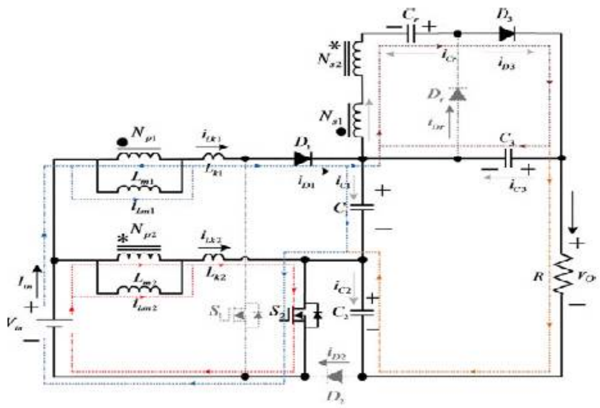

Fig 3.7 : mode 7

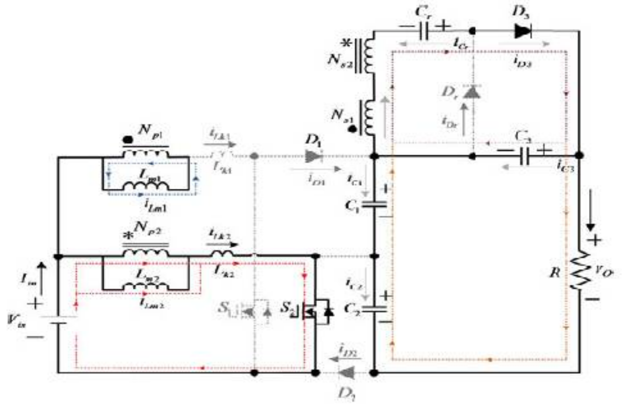

Fig 3.8 : mode 8

Mode 8 [$t_7 – t_8$] :

At time t = t_7 , since the total energy of leakage inductance L_{K1} has been completely released to the capacitor C_1 , diode D_1 automatically switches OFF as shown in Figure 3.8. The current of the magnetizing inductance L_{m1} is directly transferred to the output through the secondary side of coupled inductor.

III.STEADY STATE ANALYSIS OF THE CONVERTER

To simplify the circuit performance analysis of the converter in continous conduction mode, the following assumptions are made.

1. All of the power devices are ideal. That is to say, the on-state resistance $R_{DS(ON)}$ and all parasitic capacitors of the main switches are neglected,and the forward voltage drop of the diodes is ignored.
2. The coupling-coefficient k of each coupled inductor is defined as $L_m/(L_m+L_K)$. The turn ratio N of each coupled inductor is equal to N_S /N_P .
3. The parameters of two coupled inductors are considered to be the same, namely $L_{m1} = L_{m2} = L_m$, $L_{K1} = L_{K2} = L_K$, $N_{S1}/N_{P1} = N_{S2}/N_{P2} = N$, and $k_1 = L_{m1}/(L_{m1} + L_{K1}) = k_2 = L_{m2}/(L_{m2} + L_{K2}) = k$.
4. Capacitors C_1, C_2, C_3 , and C_r are large enough. Thus, the voltages across these capacitors are considered as constant in one switching period.
5. The time durations of modes I, IV, V, and VIII are significantly short, hence only stages II, III, VI, and VII are considered for the steady-state analysis.

A Voltage gain

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If the transient characteristics of circuit are disregarded, each magnetizing inductance has two main states in one switching period. In one state, the magnetizing inductance is charged by the input source. In the other state, the magnetizing inductance is discharged by the output capacitor voltage V_{C1} or V_{C2} minus the input voltage.

At stages II and VI, following equations can be written

$$V_{Lm1}^{II} = V_{Lm1}^{VI} = kV_{in} \quad (1)$$
$$V_{Lm2}^{II} = V_{Lm2}^{VI} = kV_{in} \quad (2)$$
$$V_0 = V_{C1} + V_{C2} + V_{C3} \quad (3)$$

At mode III, the following equations are written.

$$V_{Lm1}^{III} = kV_{in} \quad (4)$$
$$V_{Lm2}^{III} = k(V_{in} - V_{C2}) \quad (5)$$
$$V_{Cr} = V_{S1} - V_{S2} = kNV_{C2} \quad (6)$$

During the time duration of mode VII, the following voltage equations can be expressed.

$$V_{Lm1}^{VII} = k(V_{in} - V_{C1}) \quad (7)$$
$$V_{Lm2}^{VII} = kV_{in} \quad (8)$$
$$V_{C3} = V_{Cr} + V_{S2} - V_{S1} = kN(V_{C1} + V_{C2}) \quad (9)$$

Using the volt-second balance principle on L_{m1} and L_{m2} respectively, voltage across capacitors are obtained as

$$V_{C1} = V_{C2} = \frac{V_{in}}{(1-D)} \quad (10)$$
$$V_{Cr} = \frac{kNV_{in}}{(1-D)} \quad (11)$$
$$V_{C3} = \frac{2kNV_{in}}{(1-D)} \quad (12)$$

Hence voltage gain can be written as

$$M_{CCM} = \frac{V_0 2(kN+1)}{V_{in}(1-D)} \quad (13)$$

Neglecting the impact of leakage inductances of the coupled inductor,coupling coefficient k is equal to one.Thus ideal voltage gain is rewritten as

$$M_{CCM} = \frac{V_0 2(N+1)}{V_{in}(1-D)} \quad (14)$$

B Voltage and current stress analysis

To simplify the voltage stress analyses of the components, the leakage inductance of coupled inductor and the voltage ripples on the capacitors are ignored. The voltage stresses on power switches S_1 and S_2 are derived as

$$V_{S1-stress} = V_{S2-stress} = \frac{V_{in}}{(1-D)} = \frac{V_0}{2(1+N)} \quad (15)$$

This confirms that low-voltage-rated metal-oxide-semiconductor field-effect transistors with low $R_{DS(ON)}$ can be adopted for the proposed converter to reduce conduction losses and costs.The voltage stresses on the diodes D_1,D_2,D_3 , and D_r related to the turns ratio and the output voltage can be derived as

$$V_{D1-stress} = \frac{2V_{in}}{(1-D)} = \frac{V_0}{(1+N)} \quad (16)$$
$$V_{D2-stress} = \frac{V_{in}}{(1-D)} = \frac{V_0}{2(1+N)} \quad (17)$$
$$V_{D3-stress} = V_{Dr-stress} = \frac{2NV_{in}}{(1-D)} = \frac{NV_0}{(1+N)} \quad (18)$$

The average currents of the diodes D_1,D_2,D_3 , and D_r can be derived

$$I_{D1} = I_{D2} = I_{D3} = \frac{V_0}{(1-D)R} \quad (19)$$

Similarly, according to the steady operating principle, the average currents of the power switches are given by

$$I_{S1} = \frac{D}{(1-D)} I_{D1} = \frac{DV_0}{(1-D)^2 R} \quad (20)$$
$$I_{S2} = \frac{D}{(1-D)} I_{D2} + \frac{1}{(1-D)} I_{D1} = \frac{(D^2-D+1)V_0}{(1-D)^2 R} \quad (21)$$

IV.SIMULATION AND RESULTS

Simulations were done to test the performance of the converter by using simulink/MATLAB software. Circuit used for simulation is as shown in Figure 5.1. Gate pulses to the two power switches generated are given in Figure 5.2.

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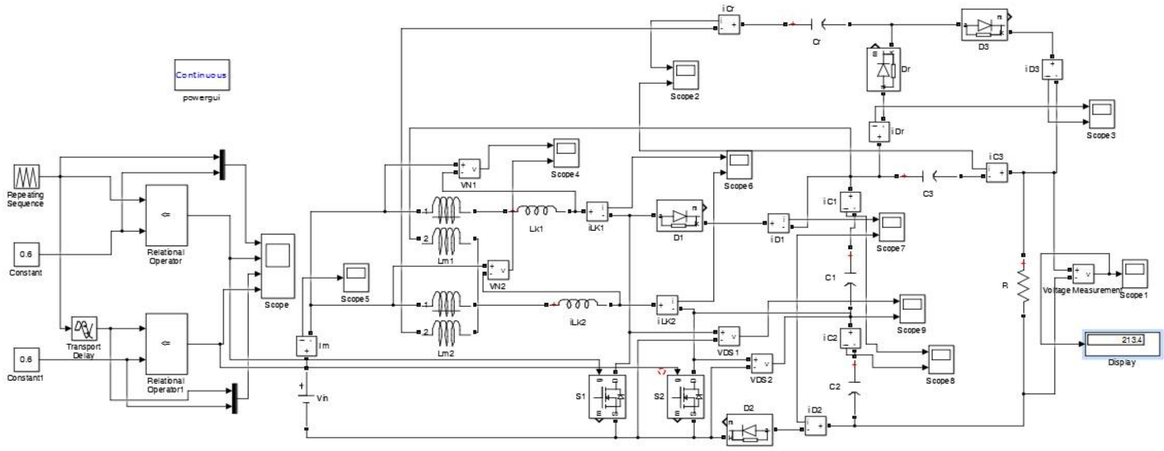

Fig 5.1 Simulation circuit of converter

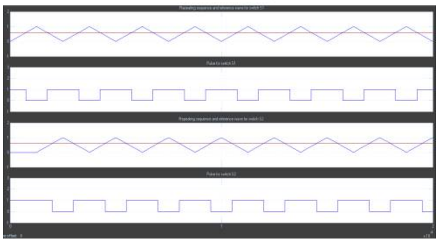

Fig 5.2 Switching pulses

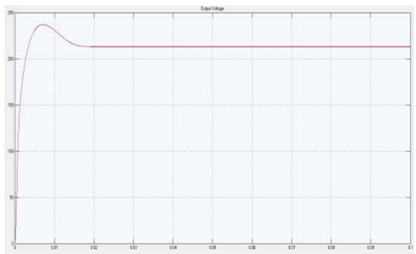

Fig 5.4: Output voltage waveform

V .CONCLUSION

For low input-voltage and high step up power conversion, this paper has successfully developed a high-voltage gain dc–dc converter by input-parallel output-series and inductor techniques. The key theoretical waveforms, steady-state operational principle, and the main circuit performance are discussed to explore the advantages of the proposed converter.Performance of the converter is simulated using MATLAB/SIMULINK software.From simulation circuit,we can see that the converter can achieve a much higher voltage gain and avoid operating at extreme duty cycle and numerous turn ratios.The main switches can be turned ON at ZCS so that the main switching losses are reduced.The current falling rates of the diodes are controlled by the leakage inductance so that the diode reverse-recovery problem is alleviated.

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