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A Novel Voltage Multiplier for High Voltage/ Low Current Applications

Soumya Simon[2], Shebin Rasheed[1]

Assistant Professor, Dept. of Electrical and Electronics, FISAT, Angamaly, Kerala, India[2]

M.Tech Scholar, Dept. of Electrical and Electronics, FISAT, Angamaly, Kerala, India[1]

ABSTRACT: Voltage multiplier circuit are widely used in many high-voltage/low-current applications. A conventional symmetrical voltage multiplier (SVM) has much better performance, when compared with its half-wave counterpart. However, it requires a high-voltage transformer (HVT) with center-tapped secondary to perform its push pull kind of operation. The design of an HVT with center-tapped secondary is relatively complex. This paper proposes a hybrid SVM (HSVM) for dc high-voltage applications. The multiplier is formed by cascading a diode-bridge rectifier and an SVM with diode-bridge rectifier as the first stage of multiplier. The proposed topology saves two high-voltage capacitors and requires only one secondary winding of HVT. Besides, it has lesser voltage drop and faster transient response at start-up, when compared with conventional SVM. The feasibility of the proposed HSVM is validated both by simulation and experimental results of a laboratory scaled-down prototype.

KEYWORDS: DC high voltage, hybrid, transient response, voltage drop, voltage multiplier.

I.INTRODUCTION

High voltage dc power supplies are widely used in many applications, such as particle accelerators, lasers systems, X-ray systems, electron microscopes, photon multipliers, electrostatic systems, etc. There are two basic approaches that are generally used to generate dc high voltage for high-voltage/low-current applications. In the first approach, a high-voltage transformer (HVT) with high turn ratio and diodes with high breakdown voltage are used. However, an HVT with high turn ratio is undesirable because it exacerbates transformer non idealities. These non-idealities cause voltage and current spike, and increase loss and noise. The second approach is to use the voltage multiplier circuit on the secondary side of HVT. By using a voltage multiplier circuit, the turn ratio of HVT and thus the aforementioned non-idealities can be greatly reduced.

This original voltage multiplier circuit was of half-wave type, and suffers from several problems such as large output voltage ripple and output voltage drop. To overcome these problems, a symmetrical voltage multiplier (SVM) was developed by Heilpern in 1954 by adding an additional oscillating column of capacitors and a stack of rectifiers. It was thought that SVM has a push pull kind of operation. For this kind of operation, two ac sources, out of phase by 180, were required. Therefore, an HVT with center-tapped secondary was used to operate SVM in push pull manner.A fully balanced SVM normally has much better performance, when compared with a half wave multiplier (i.e., it has significantly smaller voltage ripple, voltage drop, and higher output power). However, the use of HVT with center-tapped secondary windings has two drawbacks. First, it increases the complexity oftransformer winding, and second, any asymmetry between the output voltages (driving voltages) of the two secondary windings may give rise to fundamental and higher order odd harmonics in the dc output of SVM. Such harmonics are inversely proportional to load current, and it is difficult to eliminate them. In this paper, a hybrid SVM (HSVM) is proposed, which has better performance, lesser component counts, and complexity.

III.DESCRIPTION AND OPERATION OF HSVM

Figure 3.1 shows the circuit diagram of the proposed n-stage HSVM. It consists of an input ac source V (t), HVT, bridge rectifier with a filter capacitor C1, and an (n 1)-stage SVM. The first stage of the proposed topology is a

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diode-bridge rectifier and the remaining n 1 stages form an SVM. The first stage of the proposed topology does not have coupling capacitors; therefore, it saves two high-voltage capacitors (i.e., it needs only 3n2 capacitors). As the proposed topologyis a combination of diode-bridge rectifier and SVM, it is named as an HSVM. The secondary winding of HVT is connected in parallel to diode bridge rectifier and SVM. Thus, both the diode-bridge rectifier and SVM are driven in parallel by the input supply voltage Vxy(t). However, their output terminals are connected in series; therefore, the total output voltage of the proposed topology is equal to the sum of the output voltages of the diode-bridge rectifier and SVM. The key steady-state waveforms of the proposed HSVM are shown in Figure 3.2. In steady-stateoperation, the capacitors of the smoothing column will discharge through theload and recharge to peak value twice every cycle of the input voltage.

Thus, there exist two charging modes (modes 1 and 3) and two discharging modes (2 and 4) in one complete cycle of operation. During modes 1 and 3, the capacitors of the smoothing column are charged in parallel by the currents (i1, i2, . . ., in) and (I1, I2, . . . , In), respectively, whereas during modes 2 and 4,the capacitors of the smoothing column are discharged in series through the load. The equivalent circuits related to these charging and discharging modes are shown in Figure 3.2.As the first stage of the proposed HSVM is directly connected (without coupling capacitors) to the input ac source, its smoothing capacitor charges to peak value within the first half cycle of the input voltage. On the other hand, in conventional SVM, the smoothing capacitor of first stage takes two to three cycles to charge to peak value due to the limited rate of charge transfer from the coupling capacitors of this stage. Consequently, the proposed HSVM has slightly faster transient response at start-up, when compared with conventional SVM.

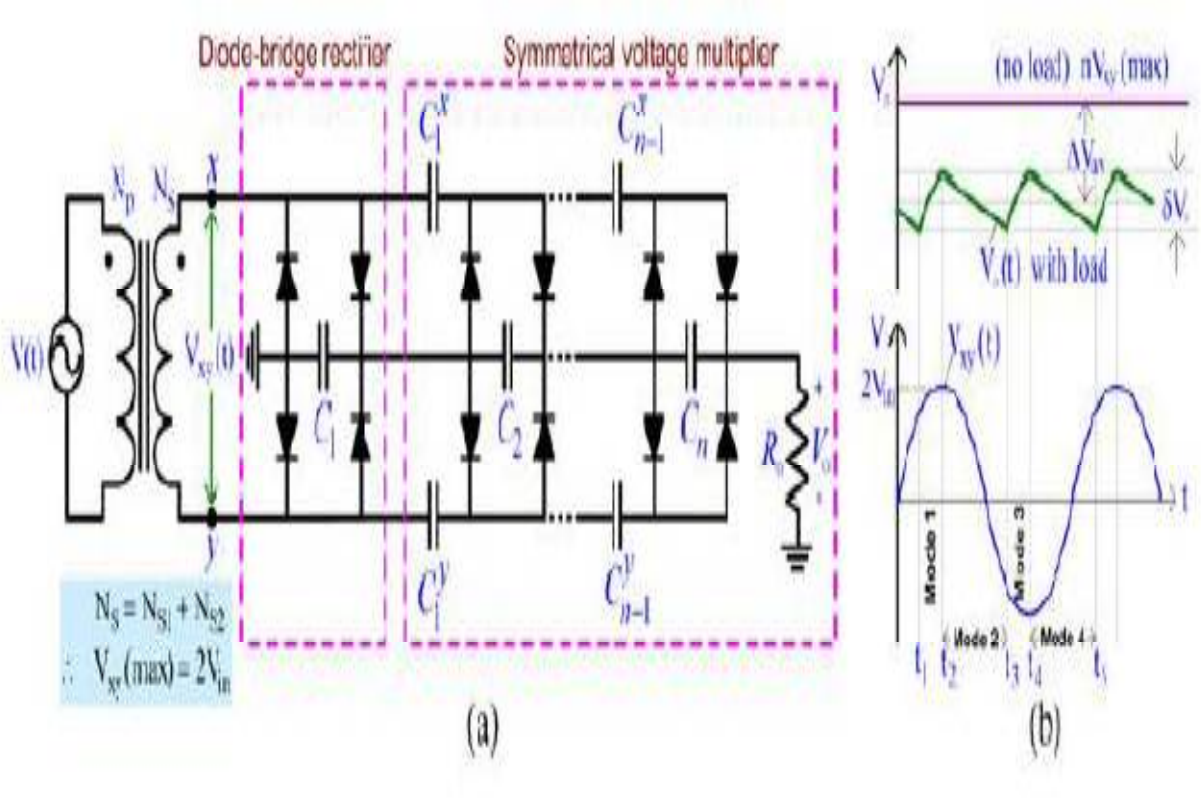

Figure 3.1: (a) Proposed hybrid symmetrical voltage multiplier and (b) key steady-state waveforms.

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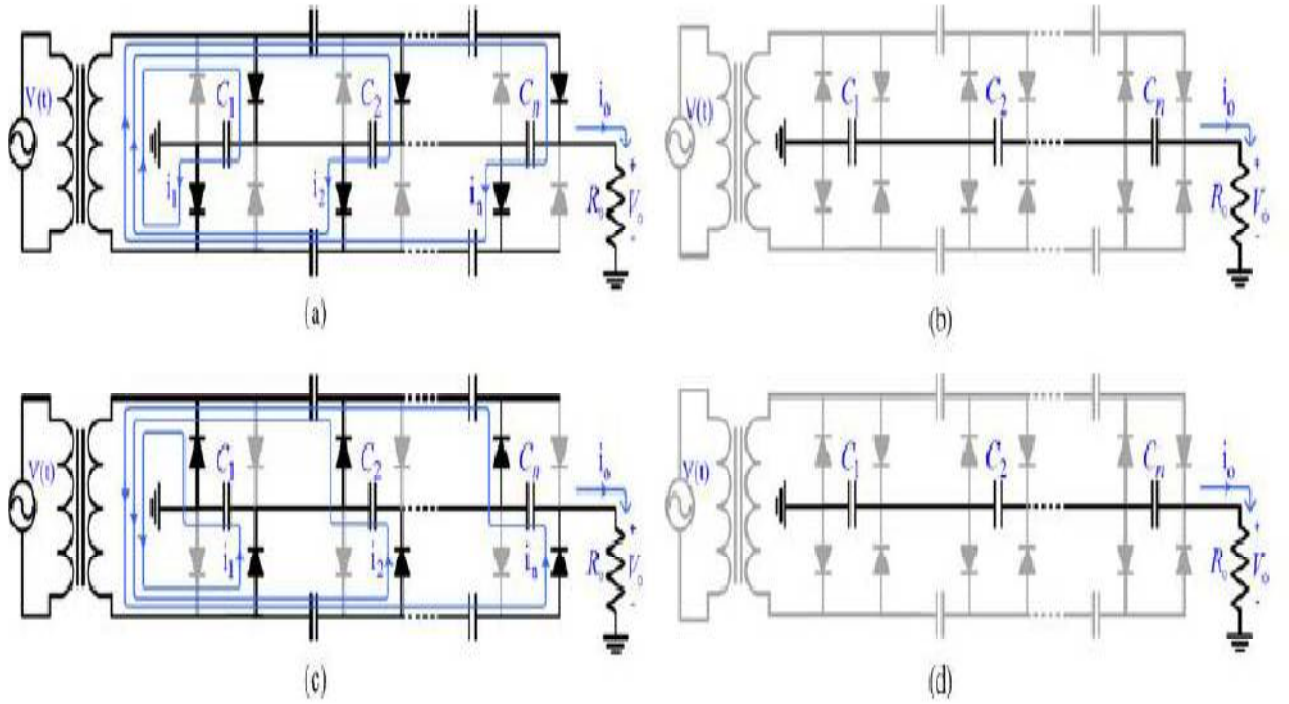

Figure 3.2: Equivalent circuits for various modes of operation: (a) mode 1 (t1-t2), (b) mode 2 (t2-t3), (c) mode 3 (t3-t4), and (d) mode 4 (t4-t5).

Thus, the analytical results reveal that the voltage produced by the proposed HSVM is approximately 460 V higher than that produced by the conventional SVM for the aforementioned specifications. As the load resistance is equal, the output power of the proposed HSVM and conventional SVM is 22.58 and 17.20 W, respectively. Hence, the proposed topology also has higher output power under the same input and output conditions than the conventional SVM. Both the proposed HSVM and conventional SVM were simulated using MATLAB, and the obtained results are presented in Figure 5.1. and Figure 5.2. Figure 4.1. shows the transient output responses of HSVM at start-up. The proposed topology stabilizes its output voltage approximately 200 _S earlier than the conventional one. Thus, the transient response of the output voltage of the proposed HSVM is slightly faster, when compared with conventional SVM. This is due to the reason that in the proposedHSVM,it saves two high power capacitors normally coupling capacitors.

IV. SIMULATION RESULTS

A. Simulation Results

The performance of the proposed HSVM was first evaluated on the basis of computer simulation using MATLAB software. The specifications of the simulation circuits were as follows: the frequency of ac voltage f = 40 kHz; capacitance ofmultiplier capacitors C = 10 nF; number of stages n = 4; and load resistance R = 105 k ohm. The input driving voltages for both the multipliers were equal. For the proposed HSVM, VS (max) = 450 V, and for conventional SVM, VS1(max)= VS2(max) = 225 V (i.e., Vxy(max) = 450 V). we found that the average output voltage is 1000 and 1460 V for the conventional SVM and proposed

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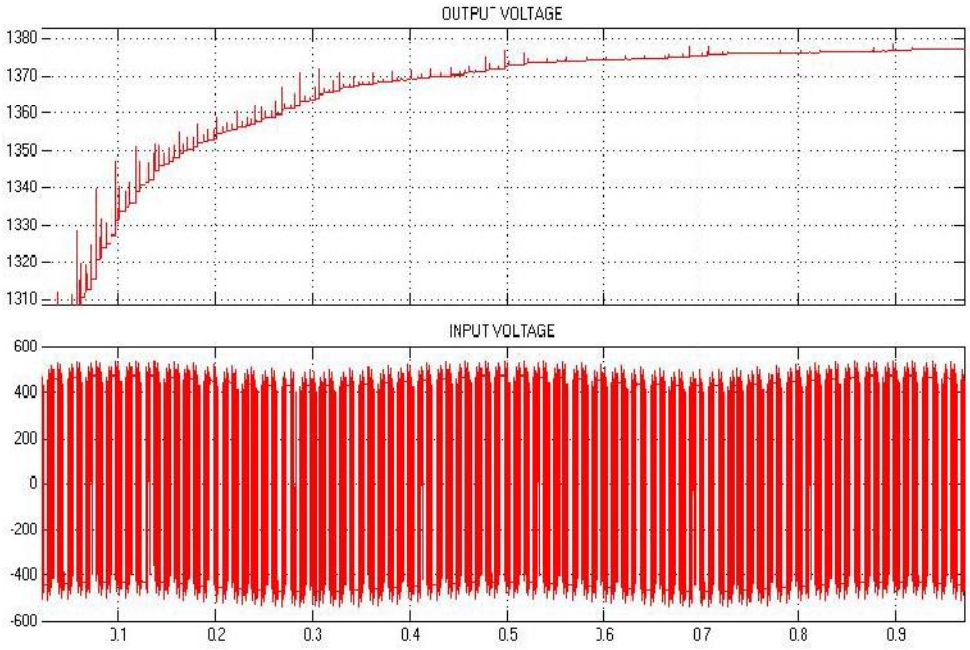

Figure 4.1: (a) Simulated output and input voltage waveforms during the start-up process of HSVM

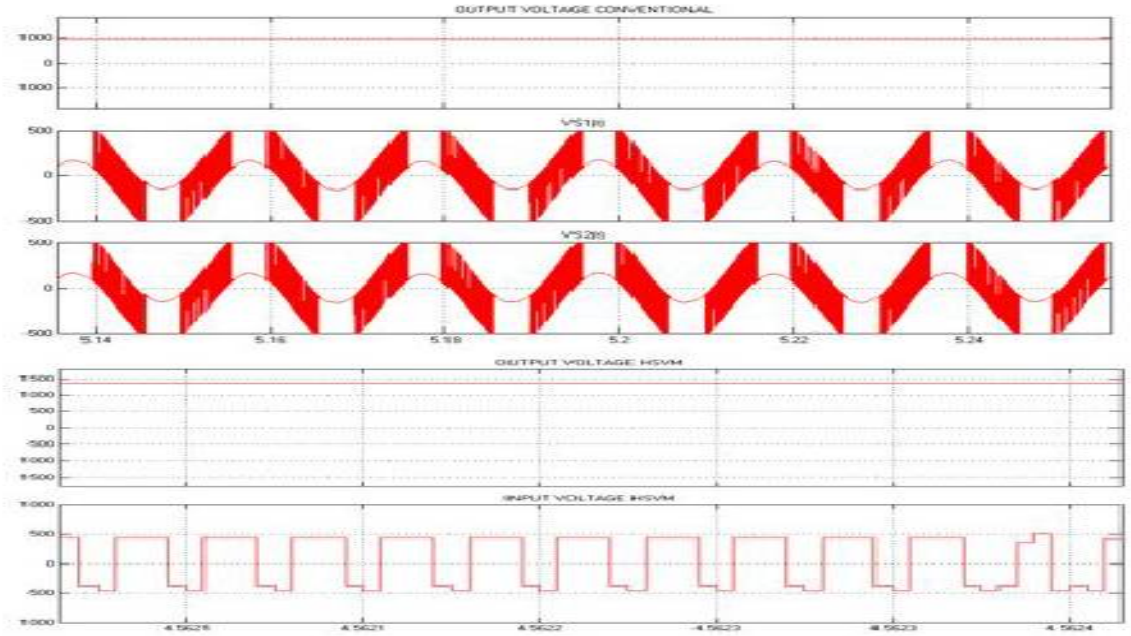

Figure 4.2: Simulated output and input voltage waveforms in steady state of conventional and proposed HSVM

HSVM, the smoothing capacitor of first stage is charged to peak value during the first half cycle of the input voltage VS (t), whereas in the conventional SVM, several cycles are required to charge up to the peak value of the input voltagedue to limited rate of charge transfer from the coupling capacitors of first stage. Figure 4.2 shows the steady-

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state output and input voltage waveforms of both the multipliers. The output voltages of the proposed HSVM and conventionalSVM are 1460 and 1000 V, respectively.

The output load current for the proposed and conventional topologies is 14.7 and 12.82 mA, respectively. Thus, the output power of proposed and conventional topologies is 22.70 and 17.28W, respectively. This proves that the proposed topology has less voltage drop and higher outputpower. The peak-peak voltage ripple in the dc output of the proposed topology and conventional SVM is 50 and 42V, respectively, and is slightly greater in the proposed topology because of high load current. Thus, the simulation results are completely in agreement with the analytical ones.

B. Experimental Results

Finally, a low-power prototype of the proposed HSVM was implemented for experimental verification. The high-frequency ac input driving voltage VS(t) was obtained by implementing a zero-current switching (ZCS) series resonant inverter with open-loop control. The output voltage was varied by varying the switching frequency of the converter. The switching signals for ZCS-inverter were obtained by using an ARDUINO UNO board. The schematic circuit diagram of the experimental prototype is shown in

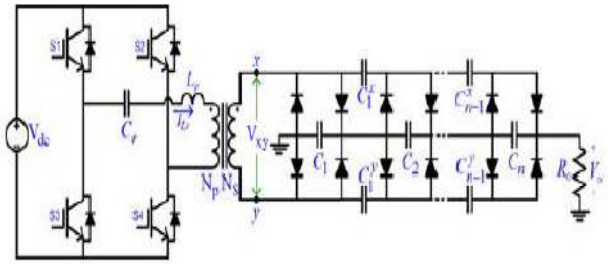

Figure 4.3: Schematic circuit diagram of the experimental prototype.

Figure 4.3. The specifications of the experimental prototype are as follows: input dc voltage Vdc = 30 V; capacitance of the resonant capacitor Cr = 100 nF; turn ratio of high-frequency transformer n = 1:15; leakage inductance of high-frequency transformer Lr = 15 _H; switching frequency of high-frequency inverter fS = 40 kHz; capacitance of multiplier capacitors C = 10 nF; total number of stages n = 4; and output load resistance Ro = 105 k. A prototype of the conventional SVM was also implemented with same specifications for the purpose of comparison. Figure 5.3shows the experimental prototype of the proposed HSVM and conventional SVM, respectively. The values of the input dc voltage, switching frequency of ZCS-SR inverter, and output load resistance are the same for both the multipliers. It can be observed that the transient rise time for the proposedmultiplier is 375 microsec; whereas it is approximately 475 microsec for the conventional multiplier. This proves that the transient response of the proposed multiplier is slightly faster than that of the conventional SVM, and the reason for this observation is explained earlier.

VI. CONCLUSION

An HSVM has been proposed for dc-high-voltage applications. It was formed by cascading a diode-bridge rectifier and an SVM. The circuit topology, operation, and steady-state analysis have been described in detail. The proposed topology has been found to have smaller voltage drop, faster dynamic response, lesser component count, and lesser complexity, when compared with the conventional SVM. The feasibility of the proposed HSVM has been validated both by simulation and experimental results of a laboratory scaled-down prototype. Both the simulation and experimental results confirmed the superior performance of the proposed topology. Thus, the proposed topology may be considered as a better alternative to the conventional SVM.

REFERENCES

[1] "*Theoretical performance of voltage multiplier circuits*", IEEE J. Solid-State Circuits, vol. SSC-6, no. 3, pp. 132135, Jun. 1971.
[2]"*Topological generation and analysis of voltage multiplier circuits*", IEEE Trans. Circuits Syst., vol. CAS-24, no. 10, pp. 517530, Oct. 1977.
[3] "*Low-ripple compact high-voltage dc power supply*", IEEE Trans. Ind. Appl., vol. 42, no. 5, pp. 11391145, Sep./Oct. 2007.

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[4] "*A three-phase symmetrical multistage voltagemultiplier"*, IEEE Power Electron. Lett., vol. 3, no. 1, pp. 3033, Mar. 2005.
[5] G. K. Singh, R. Besar, and G. Muhammad, "*A cascaded three-phase symmetrical voltage multiplier*", J. Instrum., vol. 1, no. 10, p. T10001, Oct. 2006.
[6] "*Analysis of CockcroftWaltonvoltagemultipliers with an arbitrary number ofstages*", Rev. Sci. Instrum., vol. 40, no. 2, pp. 330333, Feb. 1969.
[7] "*Theoretical performance of the capacitor diode voltage multiplier fed by a current source"*, IEEE Trans. Power Electron., vol. 8, no. 2, pp. 147155, Apr.1993.
[8] P. G. Maranesi, and L. Radrizzani,"*Small-signal model of the Cockcroft Walton voltage multiplier"*, IEEE Trans. Power Electron., vol. 9, no. 1, pp. 1825, Jan. 1994.
[9]"*The dynamics of the Cockcroft Walton voltage multiplier"*, in Proc. 21st Annu. IEEE Vol. Power Electron. Spec. Conf., Jun. 1114, 1990, pp. 485490.