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Efficient Bridgeless Topology for Power Factor Correction Applications

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ABSTRACT: Passive and active power factor correction (PFC) methods are commonly used for power factor correction. Most of the PFC rectifier utilizes a boost/buck-boost topology converter at their front end for power factor correction due to its high power factor capability. A conventional PFC scheme has lower efficiency due to losses in the diode bridge. Compared with other single phase bridgeless topologies, the proposed bridgeless resonant pseudoboost converter topology has the merits of less component counts and absence of input diode bridge. The proposed converter topology is designed to work in resonant mode . By implementing the pseudoboost topology the power factor can be improved close to unity. As an application, bridgeless resonant pseudoboost converter is fed to electronic ballast for fluorescent lighting. The performance of this converter can be verified by using SIMULINK/MATLAB.

KEYWORDS: Bridgeless rectifier, Power factor correction (PFC), Total harmonics distortion (THD), Low conduction losses, electronic ballast.

I.INTRODUCTION

Power factor correction is applied to different applications such as in electrical power transmission utilities to improve stability and efficiency, or individual electrical customers to reduce the cost. Power factor correction is the method of correcting power factor close to unity. Active and passive power factor correction techniques are used for linear and nonlinear loads [4].Passive PFC can be achieved simply by using passive components such as resistors, inductors and capacitor (filters). Filters reduce the harmonic current, which means that the nonlinear loads now looks like linear loads. PFC using high current inductors and capacitor banks are expensive. PFC Passive PFC has some limitations such as poor dynamic response, lack voltage regulation, solutions based on filters are heavy and bulky and the shape of input current depends on the load. Passive PFC is not as effective as active PFC due to these limitations. Active power factor corrector changes the wave shape of current drawn by a load to improve PF using switching devices such as MOSFETs and IGBTs. The purpose of this method is to make the power factor corrected load circuitry appear as purely resistive. In this case, both voltage and current are in phase and reactive power consumption is zero. Boost converter topology is widely used for active power factor correction. This topology provides a higher output voltage than input voltage. Some other active PFC converters are buck, buck-boost, flyback, forward, cuk, sepic and zeta converters. The main drawback of buck-boost topology is that the reversing of polarity of its output voltage. Boost converter are superior to other dc-dc converters due to linearity of current and voltage [8]. All of these active PFC converters use bridge topology at their front end which cause more conduction losses.

Bridgeless topology is introduced to reduce the component count and THD compared to conventional bridge topology [1], [5],[10],[16]. The bridgeless topology eliminates one diode from the current path compared to conventional bridge topology and reduces conduction losses. The bridgeless boost topology requires an additional boost gate drive transformer or two inductors [7],[9],[11],[13],[15]. The bridgeless boost topology work only in DCM and CCM boundary. THD is high in bridgeless boost topology and power factor obtained is 0.888.

These are the limitations of bridgeless boost converter. The power factor can be increased by using bridgeless buck-boost converter topology. This topology works in DCM and CCM mode only. The power factor obtained by this converter is 0.9766, but the THD is high [6].Comparing with existing bridgeless topology, the proposed bridgeless resonant pseudoboost PFC rectifier has the advantages of less component counts [1]. The proposed topology has high power density and low conduction losses. This topology operates in DCM, CCM and resonant modes. The resonant

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mode operation gives the advantages of ZC turn ON in power switch and ZC turn OFF in the output diode. Previous topologies have the limits of high component counts, complex control, lack galvanic isolation, requirements of additional diodes due to floating ground. This topology reduces the complexity of control circuit.The proposed bridgeless resonant pseudoboost PFC converter is fed to electronic ballast for fluorescent lighting. Conventional electronic ballast uses a self- oscillating half bridge series-parallel resonant converter [2],[3]. But the limitations of the conventional topology are low PF and high THD. These problems are avoided by using PFC converters. The bridgeless resonant pseudoboost PFC converter is an efficient topology for this purpose compared to other PFC topologies.

II.PRINCIPLE OF OPERATION OF BRIDGELESS RESONANT PSEUDOBOOST PFC RECTIFIER

The new bridgeless resonant pseudoboost PFC rectifier shown in Fig.1 is designed to operate in discontinuous mode (DCM) during switch turn- ON and in resonant mode during the switch turn – OFF intervals. The switch current stress of proposed converter is similar to that of conventional DCM PFC converter and the switch voltage stress is higher. The two power switches Q1 and Q2 can be driven by the same control signal to reduce the complexity of control circuitry. However, the power switch Q1requires an isolated gate drive.

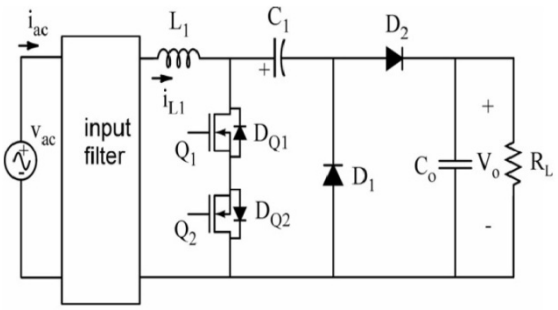

Fig.1. Bridgeless resonant pseudoboost PFC rectifier

Referring to Fig.1 the switching conduction sequence during positive ac-line cycle is Q1-DQ2, D2, D1, R_L and during negative ac-line cycle is Q2-DQ1, D1, D2, R_L. Thus the current path goes through only two or one semiconductor devices instead of three during each switching period T_s. This will result in low conduction losses compared to the conventional bridgeless PFC converter. By operating the converter in DCM, several advantages such as natural near-unity PF, ZC turn- ON of power switches, ZC turn- OFF of output diodes can be gained. Thus the losses due to switching turn- ON and the reverse recovery of the output diodes are reduced. But the increased current stress during DCM operation leads to one disadvantage of the DCM operation, which limits its use to low power applications.

III.MODES OF OPERATION

Assuming the circuit is operating in DCM, the circuit operation during one switching period Tsin a positive half cycle can be divided into four operating modes.

Stage I: Q_1 is ON

Stage I: [T_0-T_1] is shown in Fig.2. This stage starts when the switch Q1 is turned- ON. The body diode of Q2 is forward biased by the inductor current i_{L1}. Diode D1 and D2 are reverse biased by the voltage V_{c1} and (V_{c1}+ V_0) respectively. Here, the current through L_1 increases linearly with input voltage V_{ac}. The voltage across C_1 remains constant at voltage V_x.

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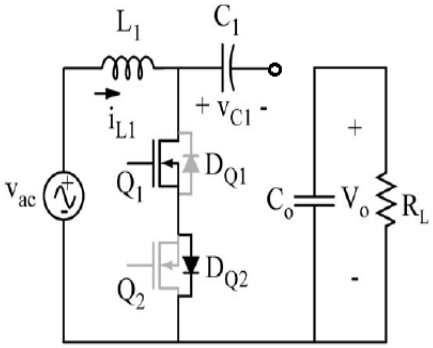

Fig.2. Topological stages over one switching period Ts for the converter when switch Q1 is on

Stage II: Q_1 is OFF

Stage II: [T_1-T_2] is shown in Fig.3. This stage starts when the switch Q2 is turned- OFF and diode D2is turned- ON simultaneously. During this interval, Diode D1remains reverse biased. The series tank (L_1,C_1) is excited by V_{ac} through Diode D2. Capacitor C_1 is charged until it reaches a peak value during this stage. This stage ends when i_{L1} reaches zero and Diode D2 turns OFF with ZC

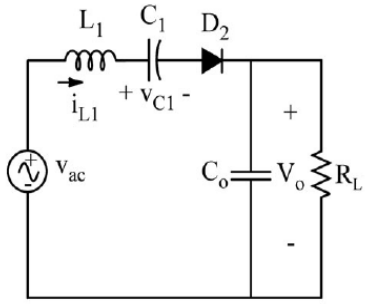

Fig.3.Topological stages over one switching period Ts for the converter when switch Q1 is OFF.

Stage III: resonant mode

Stage III: [T_2-T_3] is shown in Fig.4. Diode D1is forward biased and provides a path for resonating current i_{L1}. This stage ends when the inductor current reaches zero. The Diode D1 is switched ON and OFF under ZC condition during this stage. Assuming that the input voltage is constant, then the capacitor is discharged until it reaches a voltage V_x.

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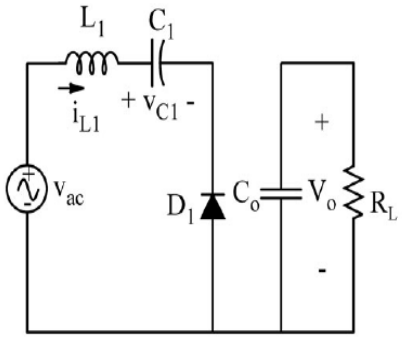

Fig.4.Topological stages over one switching period Ts for the converter under resonant mode

Stage IV: Discontinuous mode

Stage IV: [T_3-T_4] is shown in Fig.5. All switches are OFF during this stage. The inductor current i_{L1} is zero and capacitor voltage V_{c1} remains constant (V_{c1} = V_x).

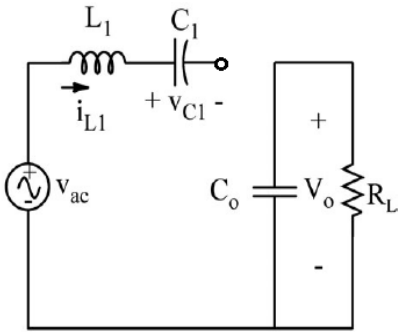

Fig. 5.Topological stages over one switching period Ts for the converter under discontinuous mode.

The corresponding theoretical waveforms over one switching period Ts for the converter during positive half cycle is shown in Fig.6. The waveform clearly indicates the charging and discharging of the inductor and capacitor through i_{L1} and V_{c1} representations.

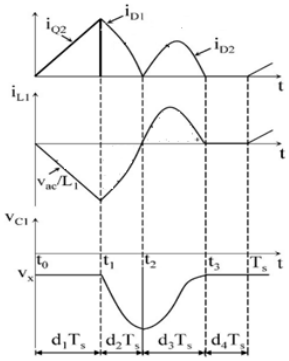

Fig.6.Theoretical waveforms for the converter

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IV. DESIGN PROCEDURE

In the design procedure of the bridgeless resonant pseudoboostconverter, the MATLAB simulink model and the simulation waveforms are presented. The converter topology has been simulated and tested using MATLAB environment.The design procedure is presented for the following power stage specifications: V_{ac} = 85Vrms, V_0= 240 V, P_{out}= 115 W, and f_s = 50 kHz. Assuming that the efficiency is 100%, the values of the circuit components are calculated as follows:

1) The voltage conversion ratio M is

$$M = \frac{V_0}{V_M} = \frac{240}{85\ X\ \sqrt{2}} = 2 \quad (1)$$

2) The normalized switching frequency (F) must be less than 1 to ensure DCM operation. Here, F=0.8.is chosen.

3) The value of the critical inductance required to maintain DCM operation,

$$L1 \leq \frac{R_L T_S}{4}\left(\frac{F}{\Pi}\right)^2 = L_{crit} = 163\mu H \quad (2)$$

L1= 100 µH is selected in this design.

4) The value of the resonant capacitance C1 is given by

$$C_1 = \frac{1}{L_{1(2\Pi f_r)2}} = 65\ nF \quad (3)$$

5) The value of dimensionless conduction parameter K is

$$K = \frac{2L_1}{R_L T_S} \quad (4)$$

Here T_S is the switching period.

6) Switch duty-cycle d1,

$$d1 = \frac{M}{\sqrt{2}\sqrt{K}} = 0.4 \quad (5)$$

Simulation parameters and specifications for the proposed converter are given in Table.1.

Table.1. Simulation Parameters and Specifications

Tank Inductor, L_1	100µH
Tank Capacitor, C_1	65nF
Filter Inductor, L_f	1mH
Filter Capacitor, C_f	1µF
Output Capacitor, C_0	470µF

V. SIMULATION RESULT AND DISCUSSION

The converter has been simulated using MATLAB for the following input and output data specifications: V_{ac} = 150 V_{rms}, V_o = 370V and f_s = 50 kHz.

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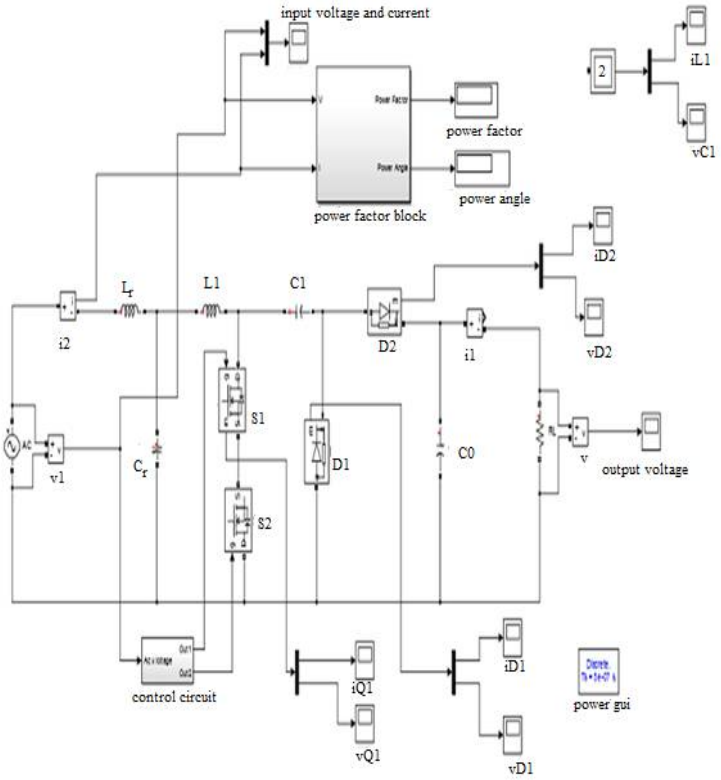

Fig.7. Simulation diagram of bridgeless resonant pseudoboost PFC rectifier

Simulation results of input and output voltages and currents of the converter are shown in Fig. 7.

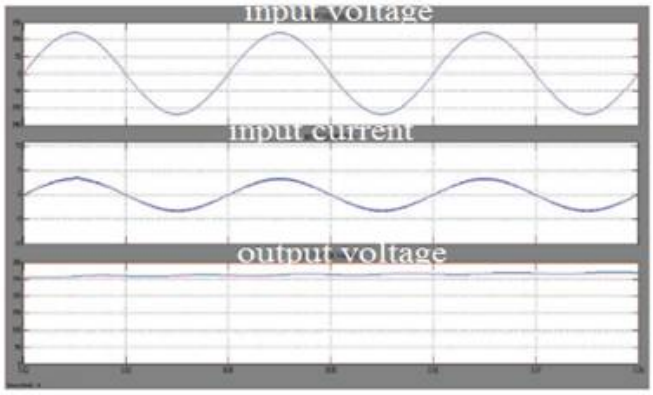

Fig.8. Input and output voltages and currents of the bridgeless modified SEPIC PFC converter fed induction motor drive

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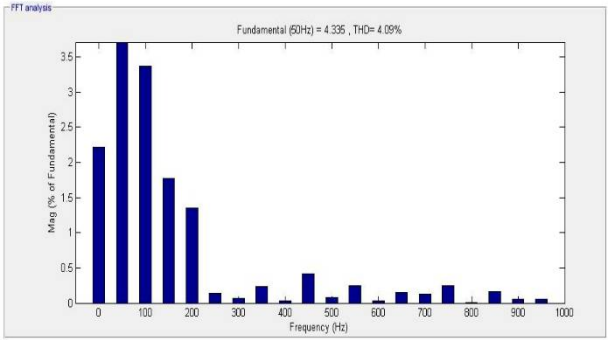

Fig.9. Measured harmonic content of input line

THD of the input line current is shown in Fig.8. It is evident from Fig.9 that the calculated results are well below the allowable limits of class D standard.

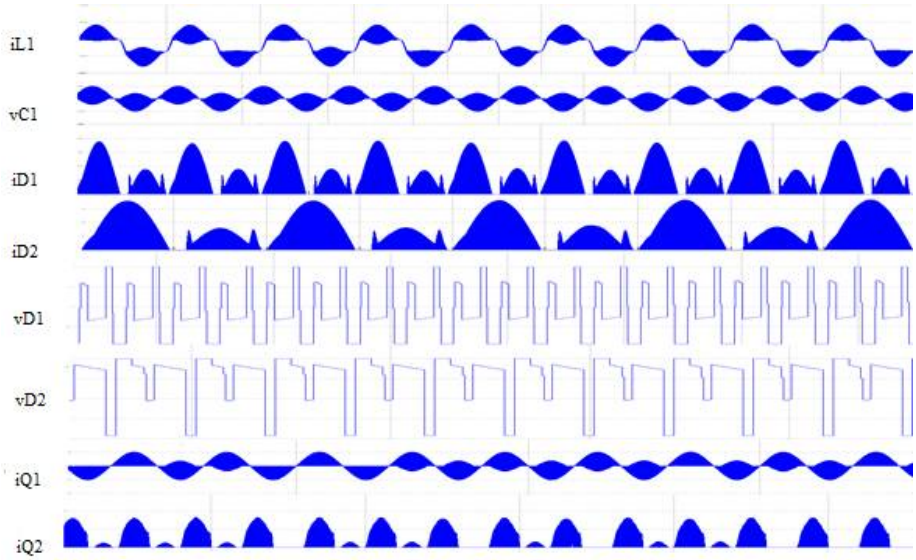

Fig.10. Simulated waveforms for the converter

The waveforms of i_{L1} and V_{c1} during a few switching periods is shown in fig.8. The current waveforms of diodes D1 and D2 shown in fig.8 shows that both diodes D1 and D2 are turned OFF under zero current conditions. It is clear that the switch Q1 turn ON under ZC condition. The current and voltage waveform of Q1 is also shown in fig.8.

VI.EXPERIMENTAL RESULTS

As seen from Fig.6, the input voltage and input current are in phase and almost sinusoidal. Therefore power factor will be almost unity. Output voltage and output current are V_{out} = 375 V, I_{out} = 0.7A respectively.

VII.CONCLUSION

Efficient bridgeless topology based on bridgeless resonant pseudoboost PFC converter has been presented. The proposed converter has low components and the components are fully utilized over the whole line cycle. The two

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power switches in the proposed topology can be driven by the same control signal, which significantly simplifies the control circuitry. It maintains efficiency at full load higher than 95% during the entire line voltage range. Although the discontinuous input current for the proposed converter may result in larger filter, the low component count and the high efficiency in universal-line range makes the proposed topology a good candidate for low-power PFC applications. The MATLAB simulink model and the simulation waveforms obtained are presented. From the simulation results we can see that a power factor of 0.998 is obtained that is almost close to unity. The converter topology is simulated and tested using MATLAB Simulink environment.

REFERENCES

1. Abbas A. Fardoun, Esam H. Ismail, Mustafa A. Al-Sa_ar and Ahmad J. Sabzali, ―A Bridgeless Resonant Pseudoboost PFC
2. Rectifer‖ IEEE Trans. Power Electron., vol. 29, no.11, pp. 384397, Nov 2014.
3. Ashish Shrivasthava and Bhim Singh, ' Power Quality Improvement using Buck-Boost Converter for Fluorescent Lighting' Insian Institute of Technology,IEEE ICSET 2012, Nepal
4. Arnaldo J Perin, Joable Andrade Alves, and Ivo Barbi, 'An Electronic Ballast with High Power Factor For Compact Fluorescent Lamps, INEP-Power Electronics Institute, Brazil, 0-7803-3544-9/96 IEEE
5. Azazi H.Z,EL Kholy E.E, Mahmoud S.A.and Shokralla S.S (2010) 'Review of Passive and Active Circuits for Power Factor Correctors in Single Phase, Low Power AC- DC Converters', Cairo University, Egypt, December 19-21,2010, paper ID 154.
6. Cao Taiqiang, Chen zhagyong, Wang Jan, Sunzhang, Luo Qian and Zhang Fei (2014) 'Study on a Novel High Efficiency Bridgeless PFC Converter',Xihua university China VOL 14, Article ID 514281
7. Daoshen Chen, Jih-Sheng Lai, 'Design Consideration for Power Factor Correction Boost Converter Operating at the Boundary of Continuous Conduction Mode and Discontinuous Conduction Mode',0-7803-0982-0193,IEEE
8. Gopinath. M and Yogeetha. D (2009) 'Efficiency Analysis of Bridgeless PFC Boost Convertor', Bharath University Chennai, and Ganadipathy Tulsis Engg Collge, Chennai ISSN 0975 - 6450 VOL 1 NO 3
9. Huai wei and Issa Bataresh (1998) 'Comparison of Basic Converter Topologies for Power Factor Correction', University of Central Florida, Orlando ,0-7803-4391-3/98 IEEE
10. Kavithamani K, Vigneswari S (2013) 'High Powerfactor Boost Converter with Bridgeless Rectifier' ,Anna University Chennai,
11. 2278-1676 Volume 4, Issue 3 (Jan. - Feb. 2013), PP 33-38
12. Kiran Mohan. M.N, Nisha B Kumar(2014) 'Single Phase Bridgeless SEPIC Converter with high power factor' ,Govt CET, Kannur,Volume 2, Issue 6, September 2014, PP 117-126
13. Laszlo Huber, Yungtaek Jang and Milan M. Jovanovic (2008) 'Performance Evaluation of Bridgeless PFC Boost Rectifier', Delta Products Corporation Power Electronics Laboratory USA VOL.23, NO.3
14. Mohammad Mahadavi and Hosein Farzanehfard(2011) 'Bridgeless SEPIC PFC Rectifier With Reduced Components and Conduction losses', Isfahan University, Iran.VOL. 58, NO.9
15. Neethu Pavoo P, Rajesh P(2014) 'Bridgeless High Efficiency Boost Rectifier for Energy Harvesting', University of Calicut,Volume 2 Issue 1, January 2014
16. Robert C. N. Pilawa Podgurski, Anthony D. Sagneri, Juan M. Rivas, David I. Anderson, David J. Perreault (2007) 'Very High Frequency Resonant Boost Converters', Massachusetts Institute of Technology, Massachusetts,1-4244-0655-2/07
17. Suja C Rajappan, K. Sarabose, Neetha John (2012) 'An Efficient AC/DC PFC Boost Converter', Sri sakti Institute of Engineering and Technology Coimbatore, ISSN 2278-3806
18. Yungtaek Jang and Milan M. Jovanovic (2011) Bridgeless High Power Factor Buck Converter, Delta Products Corporation VOL.26, N0.2