ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

*An ISO 3297: 2007 Certified Organization* *Vol. 5, Special Issue 3, March 2016*

National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE'16)

Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India

On 17th & 18th March 2016

# A Modified Cascaded Multilevel Inverter Using Reduced Switches

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**ABSTRACT**: A cascaded multilevel inverter with a different unit is proposed. By series connection of voltage sources and switches, a cascaded multilevel inverter that only generates positive levels at the output is introduced. An additional voltage source with two unidirectional switches is also added to this cascaded unit to obtain a minimum voltage level as the magnitude of this additional voltage source. A H-Bridge is also added to the proposed inverter to generate all (positive and negative) voltage levels. The comparison of this unit with conventional inverter is also performed on the basis of total harmonic distortion and switching units. MATLAB Simulink model of the unit is evaluated for verifying the results. A 13-level inverter is verified using MATLAB and harmonic spectrum also analyzed.

**KEYWORDS:** cascaded multilevel inverter, total harmonic distortion, fundamental frequency switching, reduced switch count topology, symmetric and asymmetric inverter.

## I. INTRODUCTION

Because of energy crisis present in the current scenario, the renewable energy sources have significant application in various fields. Multilevel inverters are incorporating with renewable energy sources since they can produce high power from the medium voltage sources. Several topologies for multilevel inverters have been introduced in recent years for producing system with more efficient, cost effective as well as high quality and lower harmonics. The cascaded inverters generally use less number of components like diodes and capacitors as compared to other topologies such as capacitor clamped or diode clamped inverters, because it only use switches and DC sources[1]. Several configurations on cascaded inverters were also innovated for reducing the switches and DC sources used. The main features of this inverter are that modularity, simplicity of control, and reliability and they requires a very low number of switches[2].

This paper introduces a configuration of cascaded multilevel inverters for the aim of reducing the number of switching components, thereby a total reduction in power circuitry and installation space. By this configuration, only positive levels are obtained at the output side, hence an H-Bridge is added to the unit for positive and negative levels. This circuit can work as both symmetric and asymmetric multilevel inverter with, having same magnitudes for DC sources and different magnitudes for DC sources respectively. The asymmetric multilevel inverter generates the highest number of levels, hence the different algorithms and configuration results large number of output levels with less number of switches[3].

While discussing about the multilevel inverters, lowering of total harmonic distortion is an important topic since they can achieve a minimum lower order harmonics and higher quality sinusoidal output voltage. It is important to note that this topology uses unidirectional switches, because bidirectional switch requires two IGBTs, two antiparallel diodes, and one driver circuit if a common emitter configuration is used [4-6].

The control of power semiconductor devices also performs a high role in decreasing the power losses of switches, use of filters and total harmonic distortion (THD). This circuit uses a fundamental switching method with very low THD, is a major feature of this circuit.

## II. PROPOSED TOPOLOGY

A basic circuit of cascaded multilevel inverter as shown in fig.1, it consists of five switches and three DC sources in series. The number of levels can be increased by connecting switches and DC source again series to this basic

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configuration as shown in fig2. But an additional DC source is connected to this whole circuit by two unidirectional switches, and the magnitude of this voltage source is the minimum voltage level produced at the output as well as this additional configuration will also help to increase the number of levels.

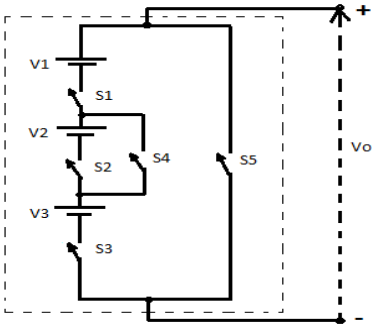


Fig. 1. Basic circuit of multilevel inverter

Considering the fig.1, the simultaneous switching of the switches (S2, S4), (S1, S2, S3, S5) and (S1, S3, S4, S5) should avoid for preventing the short circuiting of DC voltage sources, and for the fig.2 the switches (S3, S6), (S2, S3, S4, S7), (S1, S2, S3, S4, S5, S8) and the switches of additional unit (S1',S2') also should not turn on at a time. A H-Bridge is also connected to the output with positive levels for generating both positive and negative levels.The switching states of fig.1 by considering all the criteria is shown in table.1.
The maximum voltage obtained at the input of H-bridge is the sum of all outputs as follows:

$$V_{O(t)} = V_{O,1}(t) + V_{O,2}(t) + \cdots + V_{O,n}(t) + V'_O(t) \quad (1)$$

Where $V_{O,1}(t)$, $V_{O,2}(t)$,... $V_{O,n}(t)$ are the voltage generated due to each switching configuration and $V'_O(t)$ is the voltage of additional unit.

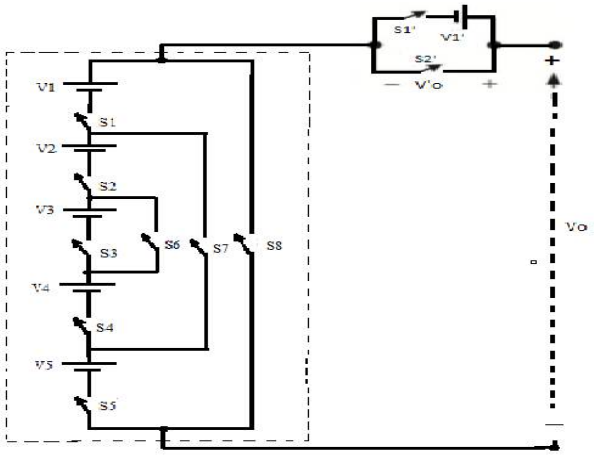


Fig. 2. 7-level configuration with additional unit

The blocking voltage of semiconductor switches is also an important factor that determines the switching rates and hence the cost of switches. There by calculation of maximum blocking voltage is necessary for a multilevel inverter, the switches S1' and S2' holds a blocking voltage of V1'.

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Table 1. Switching states of basic unit

| State | Switching State | | | | | Vo |
|---|---|---|---|---|---|---|
| | S1 | S2 | S3 | S4 | S5 | |
| 1 | Off | Off | Off | Off | On | 0 |
| 2 | On | Off | On | On | Off | V1+V3 |
| 3 | On | On | On | Off | Off | V1+V2+V3 |

The number of levels in this cascaded multilevel inverter can also be increased by connecting in series the basic unit shown in fig.1. By using the same switching provided in table.1, we can develop any number of levels as required. Bt if doing so, the number of switching devices used by the circuit is high as comparing with the developed configuration shown in figure.2.

Table.2. Switching states of 7-level inverter

| State | Switching State | | | | | | | | | | Vo |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | S1' | S2' | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | |
| 1 | Off | On | Off | Off | Off | Off | Off | Off | Off | On | 0 |
| 2 | On | Off | Off | Off | Off | Off | Off | Off | Off | On | V1' |
| 3 | Off | On | On | Off | Off | Off | On | Off | On | Off | V1+V5 |
| 4 | On | Off | On | Off | Off | Off | On | Off | On | Off | V1'+V1+V5 |
| 5 | Off | On | On | On | Off | On | On | On | Off | Off | V1+V2+V4+V5 |
| 6 | On | Off | On | On | Off | On | On | On | Off | Off | V1'+V1+V2+V4+V5 |
| 7 | On | Off | On | On | On | On | On | Off | Off | Off | V1'+V1+V2+V3+V4+V5 |

The table 2. Shows the switching states of 13-level inverter shown in fig. 2, but that configuration, generate positive 7-level output unless an H-Bridge added to it as in fig.3.

If the number of DC source is N by excluding the additional source, the switches S1 to SN have maximum blocking voltages V1, (V1+V2)... (V1+V2+… (VN\2))… (V1+V2), V1 respectively. And the switches S (N+1), …S (N+3) will have blocking voltage of V1, (V1+V2)… (V1+V2+…+VN) respectively. But the switches of H-Bridge has all the maximum output voltage blocking voltage.

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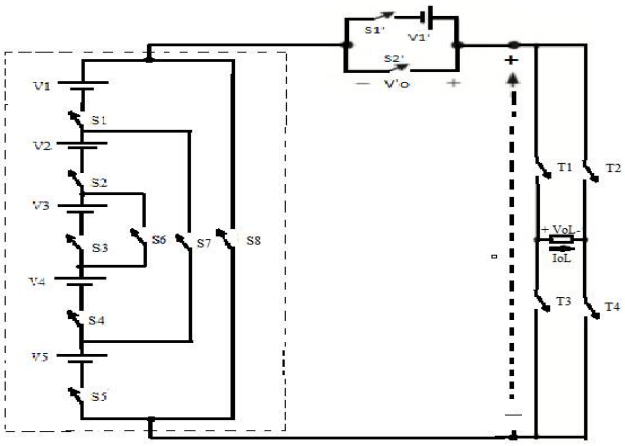


Fig. 3. 13-level multilevel inverter

## III. SIMULATION AND RESULTS

Working on 13-level inverter using this model is evaluated by using the software MATLAB Simulink model and the diagram is shown in fig.3, the voltage with 13 levels and current obtained successfully. The load used is resistance-inductor with values 70 ohms and 55mH.

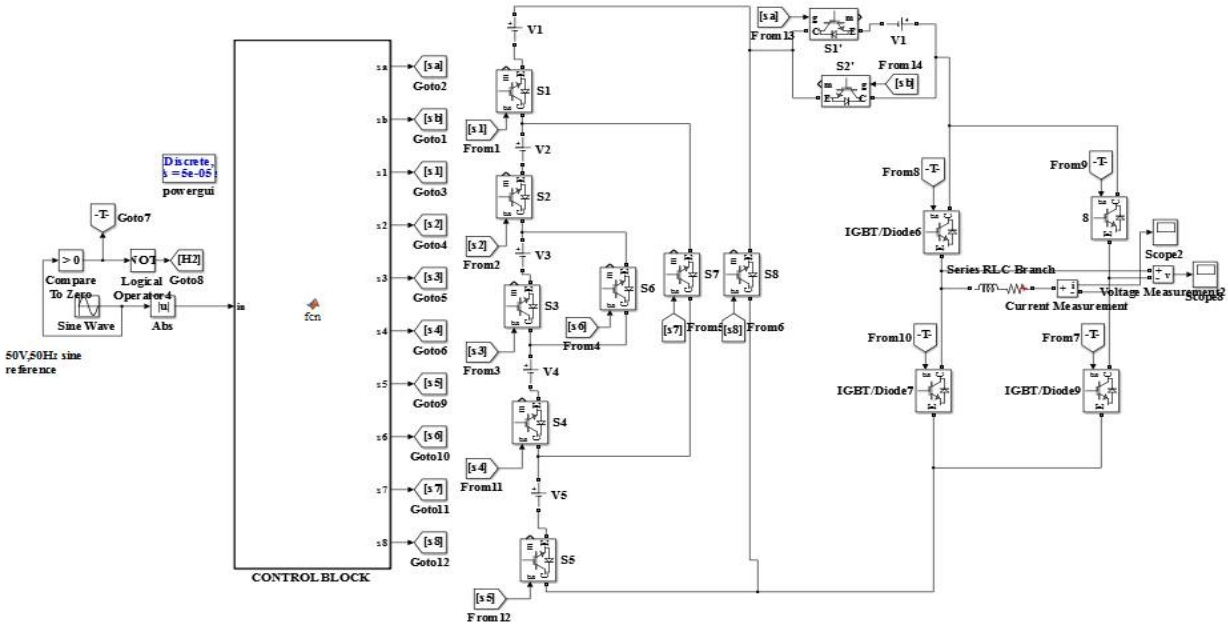


Fig. 3 MATLAB Simulink model 13-level multilevel inverter

The symmetric configuration is used here with magnitudes of voltage sources as 20V and the output voltage will have a maximum amplitude of 120V and a current of 1. 7 amperes.

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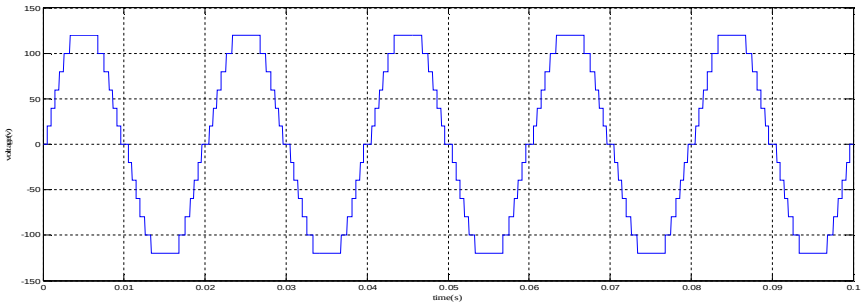


Fig. 4 Output voltage waveform of 13-level multilevel inverter

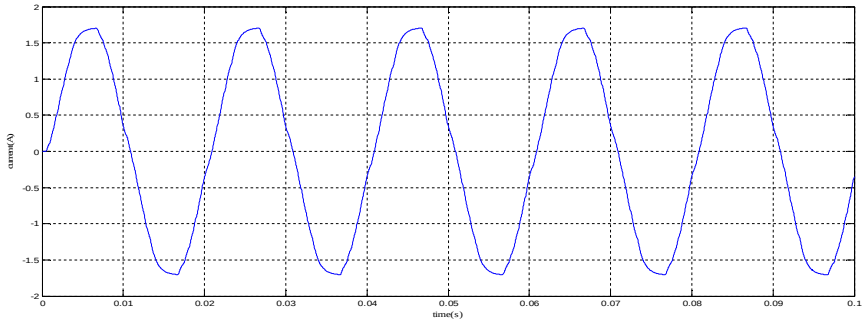


Fig. 5 Output current waveform of 13-level multilevel inverter

The harmonic spectrum of voltage and current is analyzed by using FFT analysis, and it can be seen that voltage distortion of 7.60% and that of the current 3.23% is only present in the outputs as shown in fig6 and fig.7. So very less distorted outputs are achieved even though normal fundamental frequency control technique is used for switching. The distortion will further decrease to increase the number of levels and the switches used by the circuit for high level is very less as compared to conventional cascaded multilevel inverters.

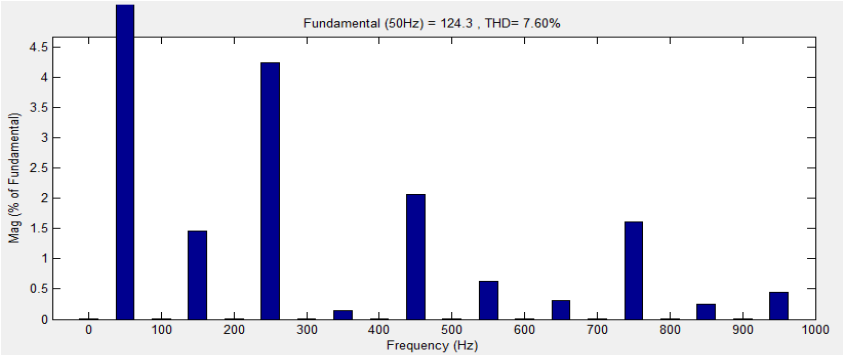


Fig. 6 Harmonic spectrum of output voltage waveform of 13-level multilevel inverter

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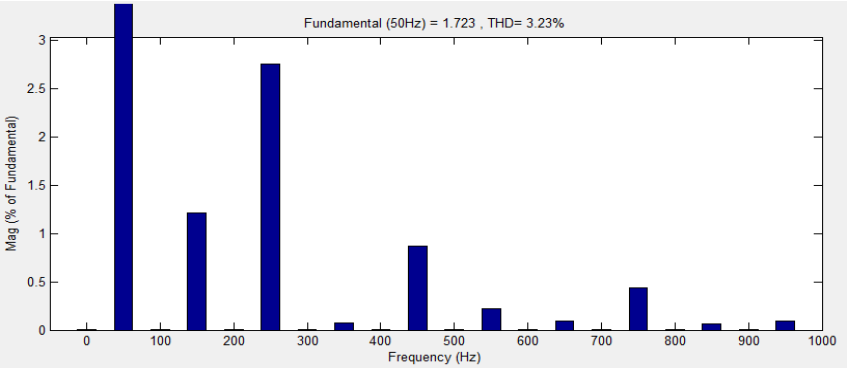


Fig. 7 Harmonic spectrum of output current waveform of 13-level multilevel inverter

## IV. CONCLUSION

A basic unit with very low number of switches introduced in this paper, which can act as both symmetric and asymmetric configurations based on the magnitude of DC sources. Since this unit can only generate positive levels, an H-Bridge is added to this unit for producing sinusoidal like waveforms. The levels can further increase by adding voltage sources and switches in series to the basic unit. The MATLAB Simulink model of 13-level cascaded multilevel inverter is performed and harmonic analysis is carried out for evaluating the THD of waveforms. The number of switches used by the unit is very less for higher levels and the input DC source used have low magnitude.

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