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# Single Active Switch Power Electronics for Kilowatt Scale Capacitive Power Transfer

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**ABSTRACT:**Contactless power transfer is of two types; Inductive power transfer (IPT) and Capacitive power transfer (CPT). IPT is the dominant means of power transfer. IPT is suited where the power transfer distance is small to large. IPT uses magnetic flux while CPT uses electrical flux to couple across the gap. Nowadays, capacitive power transfer (CPT) systems are widely used for very low power delivery due to a number of limitations and small coupling capacitance. Recent research has increased the coupling capacitance from the pF to the nF scale, enabling extension of CPT to kW power level applications. To reduce the cost and losses single-switch-single-diode topologies are investigated as efficient power electronics suitable for CPT at higher power levels while remaining cost effective. Four single active switch CPT topologies based on the canonical Cuk, SEPIC, Zeta, and buck-boost converters are investigated and verified using MATLAB R2014a/SIMULINK. Observed 1kW power transfer at a frequency of 200 kHz.

**KEYWORDS:** Capacitive power transfer (CPT), non-contact, SEPIC, Ćuk, Single switch converter, wireless power transfer.

## I. INTRODUCTION

Contactless power transfer technology provides a solution for power transfer where the source is normally fixed and the position of the load can be adjusted within suitable tolerances. There are two major ways to achieve contactless power transfer: inductive power transfer (IPT) and capacitive power transfer (CPT). Of these, the dominant means of transferring electrical energy across a gap/boundary without contact is inductive, e.g. magnetic flux coupling between isolated windings [1]. IPT techniques are ideally suited for applications where the power transfer distance is small to large, spanning a scale from millimeters to single meters. As shown in figure 1, IPT uses magnetic flux to couple between isolated coils connected to electric circuits. Conversely, CPT uses electric flux between conducting surfaces to couple between circuits. A minimum of two capacitors is required to transfer current across the air gap.

IPT has already been developed but CPT has only been developed for low power applications, CPT systems can transfer power through metal barriers, and they are not affected by metal surroundings. In comparison, means by which high-power losses can be mitigated are always a consideration when IPT systems are used in environments where metal is present. Fgure1 shows the block diagram of a typical CPT system with two pairs of metal plates for electric field coupling. A dc voltage source is converted to a high-frequency ac voltage which is then applied to two primary metal plates. When two secondary metal plates are placed in close proximity, an alternating electric field is formed between the plates enabling a displacement current to flow. By appropriate power conditioning, power can be transferred to the load without direct electrical contact and some freedom of movement between the primary and secondary plates is allowed. Here, the capacitive coupling comprises two equivalent capacitors formed by two pairs of primary and secondary (pickup) plates while a suitable dielectric material is assumed to exist between the coupling plates [2].

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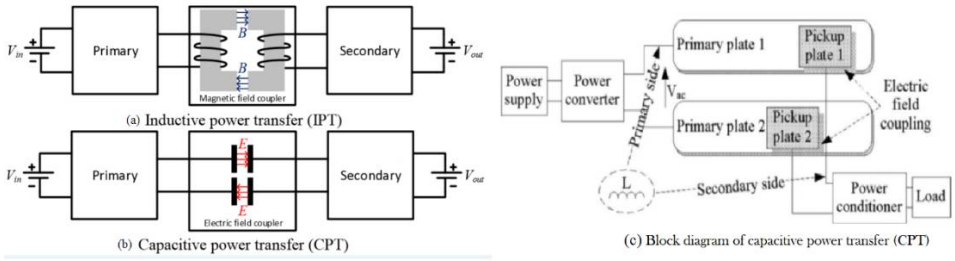


Figure 1: (a) Inductive power transfer (IPT) (b) Capacitive power transfer (CPT) (c) Block diagram of capacitive power transfer (CPT)

Recently the use of hydrodynamic supported capacitors has increased capacitive coupling by an order of magnitude. Coupling capacitances based on hydrodynamic fluid bearings demonstrate non-contact coupling at the 10nF scale. Previously coupling capacitances were limited to the 10s or 100s of pF ultimately limiting the power throughput of a CPT system. Other factors affecting power throughput include coupling capacitor current and operating frequency. Unsurprisingly, high frequency operation paired with higher-voltage-lower-current loads lends itself to higher power throughput. Consequently, the development of efficient kilowatt scale power electronics capable of switching hundreds of volts at frequencies in the range 200 kHz to 1 MHz is necessary.
Converters need to be cost effective, reliable, efficient and easy to control. CPT converters with a single active switch are taken as a means to meet these general criteria.

## II. SINGLE ACTIVE SWITCH CONVERTER TOPOLOGIES

### 2.1 Design Idea

There are several kinds of basic single active switch converters: Buck, Boost, Buck- boost, Cuk, SEPIC, Zeta (Inverse-SEPIC). For a CPT we need two capacitors. Among these topologies, Cuk, SEPIC, and Zeta have a capacitor that can split the circuit into two sides, i.e. primary and secondary. So these three topologies can be modified to accommodate CPT. Similarly, the inductor in a Buck-boost converter can be split and separated by two capacitors to realize a CPT circuit, as shown in figure 2.1. All four circuits are modified to a more general form: a primary circuit with a high-side inductor in series with a low-side switch; a secondary circuit with a high-side inductor in series with a low side diode; and two interface coupling capacitors that can be connected to the primary and the secondary circuits, as shown in figures 2.1.
To differentiate between the four configurations in a topological perspective, we define four new names: LSDL (Cuk), LSLD (SEPIC), SLDL (Zeta), SLLD (Buck- boost). The names are given by the sequence of the components (not including coupling capacitors) from left to right in the modified circuit of each topology in figure. This may be illustrated using the buck boost converter as an example. The standard and modified circuits in figure 2.1 both show that while observing from the left to the right side, the component sequence is switch (S),inductor (L), inductor (L), diode (D), thus the name is SLLD.

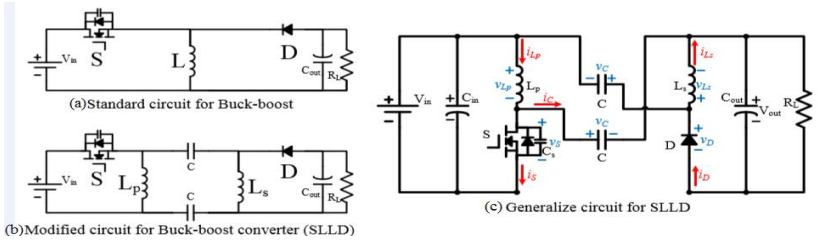


Figure 2: Buck Boost converter (SLLD)

The major difference between the four different converters is the average voltage on the power transfer capacitors, i.e. coupling capacitors C. If D is higher, the voltage stress on switch is higher. If D is lower, for the same power delivered, the AC voltage on the coupling capacitors will be higher. Therefore, all else being equal, the ratio was set to 50

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percentage i.e. the duty ratio is fixed to D = 0.5. The following observations can be made: 1) the switch and diodehave same voltage/current stress, 2) The coupling capacitor has DC bias for LSDL, LSLD, SLDL converters, and 3) there is no DC bias on SLLD converter coupling capacitors.
For CPT converters, the current transferred through the capacitors is limited by the frequency and the break down electric field strength between the capacitor plates, i.e. a given A/Hz. Therefore the DC bias voltage on the coupling capacitors should be minimized or eliminated to maximize the AC electric field margin that facilitates power transfer across the gap. Among the four converters SLLD is the best candidate for CPT applications.

**2.2 SLLD operational waveforms**

Figure 3.1 shows the SLLD converter circuit and its operational voltage and current waveforms in steady state. In the figure, current and voltage are plotted in solid red and blue lines respectively. In the waveform of C, the dashed red lines are the current of Lp and Ls, which are provided as references. As shown in the figure 3.1, the circuit is operating in discontinuous mode to realize zero voltage turn on for S. The seven stages of operation are detailed below and are illustrated in figure 3.2.

3.1.1 Stage 1: $[t_0 - t_1]$

$i_D$ is zero, so all the current through Ls is injected to the point between Lp and S. Meanwhile, $i_{Lp}$is negative and the magnitude is larger than $i_{Ls}$, such that there will be negative current going through S and the body diode is turned on first. Zero voltage turn on for S is achieved. During this time, $v_{Lp} = V_{in}$ thus charges Lp and increases $i_{Lp}$. $i_{Ls}$ changes little, so $i_S$also increases. Before $i_S$becomes positive, S should be turned on to allow positive current going through it.

3.1.2 Stage 2: $[t_1 - t_{2]}$

At time $t_1$, $i_S$ becomes positive. Since the S is turned on, $i_S$may still increase. At time $t_2$, S turns off.

3.1.3 Stage 3: $[t_2 - t_3]$

After S turns off at $t_2$, $i_{Lp}$and $i_{Ls}$ charge Cs together. $v_{Cs}$ increases relatively slowly, so zero voltage turn off is realized. When the drain to source voltage of S increases, $v_{Lp}$ decreases. Assuming C is large enough to keep $v_C$ from changing during this period, $v_{Ls}$ decreases when the $v_{Lp}$ decreases, thus$v_D$ decreases. At time $t_3$, $v_D$decreases to zero when D turns on.

3.1.4 Stage 4: $[t_3 - t_4]$

At time $t_3$, S is off, D is on. The current through D should increase to the sum of $i_{Lp}$ and $i_{Ls}$. $i_C$ increases to $i_{Lp}$.

3.1.5 Stage 5: $[t_4 - t_5]$

D is on, during this period. $v_{Lp}$ is fixed to $V_{out}$. $i_{Lp}$ decreases linearly, if $v_C$ changes little compared with $V_{out}$. However, in CPT applications, C is usually smaller in value. Thus during this time, Lp resonates with C.

3.1.6 Stage 6: $[t_5 - t_6]$

This stage is similar to stage 5, however $i_{Lp}$ and $i_C$ become negative.

3.1.7 Stage 7: $[t_6 - t_7 (t_0)]$

$i_C = i_{Ls}$ at time $t_6$, which means that all current through D is now transferred to C. D turns off without reverse recovercurrent. So zero voltage turn off on D is realized. During this time, $i_{Lp}$ is negative, most of the current is taken by C, which is $i_{Ls}$, and the rest of $i_{Lp}$ discharges through Cs. When $v_{Cs}$ is discharged to 0 at time $t_7$, body diode of S turns on

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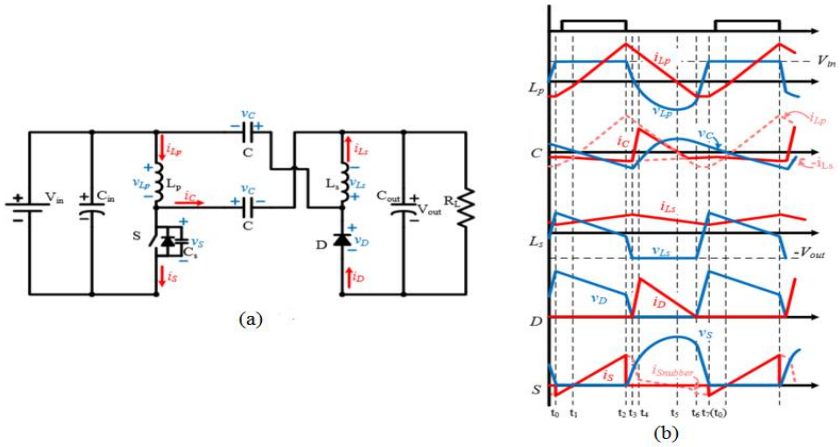


Figure 3: SLLD operation waveforms during a switching cycle

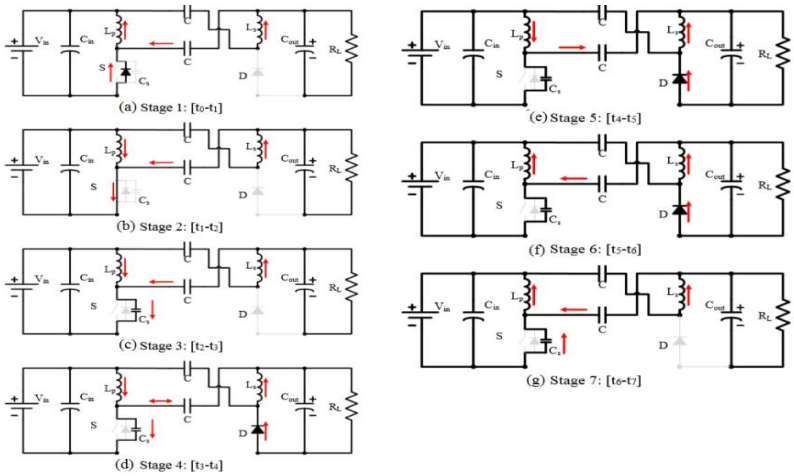


Figure 4: Modes of operation

### 2.3 Parameters Design

To achieve ZVS, the values of Lp, Cs, Ls are constrained. First, Lp should be small enough to offer enough negative current to discharge Cs before S turns on. At time t6, the magnitude of $i_{Lp}$ should be larger than $i_{Ls}$. On the other hand, Lp must be large enough to minimize current ripple. Therefore these two design points provide the bounds for Lp selection. Ls is used to provide constant current. It should be large enough to make sure the diode operates normally even during light load conditions. Alternatively, Ls should also be limited by its size and weight. C is limited by its surface area (size) and the breakdown electric field strength of the gap media. In this case, the calculation is an iterative procedure and the answer can be easily obtained by simulation. The parameters used to analyze the SIMULINK model are given in table 1.

Table 1: Circuit parameters

| Name | Symbol | Value | Name | Symbol | Name |
|---|---|---|---|---|---|
| Primary Inductor | $L_p$ | 43μH | Secondary Inductor | $L_s$ | 400μH |
| Input capacitor | $C_{in}$ | 20μF | Output capacitor | $C_{out}$ | 20μF |
| Coupling capacitor | $C$ | 24nF | Snubber capacitor | $C_s$ | 1nF |
| SiC MOSFET | S | 1200V /16A | SiC Diode | D | 1200V /30A |

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## III. SIMULATION RESULTS

### 3.1 SLLD Simulation Results

The converter was simulated using the software package MATLAB. Figure 5 shows the SIMULINK model. Figure 6 to 8 gives the voltage and current waveforms.

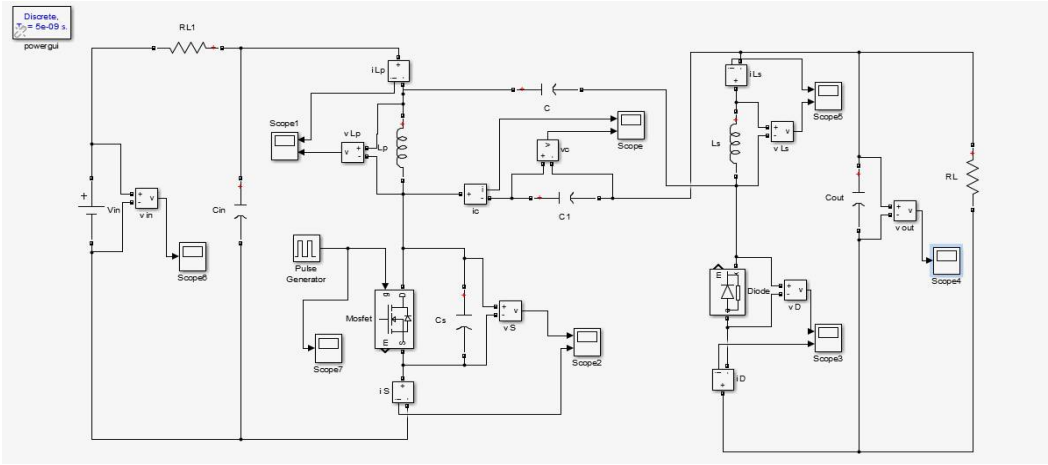


Figure 5: Simulink Model

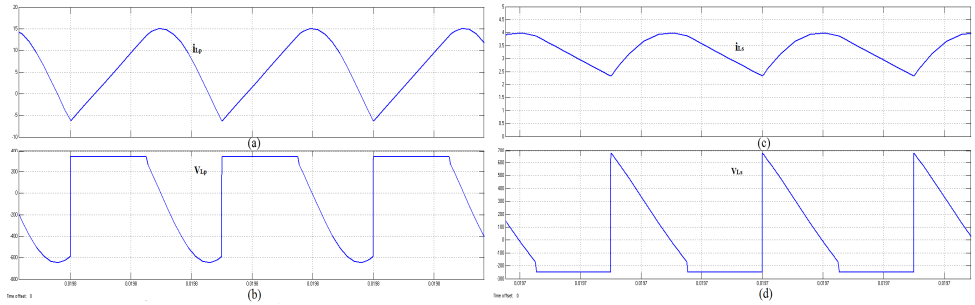


Figure 6: (a) current through Lp (b) voltage across Lp(c) Voltage across Ls (d) current through Ls

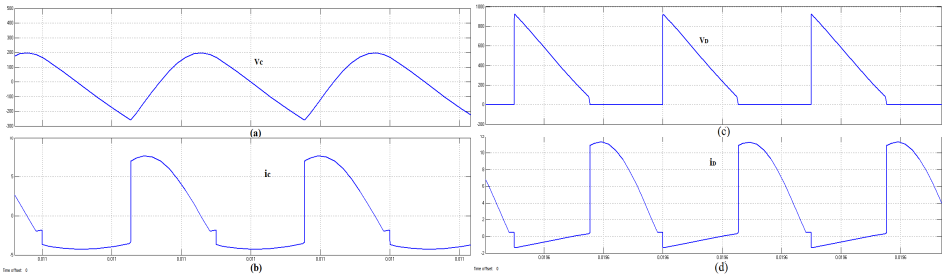


Figure 7: (a) voltage across coupling capacitor (b) current through coupling capacitor
(c) Voltage across diode (d) current through diode

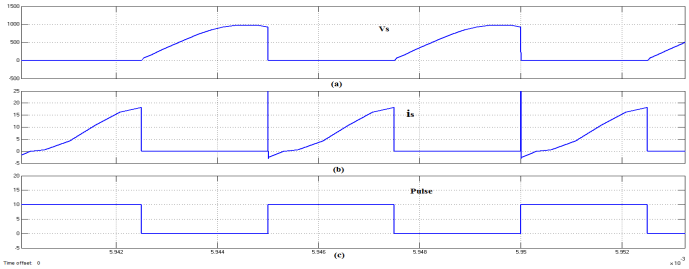


Figure 8: (a)Voltage across switch (b)Current through switch (c)Gate pulse for switch

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### 3.2 Comparison of the Four Circuit Topologies

The simulation results i.e., voltage across switch and current through switch for the four circuits are given in figure 9-11. From these we can deduce that DC biasing for coupling capacitor voltage is minimum for SLLD.

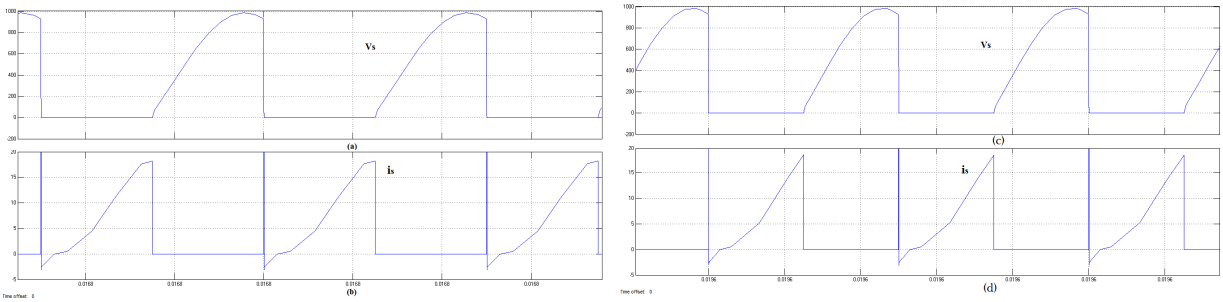


Figure 9: SLDL(a)voltage across switch (b)current through switch, LSLD (c) voltage across switch (d) current through switch

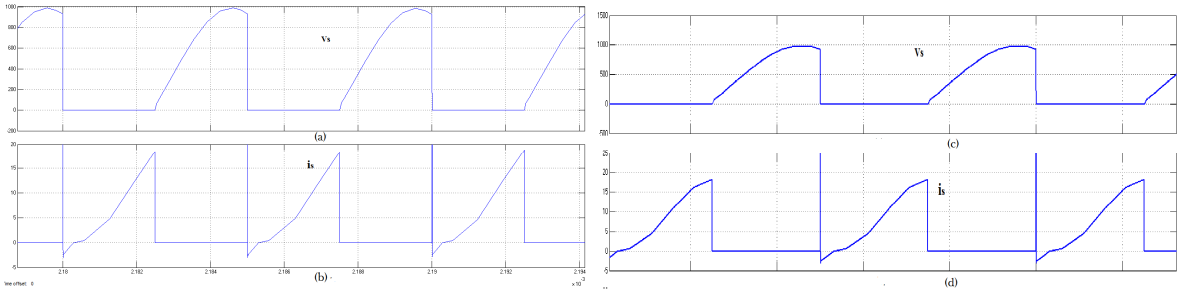


Figure 10: LSDL (a) voltage across switch (b) current through switch, SLLD (c) voltage across switch (d) current through switch

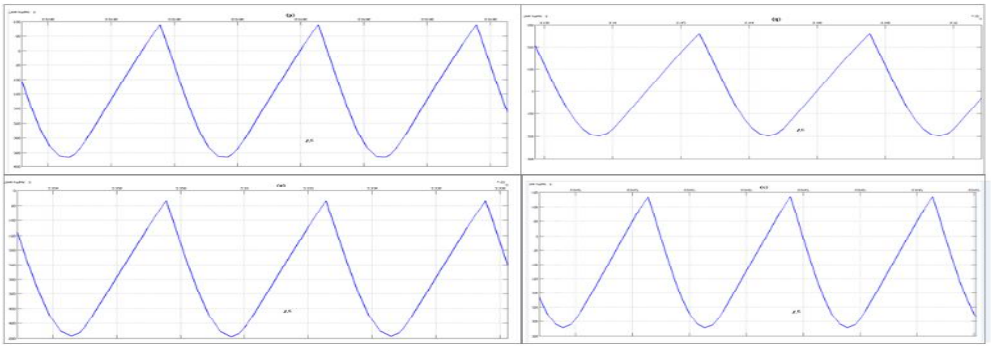

Figure 11: Coupling capacitor voltage (a)SLDL (b)LSLD (c)LSDL (d)SLLD

## IV. CONCLUSION

Capacitive power transfer is an effective alternative contactless power transfer solution. It has advantages including lower EMI, high efficiency and low cost, at high power (1kW). A series of single active switch converter topologies for CPT applications are considered .And mainly four topologies are compared and verified as CPT candidates, i.e. LSDL (Cuk), LSLD (SEPIC), SLDL (Zeta), and SLLD (Buck- boost).Out of these SLLD possesses the best properties for CPT applications because of its zero DC bias voltage on the coupling capacitors. Eliminating the DC bias on the coupling capacitors has the benefit of allowing greater AC current to pass through the coupling capacitors for a given voltage rating. Simulation is done using an input $V_{in}$ = 340V,switching frequency =200kHz and obtained power output

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nearly equal to 1KW. And the SLLD converter demonstrated the highest efficiency among the four converters, although all four possessed comparable efficiencies.

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