ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization *Vol. 5, Special Issue 6, July 2016*

4th National Conference on Design Innovations for 3Cs "Compute-Communicate-Control"

Organized by

Dept. of ECE, MVJ College of Engineering, Bangalore-560067, India

Divide-by-16/17 TSPC Dual Modulus Prescaler Implementation Using Verilog

Aruna .J[1], Manjula B.N[2]

Associate professor, Dept. of ECE, The Oxford College of Engineering, Bengaluru, Karnataka, India[1]

PG Student [VLSI Design and Embedded Systems], Dept. of ECE, The Oxford College of Engineering, Karnataka, India[2]

ABSTRACT: A high speed CMOS TSPC disengage by-16/17 twofold modulus prescaler is proposed. The double modulus prescaler assumes an essential part in stage lock circle, In PLL inside the chip utilizing double modulus prescaler. The pace of the prescaler is upgraded in two points. To begin with, by getting another pseudo crevice by-2/3 prescaler, the base working period is reasonably decreased essentially a NOR entryway's delay. Second, by changing the relationship of D-Flip-Tumbles, the base working period is further decreased impressively an inverter's deferment. Reenactment results exhibit that the best working repeat of the proposed circuit is improved by ~40% differentiated and standard circuit. The traditional circuit utilizing D flip-failure, two OR gates and one NAND gates so it seems two basic ways however proposed circuit utilizing just two AND entryways so the primary basic way is vanished and second basic ways can lessened .isolated by-2/3 prescaler has the pace advantage and is a great deal more power effective. Accordingly, isolated –by-2/3 prescaler is favored in 16/17 prescaler. This Proposed Framework Actualized using Verilog HDL and Recreated by Modelsim 6.4 c.

KEYWORDS: CMOS TSPC, Prescaler, D-Flip-Tumbles PLL**.**

I. INTRODUCTION

Double modulus recurrence prescaler assumes a vital part in stage bolted circle (PLL) plans. Albeit current-mode rationale and infuse locking prescaler can give working recurrence of hundreds/tens GHz with procedure of SoI CMOS or InP DHBTs et cetera, double modulus prescaler is generally used in a few GHz with standard CMOS process. It has the benefits of single clock stage, low power, little zone, and vast yield swing. Enhancing the rate is an essential configuration issue for prescaler. What's more, a few strategies have been created. In the transistor level, forward body biasing strategy can enhance the pace by diminishing the limit voltage of nMOS transistors. Be that as it may, it experiences high least working recurrence and also expanded cost and diminished vigor. In the entryway level, receiving amplified flip-flop can adequately enhance the working pace. Be that as it may, the present spillage is not kidding, along these lines the base working recurrence execution is restricted. In the RTL level, enhancing the pace of separation by-2/3 prescaler can likewise upgrade the pace of gap by-16/17 prescaler. Nonetheless, in these papers, a few configuration tenets of circuits are broken. It prompts contracting recurrence range in light of the fact that these prescaler are no more suitable for low recurrence operation. In enhancement combining 2/3 prescaler, 4/5 prescaler, 8/9 prescaler and 16/17 prescaler in a single circuit so it can reduce the area, power, delay.

II. CONVENTIONAL DIVIDE-BY-16/17 MULTI MODULUS PRESCALER

A. D-Flip-Flop

Favorable position of circuit is that AND/OR rationale entryways can be consumed into the principal phase of dff and the rationale profundity can be decreased. After AND/OR gate assimilation, the principal phase of the dff's will turn into a timed NANAD/NOR door.The rationale profundity can be diminished by around two inverters delay after retention. Usually, there are different structures to understand the required capacity by using rationale entryways and dffs. The streamlined outline is to utilize one and only AND/OR rationale doors before one dff. Then, the dffs retain all the rationale entryways into their first stage. After this, the rationale depth, power consumption, and format range will all be reduced .Above all, the outline tenets of circuits ought to be taken after. First, it will be better if the rationale

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization Vol. 5, Special Issue 6, July 2016

4th National Conference on Design Innovations for 3Cs "Compute-Communicate-Control"

Organized by

Dept. of ECE, MVJ College of Engineering, Bangalore-560067, India

ought to be implanted in the principal phase of dff, but not different stages. Second, it is not recommended that two way controls one hub. Otherwise, conflictions and glitches may happen.

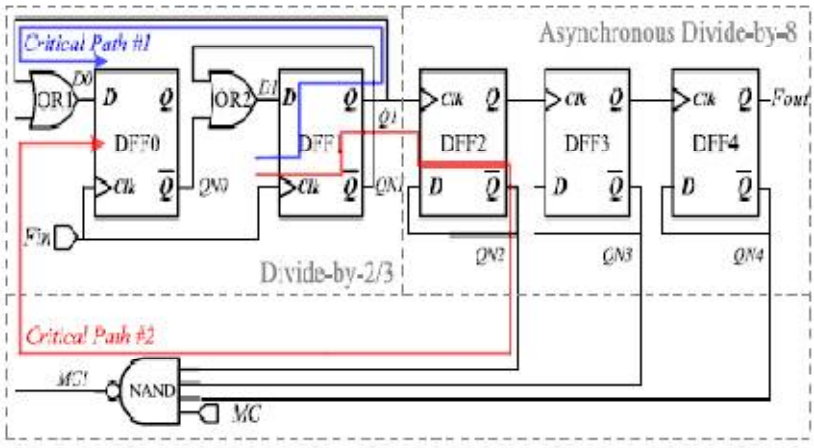


Fig.1. Schematic of conventional divide-16/17 prescaler

B. Conventional Divide-by-16/17 prescaler

The schematic of an ordinary separation by-16/17 prescaler in view of a partition by-2/3 prescaler. it has two basic ways: 1) Q1 way (basic way #1)comes through DFF1 and OR1 and 2)MC1 way (basic way #2) comes through DFF1, DFF2,NAND, and OR1. signal must pass path#1 inside of a time of Fin while it ought to pass way #2 inside of two times of Fin.In principle, it is hard to gauge which way chooses the base working period. The outcome fluctuates in various designs .it is a tradeoff between length of the two basic way in ordinary divider-by-16/17 prescaler. The advanced configuration is to make the length of basic path#1 roughly equivalent to half length of basic path#2. In traditional separation by-16/17 prescaler, two rationale gates (NAND as well as I) situate before DFF0. Obviously, it is not the improved configuration furthermore, there are two basic ways. Both basic ways ought to be enhanced to accomplish a rapid, which is an awesome test for creators.

III. PROPOSED DIVIDE-BY-16/17 PRESCALER

The schematic of the proposed partition by-16/17 prescaler. it comprises of a pseudo gap by-2/3 prescaler, a non concurrent isolate by-8 divider, and a four-data and door. contrasted and the routine circuit, there are two fundamental changes in the proposed isolate by-16/17 prescaler. initial, another pseudo separation by-2/3 prescaler is embraced rather than routine partition by-2/3 prescaler. The pseudo gap by-2/3 prescaler can precisely achieve a solitary, yet not consistent gap by-3 operation.Also, it is sufficient for separation by-16/17 prescaler on the grounds that it just needs short of what one gap by-3 operation in a cycle. by adopting the pseudo gap by-2/3 prescaler, an OR door is spared and there leaves one and only AND entryway before DFF0.as an outcome, the basic way #1 in traditional circuit is vanished and the length of basic way #2 is diminished.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization Vol. 5, Special Issue 6, July 2016

4th National Conference on Design Innovations for 3Cs "Compute-Communicate-Control"

Organized by

Dept. of ECE, MVJ College of Engineering, Bangalore-560067, India

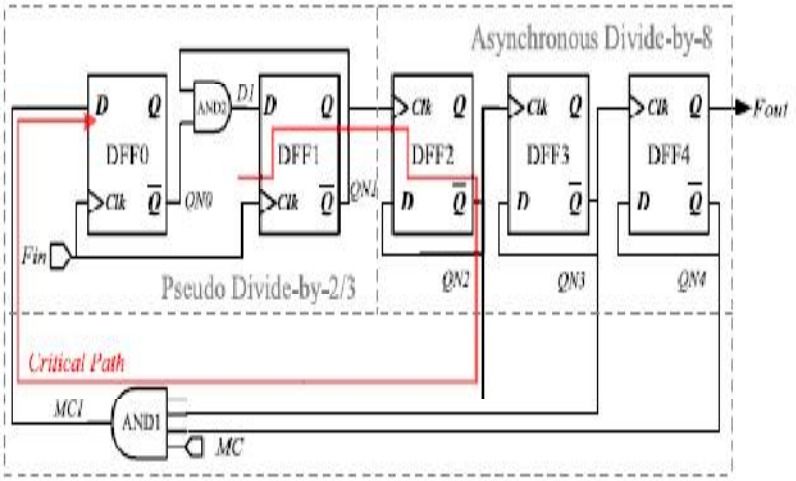


Fig.2. Schematic of proposed divide-by-16/17 prescaler

Second, QN1 and QN2 hub (rather than Q1 and Q2 hub in customary circuit) of DFF1, DFF2, and DFF3, is associated with the info CLK hub of DFF2, DFF3, and DFF4, separately. the propagation postponement of DFF1, DFF2, and DFF3 will all reduction.In this manner, the length of basic way will be further decreased. the operation method of proposed circuit is as follows. When Mc=1, Mc1 changes its worth as indicated by (QN2, QN3, QN4). The pseudo divide-by-2/3 prescaler controlled by MC1 accomplishes seven times of divide-by-2 operations and one of divide-by-3 operation in a cycle. The whole circuit operates in divide-by-17 mode. When Mc=0, MC1 keeps low and the pseudo divide-by-2/3 prescaler keeps on divide-by-2 operation. The whole circuit works in divide-by-16 mode.As well as the conventional circuit, the maximum working frequency of proposed prescaler is decided by its divide-by-17 operation mode. In addition, the key operation in divide-by-17 mode is the divide-by-3 operation of pseudo divide-by-2/3 prescaler. By adopting a pseudo divide-by-2/3 prescaler, the minimum working period is reduced by half a NOR gate's delay. By changing the connection of DFF, the minimum working period is further reduced by half an inverter's delay. The speed improvement of the proposed circuit can be estimated as follow. The simulated maximum working frequency of conventional 16/17 dual modulus prescaler is ~4.5 GHz. It corresponds to a working period of 222 ps. Simulation results also show that an inverter's delay is ~45ps and a NOR gate's delay is ~80ps. Then the minimum working period of proposed circuit will be reduced to 159.5 ps the maximum working frequency of the proposed circuit is ~6.3 GHz, which is improved by ~40% when compared with the conventional circuit.

IV. MULTI MODULUS PRESCALER

The enhancement of multi modulus prescaler is the combination of the all 2/3 prescaler, 4/5 prescaler, 8/9 prescaler, 16/17 prescaler.

The operation of multi modulus prescaler is the combination of 2/3 prescaler, 4/5 prescaler, 8/9 prescaler, 16/17 prescaler. Using the 4*1 multiplexer that is 4 inputs and one output, Fin is the CLK input and RST primary input Mc control input. the multi modulus prescaler performs in a single circuit 4 operations and it divide the prescaler according to the Sel mode.

When Sel=00 the 2/3 prescaler divides when MC=0 the operation mode is divide-by-16, when MC=1 the operation mode is divide-by-17.

When Sel=01 4/5 prescaler divides when MC=0 the operation mode is divide-by-32, when MC=1 the operation mode is divide-by-33.

When Sel=10 8/9 prescaler divides when MC=0 the operation mode is divide-by-64, when MC=1 the operation mode is divide-by-65.

When Sel=11 16/17 prescaler divides when MC=0 the operation mode is divide-by-128, when MC=1 the operation mode is divide-by-129.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

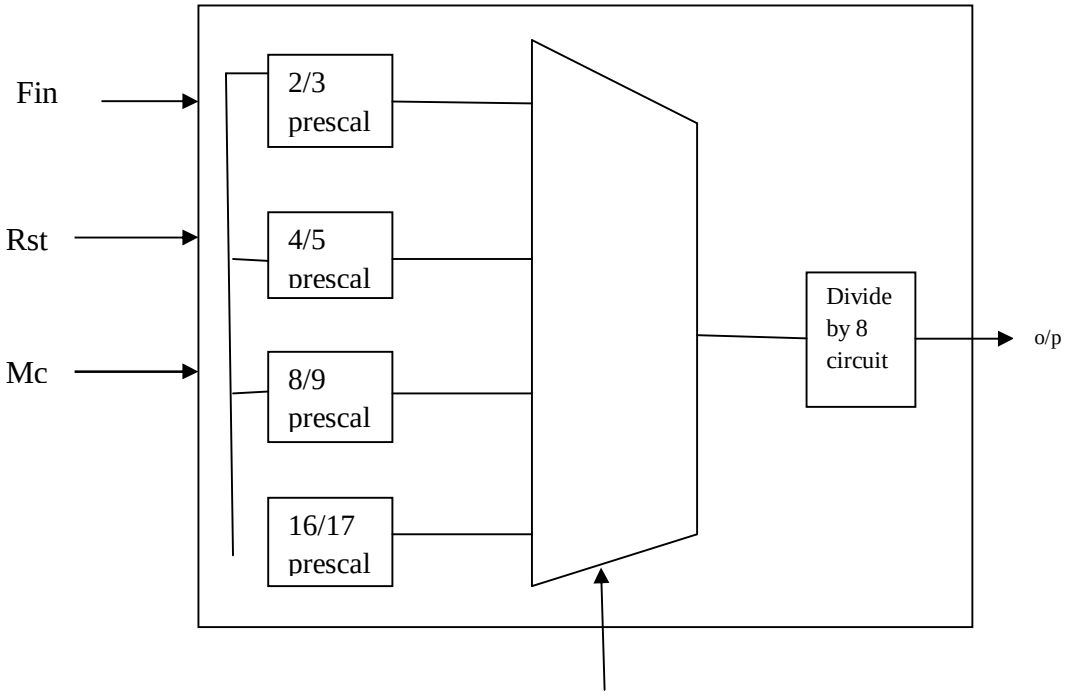
International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization *Vol. 5, Special Issue 6, July 2016*

4th National Conference on Design Innovations for 3Cs "Compute-Communicate-Control"

Organized by

Dept. of ECE, MVJ College of Engineering, Bangalore-560067, India



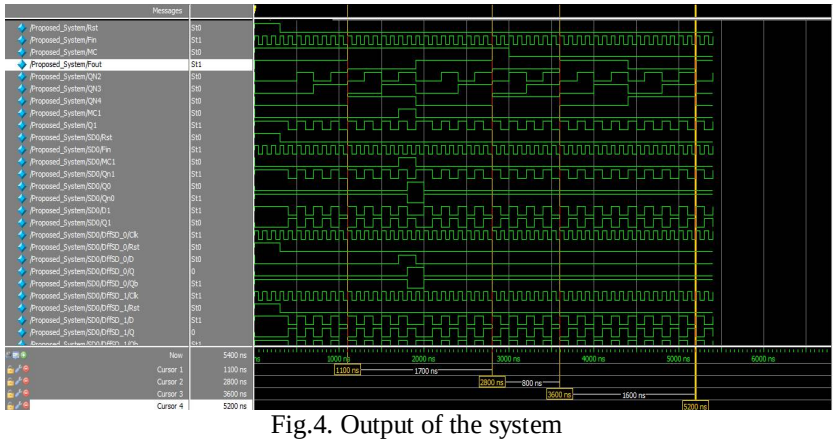


Fig.4. Output of the system

The proposed system of the 2/3 prescaler divide-by-16 when MC=0, operation mode 3 it divide-by-17 when MC=0.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization *Vol. 5, Special Issue 6, July 2016*

4th National Conference on Design Innovations for 3Cs "Compute-Communicate-Control"

Organized by

Dept. of ECE, MVJ College of Engineering, Bangalore-560067, India

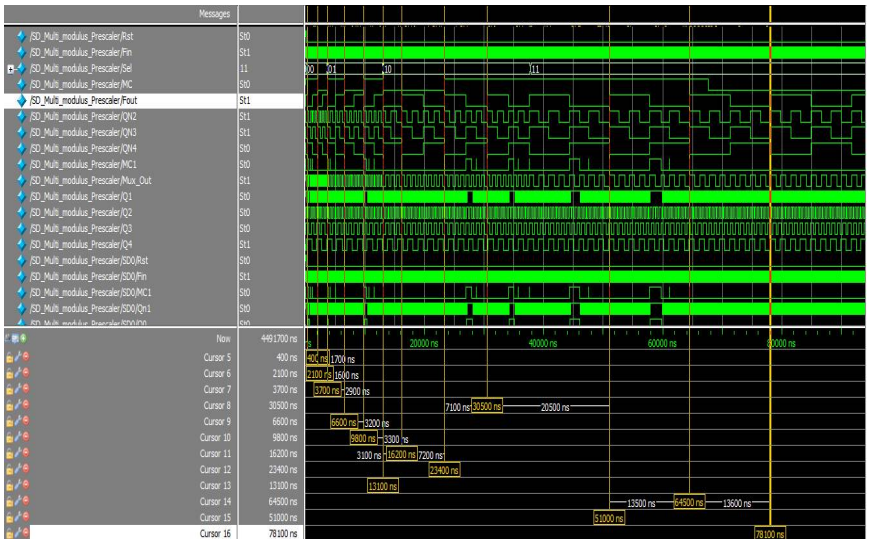


Fig.5. Output of the system

The multi modulus prescaler combination of 2/3 prescaler, 4/5 prescaler, 8/9 prescaler, 16/17 prescaler.

VI. CONCLUSION

This brief presents a novel high-speed divide-by-16/17 dual modulus prescaler. The speed of the proposed circuit is improved in two aspects. First, by adopting a new pseudo divide-by-2/3 prescaler, pseudo divide-by-4/5 prescaler, the minimum working period is effectively reduced by half a NOR gate's delay. Second, by changing the connection of DFFs, the minimum working period is further reduced by half an inverter's delay. What's more, the minimum working frequency performance is not deteriorated at the same time. Finally did 32/33 Prescaler with the DFF Flip-flop.

REFERENCES

1. T. Shibasaki, H. Tamura, K. Kanda, H. Yammaguchi, J. Ogawa, and T. Kuroda, "A 20-GHz injection-locked LC divider with a 25% locking range," in Int. Symp.
2. D. D. Kim, J. Kim, and C. Cho, "A 94GHz locking hysteresis-assited and tunable CML static divider in 65nm SOI CMOS,"
3. D. A. Hitko, T. Hussain, D. S. Matthews, R. D. Rajavel, I. Milosavljevic, and M. Sokolich, "State of the art low power (42 mW per flipflop) 50 GHz+ CML static divider implemented in scaled 0.2m.
4. B. Chang, J. Park, and W. Kim, "A 1.2 GHz CMOS dual-modulus prescaler using new dynamic D-type flip-flops.
5. C.-Y. Yang, G.-K. Dehng, J.-M. Hsu, and S.-I. Liu, "New dynamic flip-flops for high-speed dual-modulus prescaler.
6. S. Kim and H. Shin, "An E-TSPC divide-by-2 circuit with forward body biasing in 0.25µm CMOS," IEEE Microw.
7. H. Shin, "A 1-V TSPC dual modulus prescaler