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Development of a Four-Quadrant Analog Multiplier using a Single-Quadrant Analog Multiplier and Convertor Circuitry

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ABSTRACT*:* An analog multiplier is a device that performs the analog multiplication of at least two analog signals fed to its input side. Considering the analog signal to be a voltage signal, single-quadrant analog multipliers pose the difficulty of performing the analog multiplication of signals possessing the same sign only. In order to incorporate the multiplication of signals varying with either positive or negative polarities, a four-quadrant analog multiplier is used. The Gilbert Cell [1] approach is, by far, the most popular technique to achieve four-quadrant analog multiplication. However, a limited bandwidth consideration prohibits its use in high speed communication networks.This paper presents a novel approach to convert a single-quadrant analog multiplier into a four-quadrant analog multiplier using basic analog convertor circuitry with an extended bandwidth.

KEYWORDS: Analog Multiplier, Precision Rectifier, Sign Detection, Sign Conversion, Exclusive-OR logic, Zero Crossing Detector, Unity Gain Inverting Amplifier.

I.INTRODUCTION

Analog multipliers form the fundamental block in most analog and digital communication systems, nonlinear signal processing, artificial neural networks etc. Apart from the multiplication operation, they also play a huge role in the analog computing domain, where at least two analog signals are subjected to mathematical operations such as division, square, square root etc. Other complex operations such as Root Mean Square (RMS) for true RMS convertors [1], vector sum modules, etc. are also carried out fundamentally by the analog multiplier.There are many types of methods proposed to perform analog multiplication such as the "quarter-square" technique [2], log-antilog amplifier technique, transconductance multiplier topology, etc. From the above mentioned topologies, the transconductance technique serves as the most widely used design till date. This technique is based on the popular translinear principle and Gilbert gain cell approach coined by Barrie Gilbert. The log-antilog amplifier technique is limited to single-quadrant multiplication, hence called a single-quadrant multiplier.The technique proposed in this paper uses a single-quadrant multiplier, such as the log-antilog amplifier, to perform four-quadrant analog multiplication using a novel sign detection and sign conversion circuitry.

II.BLOCK DIAGRAM REPRESENTATION

Figure 1 comprises of the general block diagram of the complete system. The input signals v_x and v_y are the two analog voltage signals to be multiplied. The two precision rectifier blocks convert v_x and v_y into positively varying signals respectively. The precision rectifiers are used to prevent any diode loss that may cause errors in the multiplication process. The resultant waveforms are fed independently to the positive quadrant analog multiplier block(for example, a log-antilog amplifier) as shown in Figure 1. This block is capable ofsuccessfully performing the analog multiplication of the two positively varying signals.The sign detector block performs the process of sign detection for v_x and v_y independently. The sign detector's output provides a control signal, *ctrl*, to the sign convertor block. The sign convertor block successfully changes the sign of the result after the multiplication process to providev_o.The output v_o is the four-quadrant multiplication result of the input signals v_x and v_y.

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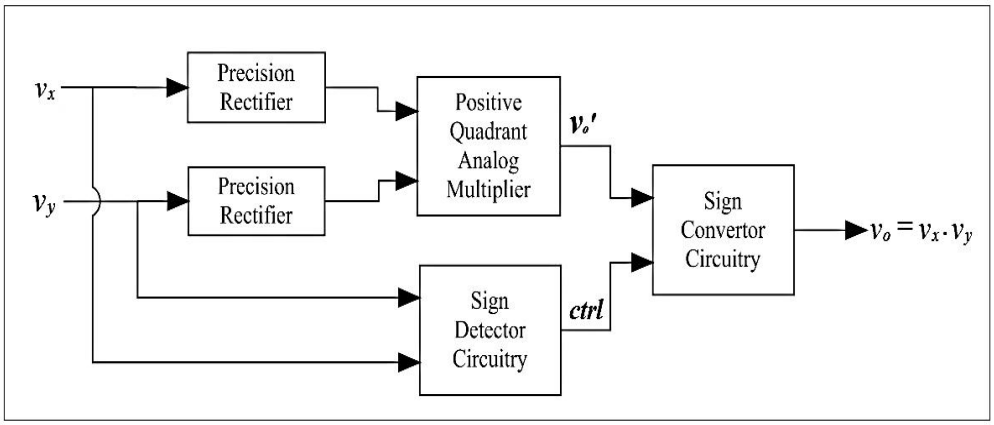

Fig.1:General Block Diagram of the proposed Four-Quadrant Analog Multiplier

III.SIGN DETECTOR CIRCUITRY BLOCK

Figure 2 depicts the sign detector circuitry block, which consists of two zero crossing detectors (ZCDs). The ZCDs are used to determine the sign change of the varying analog signals, v_x andv_y, respectively. If operational amplifier based ZCDs are used, then the outputs of the ZCDs are the saturated supply voltages applied to the operational amplifier. Depending on the polarities of v_x andv_y, the ZCD provides the sign detection as a positive or negative supply voltage transition. As in Figure 2, the outputs of the respective ZCDs are the inputs for the Complementary Metal Oxide Semiconductor (CMOS) Exclusive-OR (EXOR) gate. The CMOS EXOR gate performs the function of comparing the signs of both v_x andv_y, to provide the output signal *ctrl*.As seen in Figure 1, *ctrl* from the sign detector circuitry along with the output of the positive quadrant analog multiplier block, v_o'serve as inputs to the sign convertor circuitry.

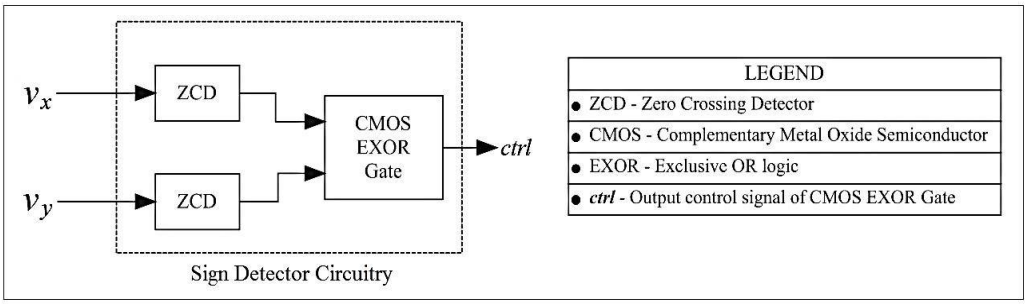

Figure 2: Block Diagram of the Sign Detector Circuitry

IV.SIGN CONVERTORCIRCUITRY BLOCK

The sign convertor circuitry block, as seen in Figure 3, performs the sign conversion of the result from the positive quadrant analog multiplier block based on the control signal, *ctrl* received from the sign detection circuitry block. The *ctrl*signal is used as a control signal for the analog demultiplexer and multiplexer blocks. As seen in Figure 3, the *ctrl* signal decides whether to allow the multiplied signal, v_o' for the inversion process or if the signal is to be passed without inversion. The analog demultiplexer, based on the *ctrl*control signal passes the signal for inversion through the unity gain inverting amplifier (UGIA) block. It is also observed that the same control signal, *ctrl*also selects between the two linesthe analog multiplexer. Finally, the analog multiplexer provides the desired output,v_o, which is the four-quadrant analog multiplication of the signals v_x and v_y.

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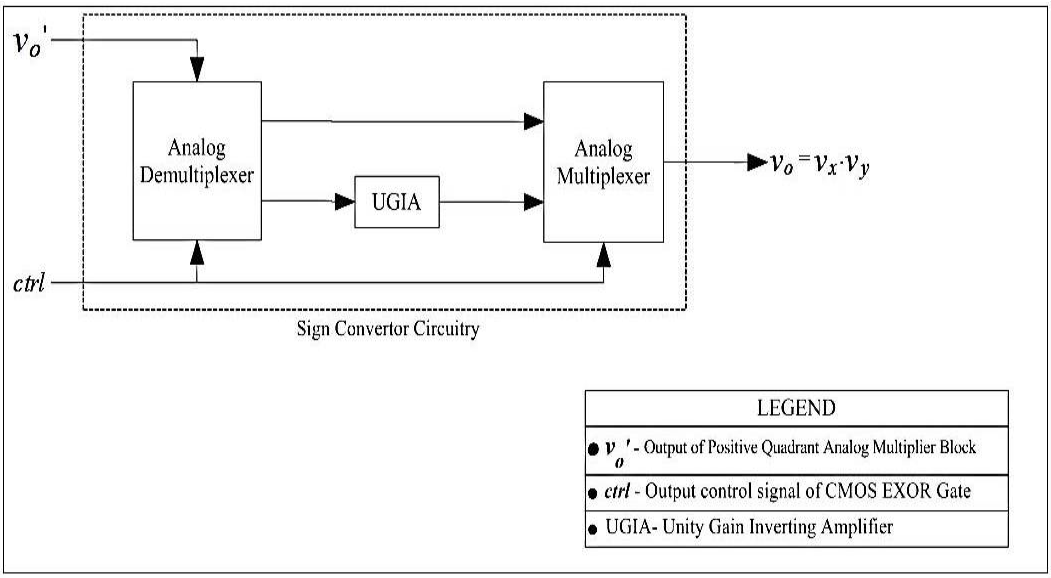

Fig. 3: Block Diagram of the Sign Convertor Circuitry

V.CONCLUSIONS

The methodology presented in this paper assumes that a precision single quadrant analog multiplier is available. For precise four-quadrant analog multiplication, the various propagationdelays in the positive quadrant analog multiplier have to be the same as that of the sign convertor and sign detector circuitries. That is, the delays of the above mentioned circuitries must be matched through design. The use of appropriate CMOS technology, ensures that the sign detection and conversion process occur at very high rates, depending on the frequency of the input analog signals. Thus, we can achieve a higher bandwidth by choosing faster switching transistors for the above circuitries.The above approach encapsulates the simple use of basic analog sub-circuitries working as a system to solve a larger problem of four-quadrant analog multiplication using the limited capabilities of a single quadrant analog multiplier.Lastly, the circuit level simulation of the design proposed is presently under experimentation.

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