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Development of Risk Prediction Tool for Signal Integrity

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ABSTRACT: In most of the new generation computing platforms, the operating frequencies of many of the interfaces are going into multi gigahertz ranges. DDR SDRAM based memory channel is the good example. Being a parallel interface it takes more real estate, includes different vendor's memory module and need much more careful designing.This makes electrical simulations/analysis critical in those design. So, traditionally an electrical model of the channel is developed and simulated for obtaining timing and voltage margins. However, for a given topology, this simulation coverage will be optimized to one set of design variables only. Furthermore it is a slow process, needs lot of computing resource and may not cover all the possible combinations of the variables in the design space. To reduce the overhead of the in-depth analysis for each design case, the idea of the risk prediction has been introduced. It gives out quick margin trends for the channel and risk associated for those margins, as it statistically predicts the channel characteristic of the larger set of topologies and routing layouts by applying ANN algorithm on the existing dat*a.*

KEYWORDS: Artificial Neural Network (ANN), Double data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM).

I.INTRODUCTION

The trends in the Semiconductor industry constantly evolve to satisfy the market demands. Unlike in the past where focus was on producing a single well designed product, the heavy competition has made it necessary to produce several variations of the base design to better fit multiple market segments simultaneously. The PCB Stack-up count, the area used to layout the traces and the bill of material (BOM) of a board has to be reduced among other things to reduce cost and produce very compact design. Assessing all these parameters to find out an acceptable trade-off between noise for a given circuit configuration is an important part of the Signal Integrity Analysis [1]. In traditional approach an electrical model of each circuit segment is built up and simulated over the expected variations to define the boundaries within which the board must be designed. A comprehensive design guide is made for each topology and released to the customer. The biggest short coming of this approach is that there are times when a circuit designer is unable to meet the constraints set by design guide. In order to find a work around, a practical trade off must be made between the signal quality and cost/area. To do this, one would need to know the impacts of different parameters and also determine which of those has the greatest effect on the signal integrity (SI).

This requires tweaking the models and extensive simulations for each new case. This incurs additional time [2], for the designs to complete and moreover the end customer, a board designer, may find it difficult to interpret the simulation results when compared to a dedicated SI team.

In the previous work [4] use of artificial neural network for the efficient statistical analysis and nonlinear modeling of high-speed systems. TheANN approach overcomes the limitation of traditional methods byconsiderably speeding up the analysis necessary to study the effectsof parameter variations. The ANN is trained using a methodical set ofdata that were generated using simulation results based on orthogonalarrays. It has demonstrated that the ANN can generalize and closelycapture the nonlinear mapping between channel parameters and performances. It has not mentionedto find the risk associated for the obtained margin.

The goal of the proposed method is to supplant the current SI analysis with the means of quick assessment without the need for additional extensive simulations .This idea is designed for a particular interface based on a predefined solution

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space but also can show results for new values of the design variable that were not tested during the design [3] [4]. The risk level is assigned to the obtained margin values.

II.METHODOLOGY

The various steps need to be performed for the prediction of the margin values, which consist of getting the input variables, create the electric model for those variable set and simulate those models. Perform the Signal integrity analysis for getting the margin values. For the obtained margins fit the model and predict the margin values. Correlate the predicted margin values with the simulated values. In Fig.1 the block diagram of the tool has been shown

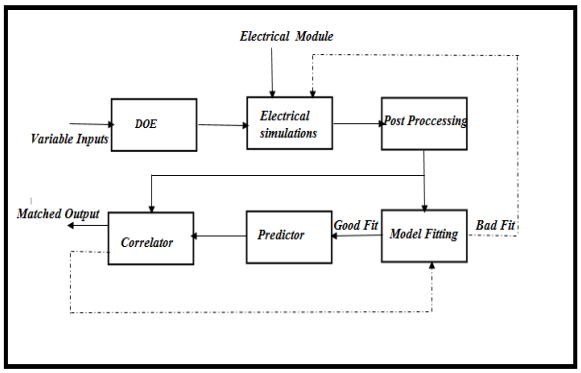

Fig.1. Block diagram of the risk prediction tool

A. DoE (Design of Experiments) Table

The DoE table for a given topology-routing combination consists of a list of combinations of all the input /Design Variables used in our model. Each of these simulations can be simulated separately in the SPICE deck, PDA (Peak Distortion Analysis) is performed and the results are obtained. The number of DOE table entries is relatively small but are selected in such a manner as to be able to be expanded into a much larger set of few million cases, this is necessary because simulations on each case takes time.

Each combinations of parameters from DoE table are taken and simulated for a variety of input patterns. The worst case bit pattern is found out using Peak Distortion Analysis and an eye diagram is developed. Using an eye mask, the various margins (Vm, Tm, Undershoot etc.) are measured. This process has to be repeated for every entry in the DoE table.

In the post-processing stage, we extract these results (Vm, Tm) and provide them to the statistical tool to create a statistical model in order to predict the margin values. The predicted result is compared to the acceptable limits as specified by the interface specifications with sufficient margins.

B. Prediction

There are various statistical modelling algorithm which are used in variety of applications. Here, Artificial Neural Network is used to 'learn' the interaction between the design variable and the output parameters and then make prediction for the combinations that were not simulated.

A very basic ANN model which uses nonlinear activation functions and multiple layers independent variables to predict the dependent variables can be visualized as shown in the Fig.2

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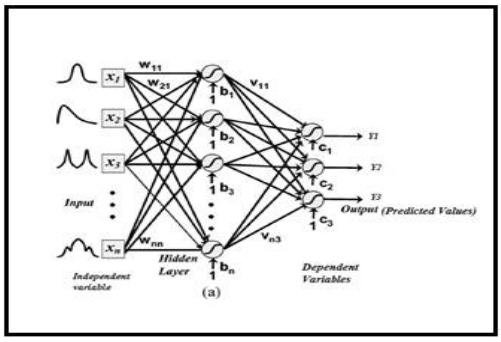

Fig.2.Simplified ANN model

C. *Training the model*

The manner in which the ANN model is developed is quite different from the others in that it's done through an automatic trial and error method. This process is called 'training' the model where the model is iteratively improved by predicting the output for one set of inputs and then comparing it with the true output. The prediction error is compensated for in each iteration through the weights till it gets minimized. This process is also referred to as supervised learning depicted in Fig.3

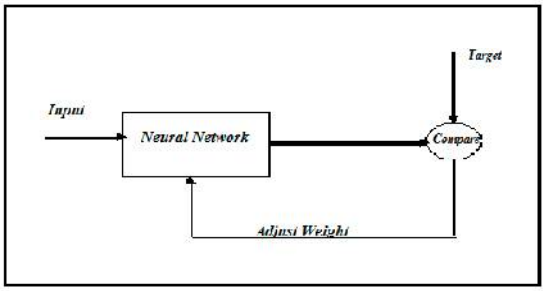

Fig.3.ANN Training Network

So, typically the DOE table is split into threesets,described asbelow:

- Training: These are used to train the ANN
- Validation:Used to check for over fit criteria
- Test: Used to evaluate the quality of the model

D. *Space Filling*

The model has to be trained before it can be used for the riskanalysis.The ANN requires several thousand points for thispurpose and therefore a space filling algorithm is used. In this,the large number of points equally distributed between upperand the lower bounds are used.

III.RISK PREDICTION

For margin values obtained from the above methodology the risk value is calculated and the risk levels are assigned to give an idea of how likely the circuit would behave for various combination of the parameter and what will be the risk level for the selected combination.

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IV.RESULTS

A. *Specifying the quality of prediction*

The Root Mean Suare Error (RMSE) factor is used to quantify the quality of the tool prediction and the confidence at which its results can be used for board design.In this specific case it is defined as the sample standard deviation of the differences between actual and predicted value.

$$RMSE = \sqrt{\frac{\sum_{i=1}^{n}(p_i - a_i)^2}{n}}$$

Where p_i and a_i are the predicted and actual values and 'n' is the total number of points used to compute the RMSE.

B. *Specifying the Risk level*

For the obtained margin values risk will be calculated .

Example:

Here is the example of the DDR3 interface.

The Risk levels are divided into following Risk levels.

Risk Value	***Risk Level***
0.00-0.33	High Risk
0.33-0.66	Medium Risk
0.66-1.00	Low Risk

V. CONCLUSION

The major benefits of this paper are that the end user,a board designer, would not need to constantly work with the SI team while making critical changes to his design and user can vary the parameters values and check the corresponding risk level for the selected combination.The other benefit is in terms of the time it takes to obtain the results. As the tool works from statistical models, actual circuit simulations are not needed for the prediction which reduces the Time to Market (TTM). This also improves the design cycle time as well as lower Non-Recurring Engineering costs.

Through this paper it has been verified that the approach taken is accurate enough for design use and also that the resulting tool is intuitive enough for someone who isn't well versed with SI theory.

VI.ACKNOWLEGMENT

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