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Design of a Two Stage CMOS Operational Amplifier using 180nm and 90nm Technology

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ABSTRACT: Op-amps are the most versatile and widely used component of electronic devices. Here in this work, a two stage CMOS Op-amp has been designed using both 180nm and 90nm technologies. The two stage CMOS op-amp has been designed which dissipates power as low as 0.19mW along with a propagation delay as low as 5.39ns. The circuit has a unity gain bandwidth of9.78MHz with a phase margin of 93.69°in 180nm technology while a unity gain bandwidth of 5.05MHz and phase margin of 82.89° in 90nm technology. Comparative analysis for both the 90nm and 180nm technologies has been done. Effect of scaling has also been discussed which results in gain bandwidth almost two times that before scaling. Layout has been designed for two stage CMOS op-amp in 180nm and 90nm technologies. All the work has been done using tanner EDA v14.1 tools. The schematic has been made using S-edit while the netlist was being created using T-spice and results were viewed using W-edit tool. The layout has been designed using L-edit tool.

KEYWORDS: CMOS two stage Op-amp , layout ,unity gain bandwidth , phase margin , low power , low propagation delay

I.INTRODUCTION

The operational amplifier(op-amp) is a fundamental and an integrated building block in analog circuit design. Op-amp in general is a 3-terminal device with an inverting input(denoted by "-" sign), a non inverting input(denoted by "+"sign) and an output terminal. The basic principle used in an Op-amp is to have high forward dc gain to implement the negative feedback so that when negative feedback is applied ,the closed loop transfer function of op-amp is independent of its gain[12-14]. As the transistor channel length and supply voltages are shrinking, the CMOS is becoming a great success among all because it can be easily scaled down to dimensions like micrometer and nanometer. Due to scaling down of channel length more number of transistors can be integrated on a single chip which leads to the need of high operating frequency which can be implemented with the help of CMOS op-amp.

Op-amps are linear devices having applications in various scientific devices and is extensively used to perform mathematical operations like addition, subtraction, integration and so on.[15] Op-amps are also used in signal conditioning, in many biomedical applications to design a low frequency active pass filter .Op-amps with two or more stages are widely used to achieve higher gain. One of the most popular Op-amps is a two stage Op-amp which is the aim of this work[4]-[8].

This paper represents the work done in a proper sequence. Part I describes the introduction. Part II describes the two stage CMOS op-amp with its working. It also describes the design steps for a two stage CMOS op-amp to find the aspect ratios of the transistors in an op-amp along with the specifications to be taken ,for instance, threshold voltages of PMOS and NMOS, slew rate, etc. Part III discusses the simulation part where a comparison has been shown between 180nm and 90nm technologies for parameters such as open loop gain, unity gain bandwidth, delay etc. Also the impact of scaling has been shown. Further in part IV, layout design for a two stage CMOS op-amp has been given for 180nm and 90nm technol0gies with a brief discussion about the area consumed and how the parameter values changed upon layout design. Finally part V concludes the work done.

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II. TWO STAGE CMOS OP-AMP

A two stage CMOS Op-amp consists of three stages. The first stage is a differential amplifier followed by a gain stage which can be a common source stage and finally followed by an output buffer. The output buffer is used only if the Op-amp is to drive large capacitive or/and resistive loads.
Op-amps can have different topologies,a two stage CMOS op-amp is one such topology. The two stage CMOS Op-amp topology is used where high input impedance and low ouput impedance is required[3]. Figure 1 below shows the basic configuration of a two stage CMOS Op-amp. Here transistors M1,M2,M3,M4 form the first stage which is the differential gain stage and transistors M6 and M7 form the second stage which is the gain stage. In the first stage, transistor M5 provides the biasing to entire circuit,transistors M1 and M2 form the differential input pair actively loaded by a current mirror pair formed by transistors M3 and M4. In the second stage, transistor M6 is a common source amplifier actively loaded by transistor M7.

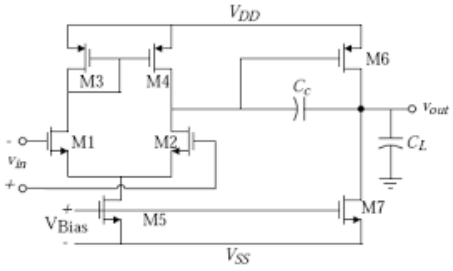

Figure 1: Two stage CMOS topology[12]

Here in the Figure 1, compensation capacitor C_c has been connected across the high gain stage which results in pole splitting phenomenon to improve the closed loop stability[1]. This topology has been simulated in the next section in both 180nm and 90nm technologies to find open loop gain, unity gain bandwidth ,phase margin, delay and power consumed by the circuit.

For the designing of a two stage CMOS Op-amp various design steps needs to be considered. These design steps helps to achieve the proper sizing of the transistors used in an op-amp.
It has been assumed that all the transistors are in saturation state. Then we choose the device length to be used throughout the circuit which keeps channel length modulation parameter constant. Below are the steps for designing a two stage CMOS op-amp[12].
1.For a desired phase margin of 60 degree, choose the minimum value of C_c by assuming z≥10GB,using equation II.1,

$$Cc > 0.22Cl \quad \text{II.1}$$

2. Determine the tail current I_5 using equation II.2,

$$I_5=SR.\ C_c \quad \text{II.2}$$

3. Design for S_3 from maximum input voltage specifications, given by equation II.3,

$$S_3=S_4=\frac{2I3}{k3'[VDD-Vin(max)-v(to3)(max)+vt1(min)]2}\geq 1 \quad \text{II.3}$$

4.Verify that the pole and zero due to Cgs_3 and Cgs_4 will not dominate by assuming p_3>10GB,

$$gm_3/2C_{gs3}>10GB \quad \text{II.4}$$

5.Design for S_1 and S_2 so as to achieve desired GB

$$gm_1=GB.\ C_c \text{which implies}$$
$$S_1=S_2=(g_{m2})^2/(k_2'I_5)$$

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II.5

6. Design for S_5 by first calculating $V_{ds5}(sat)$ as given by equation II.6,

$$V_{ds5}(sat)=V_{in}(min)-V_{ss}-\sqrt{I5/B1}-V_{t1}(max)\geq 100mV$$
$$S_5=2I_5/(k_5'[V_{ds5}(sat)]^2)$$

I.6

7.Design for S_6 by letting $p_2\geq 2.2GB$

$$gm_6=2g_{m2}(C_l/C_c) \text{which gives}$$
$$S_6=S_4(g_{m6}/g_{m4})$$

II.7

8.Now we solve for I_6 as given by equation II.6,

$$I_6=g_{m6}^2/2k_6'S_6$$

II.8

9.Design for S_7 as given by equation II.9,

$$S_7=S_5(I_6/I_5)$$

II.9

10.Check for gain and power dissipation as given by equation II.10, II.11,

$$A_v=2g_{m2}g_{m6}/\{I_5(\lambda_2+\lambda_3)I_6(\lambda_6+\lambda_7)\}$$

II.10

$$P_{diss}=(I_5+I_6)(V_{dd}+|V_{ss}|)$$

II.11

11.Finally simulate the circuit to check if all specifications are met.
By performing the calculations for all design steps explained above, the values for aspect ratios of transistors used in the topology taken(Figure) are found.
For designing of CMOS op-amp ,design specifications have been provided in Table 1.

Table 1: Specifications taken for the design procedure[11]

Specification parameter	Value in 180nm technology	Value in 90nm technology
Channel length	0.18um	0.09um
Gain bandwidth	5MHz	5MHz
Phase margin	≥60°	≥60°
Slew rate	10V/us	10V/us
$V_{tho,p}$	-.042	-0.356
$V_{tho,n}$	0.39	0.408
C_l	10pf	10pf
λ_p	0.1/V	1.45/V
λ_n	0.09/V	0.48/V

III.SIMULATION RESULTS

To check if all the design specifications have been meet , we simulate the circuit shown in figure[1] whose working has been explained in section II .The circuit has been simulated in both 180nm and 90nm technology. All the results have been simulated using tanner EDA tools v14.1. The figure below shows the topology chosen in this work.

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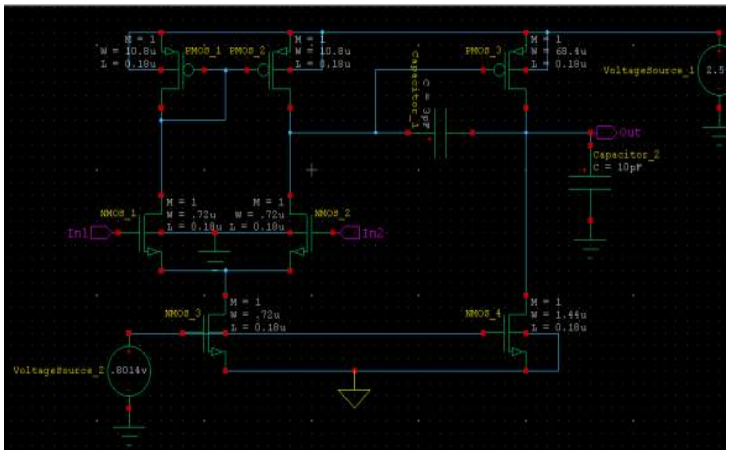

Figure 2 : Schematic implementation of the two stage CMOS Op-amp

Considering all the specifications taken in Table 1 and all the design steps explained in section II , aspect ratios of transistors used in the circuit were found. Since the length for each transistor is in accordance with the technology defined , that is, for 180nm technology the length taken is 180nm and for 90nm technology the length taken is 90nm , therefore the width of each transistor was calculated from the aspect ratio and length taken.
The table 2 below shows the aspect ratios of transistors for the designed Op-amp in both 180nm and 90nm technology.

Table 2: Aspect ratios taken for transistors

CMOS transistor	Aspect ratio(w/l) ; l=180nm	Aspect ratio(w/l) ; l=90nm
M1=M2	2	0.37
M3=M4	30	2.16
M5	2	0.78
M6	190	37.49
M7	4	0.68

From the table 2, the difference in the values of aspect ratios for 180nm and 90nm can be easily seen. The aspect ratio for transistors in 180nm technology is greater than that in 90nm technology. so from here it can be inferred that as the technology shrinks so does the transistor sizing.
In this paper, AC analysis and transient analysis have been performed to find values of various parameters such as open loop gain, unity gain bandwidth , power, delay and phase margin.

A.AC analysis:
Here gain, GB ,phase margin of the circuit have been determined by choosing start frequency to be 1MHz and stop frequency to be 10MHz. To perform AC analysis, sinusoidal waves were applied at both the inputs of the CMOS op amp. By performing AC analysis we got the curve for phase margin and voltage magnitude ,from which open loop dc gain(A_v), unity gain bandwidth(GB) and phase margin values were deduced.

The Figure 3 below shows the AC analysis curve using 180nm technology. The open loop dc gain was found using the voltage magnitude curve while the phase margin was calculated suing the voltage phase curve. The unity gain bandwidth was found using the voltage magnitude curve where it cuts the X- axis.
The values deduced for the parameters such as open loop dc gain(A_v), unity gain bandwidth(GB) and phase margin during the AC analysis in 180nm technology have been shown in the Table 3 below.

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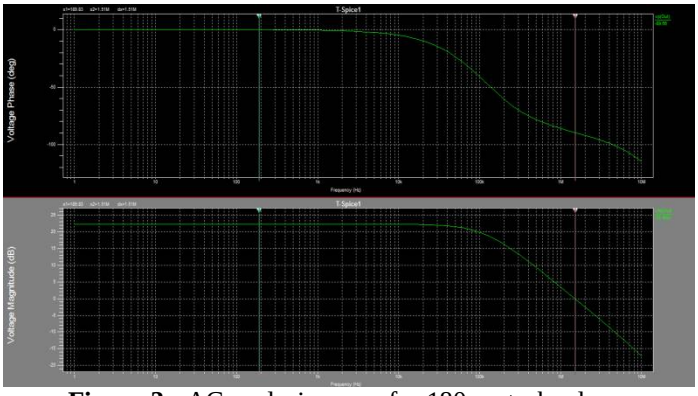

Figure 3 : AC analysis curve for 180nm technology

The Figure 4 below shows the AC analysis curve using 90nm technology. Here also, the open loop dc gain was found using the voltage magnitude curve while the phase margin was calculated suing the voltage phase curve. The unity gain bandwidth was found using the voltage magnitude curve where it cuts the X- axis. The difference in both the curves for 180nm and 90nm technologies can be easily seen from the graphs. The more clear difference between both 180nm an 90nm technologies can be inferred from the values deduced for the parameters mentioned in Table 3.
The values deduced for the parameters such as open loop dc gain(A_v), unity gain bandwidth(GB) and phase margin during the AC analysis in 90nm technology have been shown in the Table 3 below.

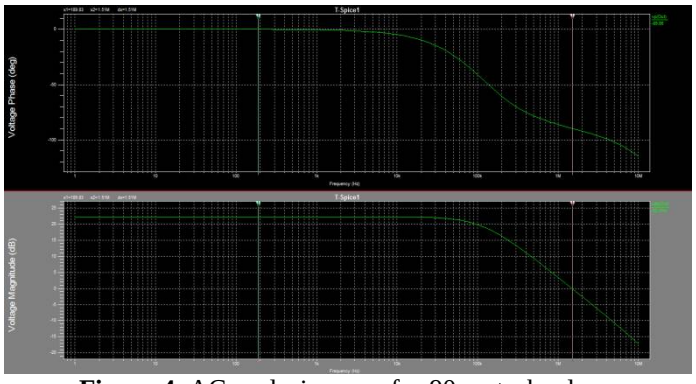

Figure 4: AC analysis curve for 90nm technology

Output results:
The Table 3 below shows the comparison of the parameter values achieved upon AC analysis in 180nm and 90nm technology. The value of open loop dc gain achieved is slightly more in 90nm technology while the unity gain bandwidth is around four times greater in 180nm technology. The phase margin achieved is higher in 90nm technology by an amount of 33.58°.

Table 3: Parameter values achieved upon AC analysis

Parameter	**180nm**	**90nm**
Gain	21.25db	22.28db
GB	5.05MHz	1.51MHz
Phase margin	94.02°	127.6°

To optimize these results , scaling of transistor sizing was done because the easiest way to achieve more gain is o increase the width and length values by a factor of 2 which due to the decreased value of ʎ ,increases the value of gain[9] . So here the widths of transistors M1 and M2 were increased by a factor of 2 giving the following output results shown in Table 4.

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Table 4: Parameter values achieved upon scaling during AC analysis

Parameter	**180nm**	**90nm**
Gain	20.95db	26.26db
GB	9.78MHz	5.05MHz
Phase margin	93.69°	82.89°

From the comparison drawn from Table 3 and Table 4 above ,it can be clearly analyzed that the value of gain has been increased and so has the unity gain bandwidth. The gain bandwidth(GB) has nearly doubled in 180nm technology while the GB has increased by a factor of 3 in 90nm technology. So the scaling of transistor sizing has improved the results achieved during AC analysis.

B.Transient Analysis:

This analysis helps us to determine the value of delay of Op-amp. Here the power has also been determined. The pulse width was taken to be 20ns and pulse period was taken to be 40ns. At the inputs pulse waves were given and the output was determined.

The Figure 5 below shows the transient analysis curve using 180nm technology. The X-axis represents the time in ns. The values deduced for the parameters such as delay and power during the transient analysis in 180nm technology have been shown in the Table 5 given below.

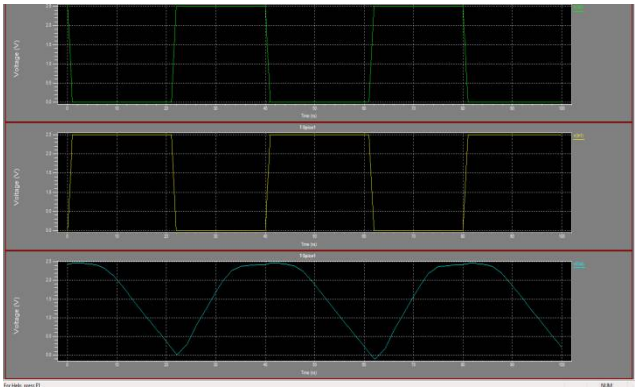

Figure 5 : Transient analysis curve for 180nm technology

The Figure 6 below shows the transient analysis curve using 90nm technology. The X-axis represents the time in ns. The values deduced for the parameters such as delay and power during the transient analysis in 90nm technology have been shown in the Table 5 given below.

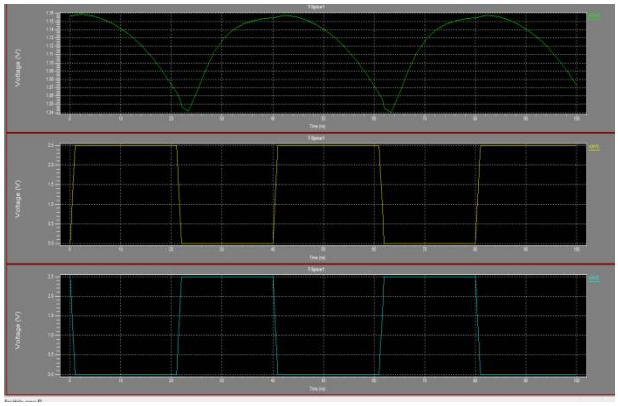

Figure 6 : Transient analysis curve for 90nm technology

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The difference in both the curves for 180nm and 90nm technologies can be easily seen from the graphs shown above. The output curve is more steeped in 180nm technology that is the delay in output is less in 180nm technology. The more clear difference between both 180nm an 90nm technologies can be inferred from the values deduced for the parameters mentioned in Table 5.

Output results:

The Table 5 below shows the comparison of the parameter values achieved upon transient analysis in 180nm and 90nm technology. The value of power consumed is more in 180nm technology while the value of delay is less in 180nm technology.

Table 5: Parameter values achieved upon transient analysis

Parameter	180nm	90nm
Power	.728mW	0.19mW
Delay	5.39ns	6.79ns

Again, as explained above in III.*A.* , scaling was performed and the values obtained are as shown below:

Table 6: Parameter values achieved upon scaling during transient analysis

Parameter	180nm	90nm
Power	.54mW	0.20mW
Delay	8.13ns	6.98ns

From the comparison drawn from Table 5 and Table 6 above ,it can be clearly analyzed that though the value of delay has slightly increased but the value of power consumed has been decreased by scaling .

IV.LAYOUT RESULTS

In this part, the layout for the two stage CMOS op-amp has been made in 180nm and 90nm technology. By doing so, we have verified our results achieved during the analysis performed above. Comparison has also been made for both 180nm and 90nm technology in terms of area and perimeter.

The layout design has been carried out in L-edit tool considering all the design rules and checking the DRC check at each step and the extract file was generated.

A. Layout design and parameters obtained in 180nm and 90nm technology:

The Figure 7 below shows the layout of two stage CMOS op-amp shown above in Figure 2 in 180nm technology.

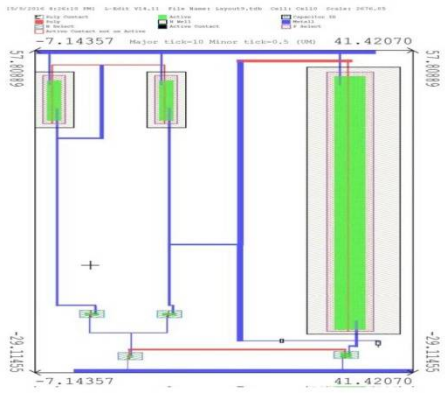

Figure 7 : Layout of CMOS op-amp in 180nm technology

The Figure 8 below shows the ac analysis curve for two stage CMOS op-amp deduced from the layout shown in Figure 7.The graph obtained in Figure 8 is used to find the parameters such as gain ,GB and phase margin in 180nm technology.

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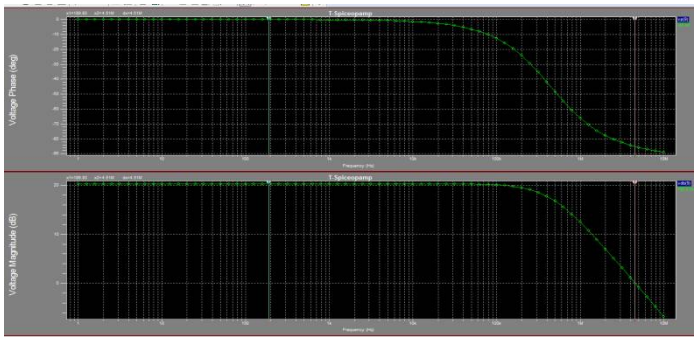

Figure 8 : AC analysis curve of CMOS op-amp in 180nm technology after layout

As can be seen from Figure 8 and Table 7 ,the values for parameters such as open loop dc gain ,unity gain bandwidth and phase margin were found to be almost same during the analysis for layout design.

Table 7: Parameter values achieved in 180nm technology before and after layout design

Parameter	Before layout	After layout
Gain	21.25db	20.26db
GB	5.05MHz	4.51MHz
Phase margin	94.02°	94.96°

From the Table 7 above , it can be inferred that the values are nearly same for the parameters so it verifies our design in 180nm technology.
The Figure 9 below shows the layout of two stage CMOS op-amp shown above in Figure 2 in 90nm technology.

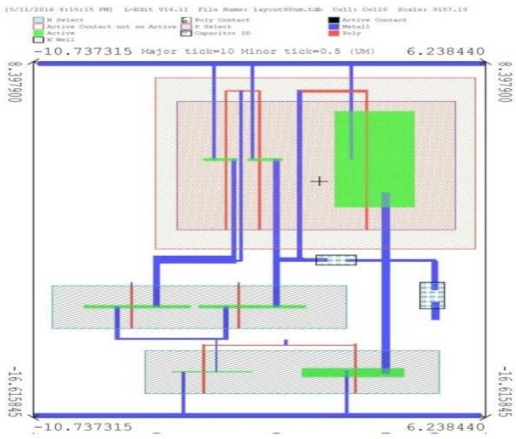

Figure 9 : Layout of CMOS op-amp in 90nm technology

The Figure 10 below shows the ac analysis curve for two stage CMOS op-amp deduced from the layout shown in Figure 9. The graph in Figure10 is almost same as that obtained in Figure 4 to find parameters like gain, GB and phase margin in 90nm technology.

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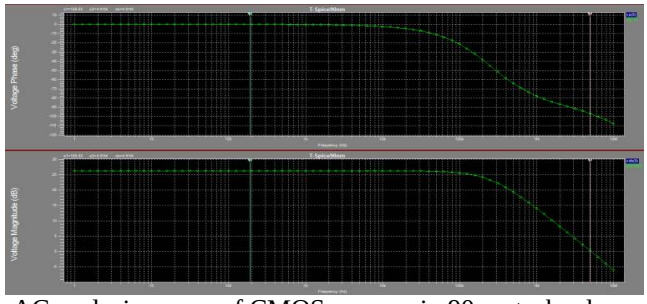

Figure 10 : AC analysis curve of CMOS op-amp in 90nm technology after layout

As can be seen from Figure 10 and Table 8 ,the values for parameters such as open loop dc gain ,unity gain bandwidth and phase margin were found to be almost same during the analysis for layout design.

Table 8: Parameter values achieved in 90nm technology before and after layout design

Parameter	**Before layout**	**After layout**
Gain	26.26db	26.23db
GB	5.05MHz	4.91MHz
Phase margin	82.89°	83.26°

From the Table 8 above , it can be inferred that the values are nearly same for the parameters so it verifies our design in 90nm technology.

B. Graphical Representation of Results obtained from Layout:

The following graphs give a more clear view of how the values of parameters such as gain, unity gain-bandwidth , phase margin have changed after layout. The values represented on the graphs for the parameters have been deduced during ac-analysis before and after layout in 180nm and 90nm technologies.

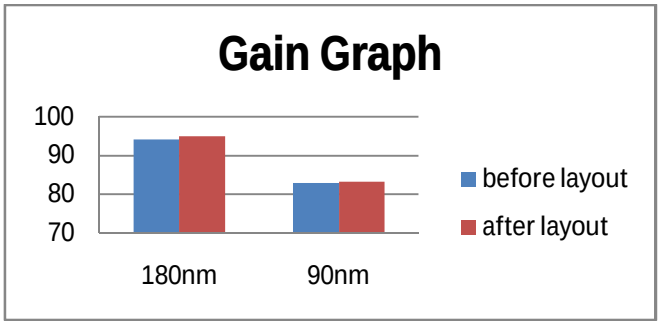

Figure 11 : Graph for open loop dc gain in 180nm and 90 nm technologies before and after layout

Figure 11 shows the open loop dc gain graph for a two stage CMOS op-amp before and after layout design for both 180nm and 90nm technologies. Here the X_axis represents the technologies used and Y-axis represents the values of open-loop dc gain in both 180nm and 90 technologies. The graphs have almost same values for the gain before and after layout.

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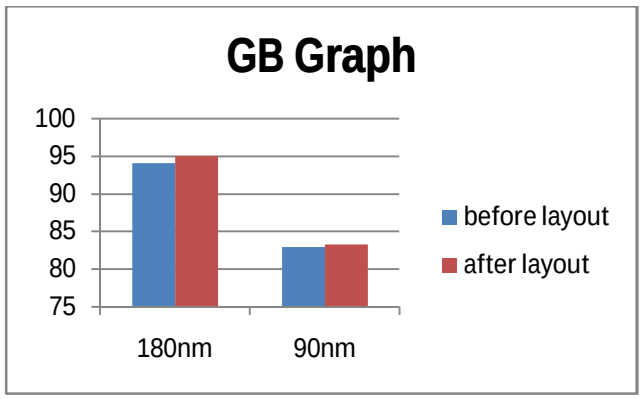

Figure 12 : Graph for unity gain bandwidth in 180nm and 90 nm technologies before and after layout

Figure 12 shows the gain bandwidth graph for a two stage CMOS op-amp before and after layout design for both 180nm and 90nm technologies. Here the X_axis represents the technologies used and Y-axis represents the values of unity gain-bandwidth in both 180nm and 90 technologies. The graphs have almost same values for the gain before and after layout.

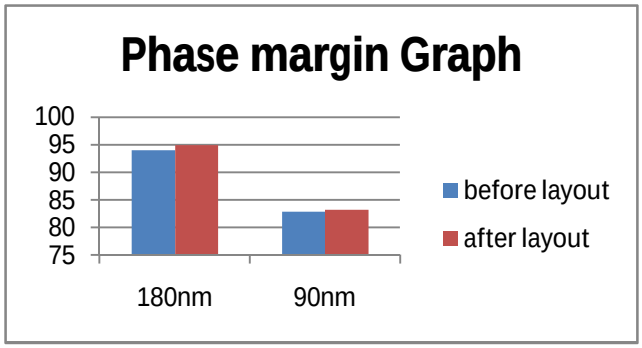

Figure 13 : Graph for phase margin in 180nm and 90 nm technologies before and after layout

Figure 13 shows the phase margin graph for a two stage CMOS op-amp before and after layout design for both 180nm and 90nm technologies. Here the X_axis represents the technologies used and Y-axis represents the values of phase margin in both 180nm and 90 technologies. The graphs have almost same values for the gain before and after layout.

The Table 9 below shows the comparison between 180nm and 90nm technology in terms of area and perimeter of the respective layout designs.

Table 9: Parameter values achieved in 180nm and 90nm technology

Parameter	**180nm**	**90nm**
Area	4221.37sq. units	424.627sq.units
Perimeter	135.48units	41.989 units

Here,1unit=1 lambda

From Table 9 , it can be deduced that the area consumed is much less for the layout design in 90nm technology.

V.CONCLUSION

This work presented the design of a two stage CMOS Op-amp in both 180nm and 90nm technologies. The open loop gain values of 21.25db,26.26db and unity gain bandwidth values of 9.78MHz,5.05MHZ have been achieved in this work for 180nm and 90nm technologies, respectively which are higher than the values achieved in work[5][10]. From

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the comparative analysis being done, it can be seen that when scaling is done, the gain achieved is more in 90nm technology by an amount of 5.31db while in 180nm technology , GB almost two times that in 90nm technology has been achieved. Finally, the layout design for both 180nm and 90nm technologies have verified the work done as shown in Table 7 and Table 8.

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