VLSI Design and Implementation of Schmitt Trigger based VCO for PLL Architecture

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ABSTRACT: this paper proposes the transient and phase noise analysis of Schmitt trigger circuit based CSVCO which will give clean square pulses from noisy input signals with less phase noise and also applicable for low power. This Schmitt based CSVCO is used in PLL architecture which further can be applicable for frequency synthesis, data recovery, tracking input signals such as in tracking generators(ex: car's cruise control),clock generation etc. After simulation i.e., after performing analysis of phase noise it provides phase noise of -106dbc/Hz at the offset frequency of 1MHz. This transient and phase noise simulation is performed in Mentor Graphics tool i.e., Pyxis (eldo) in 130nm technology.

KEYWORDS: PLL(Phase Locked Loop), PD(Phase detector), LPF(Low pass filter), CSVCO(Current starved VCO), VCO(Voltage controlled oscillator), CP(Charge Pump).

I.INTRODUCTION

In this paper the PLL is a phase locked loop which is a negative feedback system where we are locking the two phases i.e., the input phase is compared with the output phase which is the result of Schmitt trigger based CSVCO. PLL is generally a synchronizing circuit which synchronizes the output signal which is the result of Schmitt based CSVCO with the reference input signal. The objective of this paper is to generate the clean square pulses even though there is a noisy input signals from the VDD variation. Where this is very important in order to get locked condition properly or fine tune of PLL. In PLL VCO is heart of the architecture so we have to tune it properly to get locked. This Schmitt based CSVCO can be used in wireless communication (satellite communication) applications. The Block diagram for PLL is shown in figure below which consists of:
1. PD(Phase Detector)
2. CP(Charge Pump)
3. LPF(Low Pass Filter)
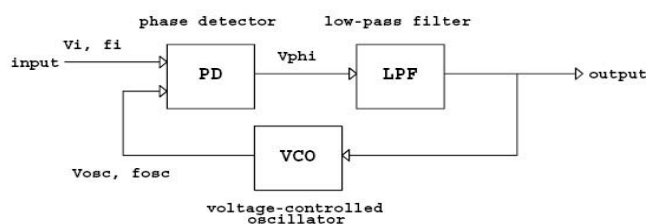4. Schmitt based current starved VCO(CSVCO)

Figure 1 Block diagram of PLL

Phase Detector detects the phase error between the input (Vi) and signal (Vosc) i.e., generated from the VCO and produces phase error proportionated output voltage (Vphi). This voltage is fed to the LPF which will produces the control voltage required for tuning the VCO. Then the output of VCO is fed back to the PD to get locked and to give feedback path hence PLL is a negative feedback system as shown in above block diagram.

The paper is organized as related work in section II, proposed methodology in section III, equations in section IV,measurement, simulation results and waveformsin section V and conclusion in section VI.

II. RELATED WORK

In previous PLL design they were using ring oscillator based VCO where, in order provide high tuning range or frequency range they were increasing VDD that means tuning range is dependent on VDD. If we increase VDD by ± 10 we used to get frequency range from 1-3GHz but VCO will become unstable. So to make independent of VDD we are increasing tuning voltage to get high frequency range.

III.PROPOSED METHODOLOGY

Phase Detector with Charge Pump:Usually PD will compare the phases of two input signals and produces output voltage. If the phases of two signals are different then it produces up and down pulses. The error voltage is produced by integration and subtraction of these up and down pulses in order to tune or control the VCO. This error voltage is fed to the charge pump in order to pump in and pump out the charge from LPF in order to increase or decrease the control voltage required for VCO.
Charge Pump is basically used to convert the digital pulses produced by up and down signals into continuous signals as analog one.
LPF: The output of PD usually consists of high frequency as well as dc components where first component is undesired so LPF is used to attenuate the high frequency components coming from the PD output and hence passes the dc to the Schmitt based CSVCO to tune it.
Schmitt based CSVCO: we are using Schmitt based CSVCO in order to produce clean square pulses even in the variation of VDD or input voltage coming from LPF which produces noisy signals.Instead of varying the supply voltage VDD in order to tune the VCO to get a frequency range from few Hzs to thousands of Hzs we are varying the control voltage which will acts as input voltage coming from LPF as shown in below figure 2. The operation of below VCO is similar to that of normal ring oscillator.
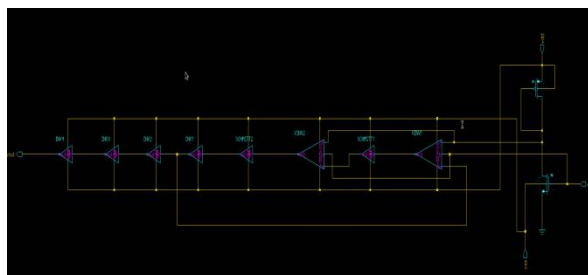

Figure 2 Schmitt based current starved VCO

As normal topology it is followed by inverters at the end. In this circuit we are using Schmitt trigger circuit in betweencurrent starved inverters to get clean square pulses. As we know that inverters are starved or hungry for current so we are using current starved inverters instead of normal inverters which will limit the current in order to charge or discharge the internal node capacitance of the MOS devices. Further in order to maintain the constant current inside each inverter we are using current mirror circuit at the input stage as shown in above figure 2.
The above VCO starts to oscillate when vin$\geqslant$ vthn it will produces maximum frequency when vin=VDD and minimum frequency when vin=vthn and normally stops oscillating when input voltage is less than threshold i.e., because NMOS will enter into cut off region (vin<vthn).
The drain currents of inverters are set by the control input voltage i.e., Vcont.
The oscillation frequency for this above VCO is given by

$$f = \frac{1}{2NT}$$

Where

$$\Gamma = t_1 + t_2$$

And N is number of stages

The internal total capacitance at the input and output node is given as

$$C_{tot} = C_{out} + C_{in}$$

$$C_{tot} = C_{ox}(W_p L_p + W_n L_n) + \frac{3}{2} C_{ox}(W_p L_p + W_n L_n)$$

$$C_{total} = \frac{5 \cdot C_{ox}(W_p L_p + W_n L_n)}{2}$$

The MOSFETs M1 and M2 at the input stage acts as current sources to maintain drain current inside the inverters which is set by Vcont.

The frequency ranges for different values of control voltage set by the control mechanism is given in below table (1).

Table 1 frequency ranges

0.42V	152.89MHz
0.6V	686.01MHz
0.8V	1.315GHz
1V	1.7970GHz
1.2V	2.1819GHz
1.4V	2.4643GHz
1.8V	2.873GHz
2V	2.9971GHz
2.2V	3GHz
2.4V	3.134GHz
2.6V	3.2GHz
2.8V	3.2209GHz
3V	3.2406GHz

IV. EQUATIONS

The closed loop transfer function of PLL that is given below in the form of mathematical description of both VCO and PD

$$\frac{C_o}{R_i}(s) = \frac{G(s)}{1 \pm G(s)H(s)}$$

The above equation is obtained from evaluation of below figure3.

Where,

Positive sign = for positive feedback

Negative sign= for negative feedback

$\frac{Co}{Ri}$ =the closed loop transfer function

G(s) = forward transfer function

H(s) = feedback transfer function

G(s)H(s) = open loop transfer function

G(s)H(s) = for positive feedback it has ration of 1 and angle of 0^0 and for negativeit has 180^0 these are for oscillations.
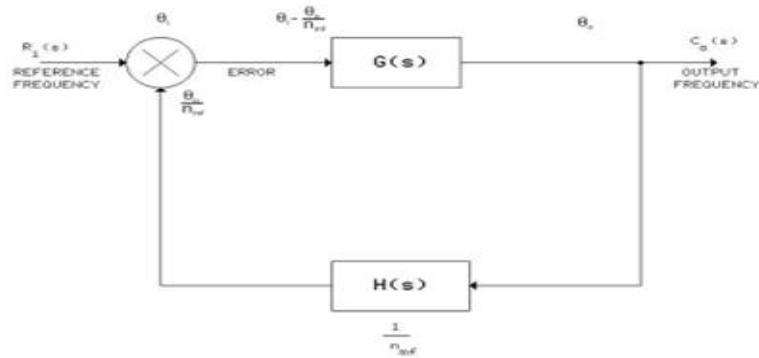
Figure 1 control systems block diagram of PLL

V. MEASUREMENT, SIMULATION RESULTS AND WAVEFORMS

The above designed PLL is used in many applications such as wireless application. It is designed using 130nm technology Mentor Graphics tool.

The above Schmitt based CSVCO will work for supply voltage of 1V-3V.The PLL is designed using 130nm CMOS technology with 1.9v supply voltage. The transient analysis of Schmitt trigger based CSVCO at each stage is given in figure (4). The power consumed by Schmitt based CSVCO is 240.411uW for 1v supply and for 3V it consumes 11.579mW.The transient analysis of complete integrated PLL is shown in figure (7) where red colour waveform is reference input signal and green one is control input voltage to CSVCO and blue is resultant signal from Schmitt based CSVCO where will get clean square wave pulses.
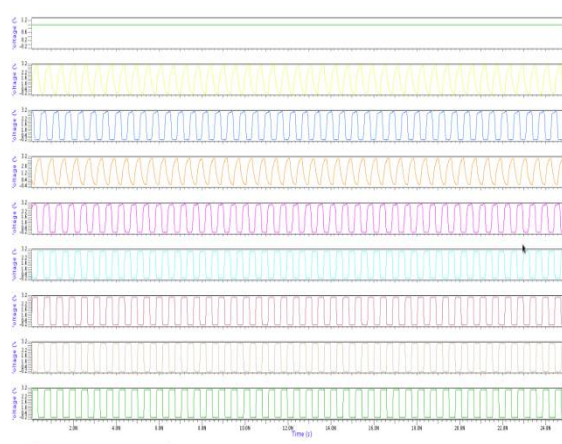

Figure 3 The transient analysis of Schmitt trigger based
CSVCO at each stage

This will results a Phase Noise at 1MHz offset frequency is -106dBc/Hz which is shown in below figure (5)
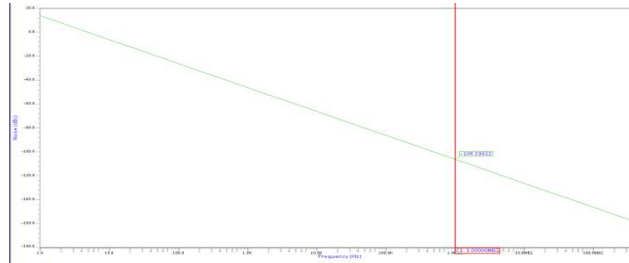
Figure 4 Phase noise of VCO

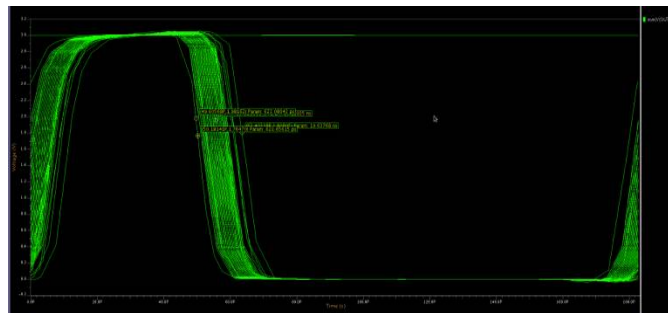The eye diagram for Schmitt based CSVCO is given in figure (6)

Figure 5 Eye diagram

The transient analysis of complete integrated PLL is shown in figure (7) where red colour waveform is reference input signal and green one is control input voltage to CSVCO and blue is resultant signal from Schmitt based CSVCO where will get clean square wave pulses.
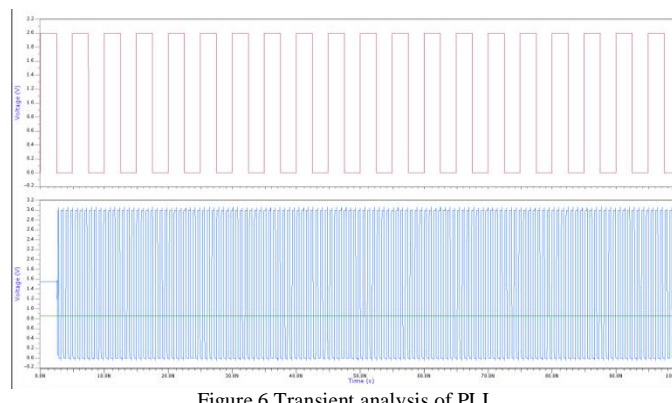

Figure 6 Transient analysis of PLL

Table 2 Result comparison

parameters	[13]	[4]	[7]	[11]	[8]	proposed work
Operating frequency(GHz)	0.39-1.41	0.12-1.3	0.528	0.0022-0.008	0.125-2.4	0.152-3.2406
Phase Noise	no	yes	yes	no	no	yes
VDD (V)	1.8	0.5	1.8	0.5	1.8	1-3
Technology(nm)	180	180	180	180	180	130
Power consumption (mW)	12.5	0.085	143	14.5	19.8	11.5796
Passive components used	yes	yes	no	yes	yes	yes

VI. CONCLUSION

The PLL design can be used in many high performance applications such as wireless applications where it requires a high performance. This is designed in 130nm CMOS technology using Mentor Graphics tool that is Pyxis for schematic simulation. This entire integrated PLL consumes 63mW power with supply of 1.9V. The implemented Schmitt trigger circuit based current starved VCO consumes 240.4113uW for supply 1V and 11.5796mW for supply 3V. This VCO has better Phase noise of -106dBc/HZ at offset frequency of 1MHz. As frequency increases power consumption will increases. So instead of increasing supply we are increasing control voltage to increase the frequency range

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