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Low Power Re-Configurable DCT for High Speed Mixed Signal DSP

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ABSTRACT: The proposed approximation of DCT provides comparable or better image and video compression performance and power than the existing approximation methods. This paper presents a generalized recursive algorithm to obtain orthogonal approximation of DCT where an approximate DCT of length N could be derived from a pair of DCTs of length (N/2) at the cost of N additions for input pre-processing. Proposed algorithm is highly scalable for hardware as well as software implementation of DCT of higher lengths, and it can make use of the existing approximation of 8-point DCT to obtain approximate DCT of any power of two length, N>8 . It performs recursive sparse matrix decomposition and makes use of the symmetries of DCT basis vectors for deriving the proposed approximation algorithm. One uniquely interesting feature of the proposed design is that it could be configured for the computation of a 32-point DCT or for parallel computation of two 16-point DCTs or four 8-point DCTs with a marginal control overhead. The proposed architecture is found to offer many advantages in terms of hardware complexity, regularity and modularity. This Proposed System Implemented using Verilog HDL and Simulated by Modelsim 6.4 c and Synthesized by Xilinx tool.

KEYWORDS: Algorithm-architecture codesign, DCT approximation, discrete cosine transform (DCT), high efficiency video coding (HEVC).

I. INTRODUCTION

The Discrete cosine transform (DCT) is popularly used in image and video compression. Since the DCT is computationally intensive, several algorithms have been proposed in the literature to compute it efficiently. Recently, significant work has been done to derive approximate of 8-point DCT for reducing the computational complexity. The main objective of the approximation algorithms is to get rid of multiplications which consume most of the power and computation- time, and to obtain meaningful estimation of DCT as well. The signed DCT (SDCT) for 8 8 blocks where the basis vector elements are replaced by their sign Bouguezel-Ahmad-Swamy (BAS) have proposed a series of methods.

They have provided a good estimation of the DCT by replacing the basis vector elements by 0, 1/2, 1. In the same vein, Bayer and Cintra have proposed two transforms derived from 0 and 1 as elements of transform kernel, and have shown that their methods perform better than the method. Particularly for low- and high-compression ratio scenarios. The need of approximation is more important for higher-size DCT since the computational complexity of the DCT grows nonlinearly. On the other hand, modern video coding standards such as high efficiency video coding (HEVC) uses DCT of larger block sizes (up to 32 32) in order to achieve higher compression ratio. But, the extension of the design strategy used in H264 AVC for larger transform sizes, such as 16-point and 32-point is not possible. Besides, several image processing applications such as tracking and simultaneous compression and encryption require higher DCT sizes. In this context, Cintra has introduced a new class of integer transforms applicable to several block-lengths. Cintra et al. have proposed a new 16 16 matrix also for approximation of 16-point DCT, and have validated it experimentally. Recently, two new transforms have been proposed for 8-point DCT approximation: Cintra et al. have proposed a low-complexity 8-point approximate DCT based on integer functions and Potluri et al. have proposed a novel 8-point DCT approximation that requires only 14 addition. On the other hand, Bouguezel et al. have proposed two methods for multiplication-free approximate form of DCT.

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The first method is for length , 16 and 32; and is based on the appropriate extension of integer DCT. Also, a systematic method for developing a binary version of high-size DCT (BDCT) by using the sequency-ordered Walsh-Hadamard transform (SO-WHT) . This transform is a permutated version of the WHT which approximates the DCT very well and maintains all the advantages of the WHT. A scheme of approximation of DCT should have the following features: i) it should have low computational complexity. ii) It should have low error energy in order to provide compression performance close to the exact DCT, and preferably should be orthogonal.

A common research question is range of performance improvements that may be achieved by augmenting general purpose processor with reconfigurable core. The basic idea of such approach is to exploit both general purpose capability and to achieve better performance for large class of applications. FPGA provides that flexibility to implement application specific computations. Such DCT/IDCT implementation mapped on FPGA will discuss here. Transform coding constitutes an integral component of substantial bottlenecks in visual data compression algorithms, filtering and other fields. Many DCT algorithms with efficient hardware software algorithms have been proposed. It has become a heart of international standard such as JPEG, H.26x, and MPEG family.

There are four types of DCT labeled as I-IV. Among them, DCT type II is mostly used. This is used in JPEG and video codec. The theoretical lower bound on the number of multiplications required for 1 D eight point DCT has been proven to be 11. In this sense, the method proposed by Loeffler with 11 multiplications and 29 additions is most efficient solution. The entire fast algorithm still require floating point multiplication which is slow in both hardware and software implementation. To achieve faster implantation, coefficients can be scaled and approximated by integer such as floating point multiplication can be replaced by integer multiplication. This can be done by rounding floating point value to integer value by multiplying floating point value with. Whereas can be any integer number This is called as fixed point arithmetic. The resulting algorithms are much faster than the original version and therefore have wide practical applications.

II. RELATED WORK

In 2006 Low-power High-performance DCT Architecture by Ahmed M. Shams, Archana Chidanandan
A new DA architecture called NEDA, aimed at reducing the cost metrics of power and area while maintaining high speed and accuracy in digital signal processing (DSP) applications. Mathematical analysis proves that DA can implement inner product of vectors in the form of two's complement numbers using only additions, followed by a small number of shifts at the final stage. Comparative studies show that NEDA outperforms widely used approaches such as multiply/accumulate (MAC) and DA in many aspects. Being a high-speed architecture free of ROM, multiplication, and subtraction, NEDA can also expose the redundancy existing in the adder array consisting of entries of 0 and 1. A hardware compression scheme is introduced to generate a butterfly structure with minimum number of additions. NEDA-based architectures for 8 8 discrete cosine transform (DCT) core are presented as an example. Savings exceeding 88% are achieved, when the compression scheme is applied along with NEDA. Finite word-length simulations demonstrate the viability and excellent performance of NEDA. We propose a novel distributed arithmetic paradigm named NEDA for VLSI implementation of DSP algorithms involving inner product of vectors. Mathematical proof is given for the validity of the NEDA scheme. We demonstrate that NEDA is a very efficient architecture with adders as the main component and free of ROM, multiplication, and subtraction. For the adder array, a systematic approach is introduced to remove the potential redundancy so that minimum additions are necessary. The effectiveness of this compression scheme is shown in an 8 1 DCT architecture employing NEDA, where over 88% of reduction in hardware is achieved. Finite word-length simulation of a 8 DCT core reveals that the NEDA is an accuracy preserving scheme and capable of maintaining a satisfactory performance even at low DA precision. Unlike existing hardware optimization algorithms at high synthesis levels, NEDA is directly mappable to low-level DSP hardware. This is self-evident in the NEDA-based 8 8 DCT core architecture developed as an example. Being scalable with differing precision requirement is another merit of NEDA, which, as a whole, is a high-performance methodology for power/area efficient digital designs.
In 2012 Zero-Quantised Discrete Cosine Transform Coefficients Prediction Technique for Intra-frame Video Encoding by Maher jridi, Pramod kumar meher, Ayman alfalou.
Identified one promising solution to reduce the computational complexity of discrete cosine transform (DCT) . The redundant computations and to get rid of them. In this study, the authors present a new method to predict zero-

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quantised DCT coefficients for efficient implementation of intra-frame video encoding by identifying such redundant computations. Traditional methods use the Gaussian statistical model of residual pixels to predict all-zero or partial-zero blocks. The proposed method is based on two key ideas. At first, the bounds of DCT coefficients are derived from the intermediate signals of the Loeffler DCT algorithm instead of calculating the sum of absolute difference (SAD) of residual pixels. The sufficiency conditions are then suitably chosen to predict the zero-quantised coefficients to reduce the arithmetic complexity without degrading the video quality. Simulation results are found to validate the analytical model and show that the proposed prediction eliminates more redundant computations than the existing methods. Moreover, the authors have derived a pipelined VLSI architecture of the proposed prediction scheme which offers a saving of more than 63 and 91% of multiplications of the second stage of one-dimensional DCT for high and low bit-rate intra-video encoding, respectively. In this paper, we have derived analytical bounds, and proposed an efficient ZQDCT coefficients prediction with zero FAR, which significantly reduces the CC of intra-frame video encoding. The proposed bounds are based on behaviour of DCT coefficients and obtained from intermediate values in Loeffler DCT algorithm. We have showed that a considerable performance gain over the existing methods is achieved in terms of overall CC and video quality. We have also shown that the proposed prediction method is more suitable for a VLSI implementation and involves very low overhead for zero detection. Therefore the proposed method can be used for efficient ZQDCT prediction in intra-frame video coding and can be combined with other methods for inter-frame ZQDCT determination for video encoding.

In 2012 Binary Discrete Cosine and Hartley Transforms by Saad Bouguezel, M. Omair Ahmad, and M. N. S. Swamy Proposes a systematic method for developing a binary version of a given transform by using the Walsh-Hadamard transform (WHT). The resulting transform approximates the underlying transform very well, while maintaining all the advantages and properties of WHT. The method is successfully applied for developing a binary discrete cosine transform (BDCT) and a binary discrete Hartley transform (BDHT). It is shown that the resulting BDCT corresponds to the well-known sequency-ordered WHT, whereas the BDHT can be considered as a new Hartley-ordered WHT. Specifically, the properties of the proposed Hartley-ordering are discussed and a shift-copy scheme is proposed for a simple and direct generation of the Hartley-ordering functions. For software and hardware implementation purposes, a unified structure for the computation of the WHT, BDCT, and BDHT is proposed by establishing an elegant relationship between the three transform matrices. In addition, a spiral-ordering is proposed to graphically obtain the BDHT from the BDCT and vice versa. The application of these binary transforms in image compression, encryption and spectral analysis clearly shows the ability of the BDCT (BDHT) in approximating the DCT (DHT) very well. In this paper, an efficient method for developing the binary version of a given transform has been proposed by exploiting the Walsh-Hadamard transform (WHT) and successfully applied for developing binary discrete cosine transform (BDCT) and binary discrete Hartley transform (BDHT). It has been shown that the resulting BDCT corresponds to the well-known sequence ordered WHT, whereas the BDHT can be considered as a new Hartley-ordered WHT and added to the list of the existing orderings. This new ordering is very useful, since it approximates the DHT very well, and hence is an efficient alternative to the well-known DFT for real data applications. Special attention has been given to this new ordering by discussing its properties and proposing a shift-copy scheme allowing for a direct generation of a Hartley-ordering function of any order for any length. In order to develop a unified structure for the computation of the WHT, BDCT and BDHT, an elegant relationship between the three transforms has been established and expressed in a matrix form. In addition, a spiral-ordering scheme has also been proposed for an easy graphical construction of the BDHT from the BDCT and vice versa. These relationships are very important for the implementation and construction of the Hadamard orderings. By considering some signal processing applications such as image compression, encryption and spectral analysis, it has been shown that the performance of the proposed binary transforms is very close to that of their corresponding original transforms and much superior to that of the signed versions of the latter. Moreover, in contrast to the signed-version transforms, the proposed binary-version transforms maintain all the advantages and properties of the WHT, namely, lower computational complexity, simplicity, regularity, orthogonality, and requiring no multiplication operations.

III. PROPOSED SCHEME

Pipelined and non-pipelined designs of different methods are developed, synthesized and validated using an integrated logic analyzer. The validation is carried out by using the Digilent EB of Spartan6-LX45. We have used 8-bit inputs, and we have allowed the increase of output size (without any truncations). For To assess the computational complexity of proposed -point approximate DCT, we need to determine the computational cost of matrices quoted. The

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approximate 8-point DCT involves 22 additions. The 8-point transform we have 11-bit and 10-bit outputs. The pipelined design are obtained by insertion of registers in the input and output stages along with registers after each adder stage, while the no pipeline registers are used within the non-pipelined designs. The synthesis results obtained from XST synthesizer are presented.

It shows that pipelined designs provide significantly higher maximum operating frequency (MOF). It also shows that the proposed design involves nearly 7%, 6%, and 5% less area compared to the BDCT design for equal to 16, 32, and 64, respectively. Note that both pipelined and non-pipelined designs involve the same number of LUTs since pipeline registers do not require additional LUTs.

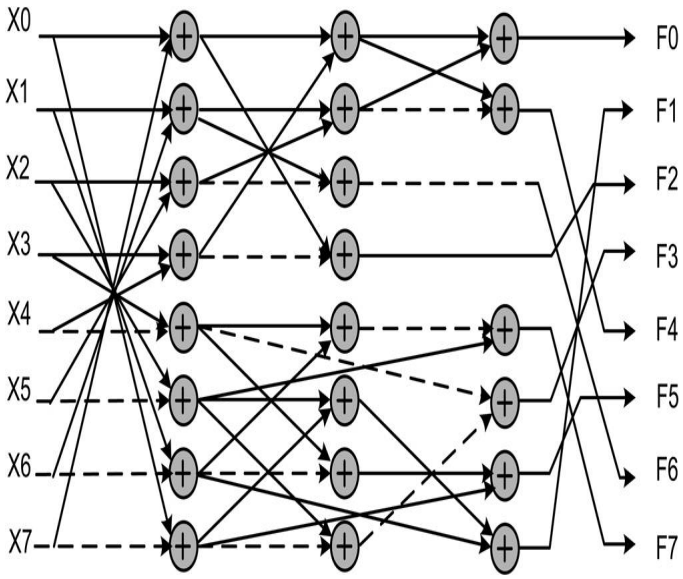

Fig.1 SIGNAL FLOW GRAPH (SFG) OF (C8)

IV. EXPERIMENTAL RESULTS

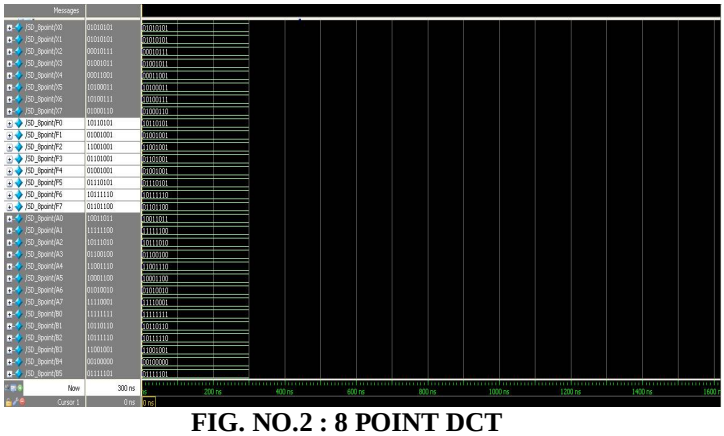

FIG. NO.2 : 8 POINT DCT

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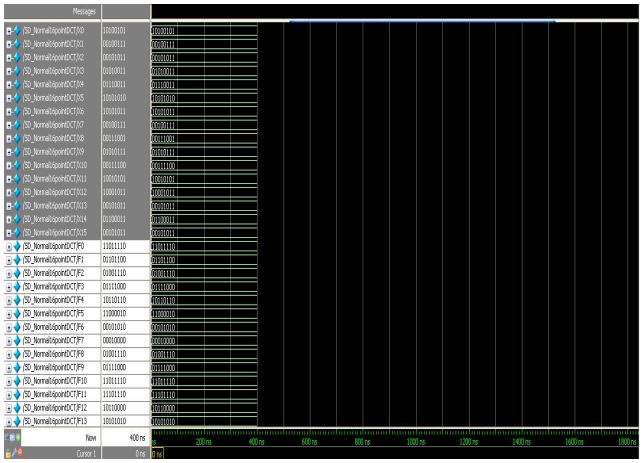

FIG. NO. 3 : NORMAL 16 DCT POINT

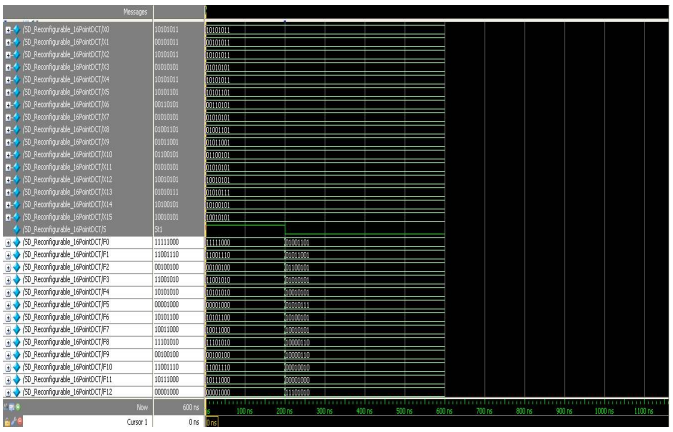

FIG. NO. 4: RECONFIGURABLE 16 POINT DCT

V. CONCLUSION

In this paper, we have proposed a recursive algorithm to obtain orthogonal approximation of DCT where approximate DCT of length could be derived from a pair of DCTs of length at the cost of additions for input preprocessing. The proposed approximated DCT has several advantages, such as of regularity, structural simplicity, lower-computational complexity, and scalability. Comparison with recently proposed competing methods shows the effectiveness of the proposed approximation in terms of error energy, hardware resources consumption, and compressed image quality. We have also proposed a fully scalable reconfigurable architecture for approximate DCT computation where the computation of 32-point DCT could be configured for parallel computation of two 16-point DCTs or four 8-point DCTs.

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