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Low Power DTCWT Architecture for Video Analytics Applications KS

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ABSTRACT: In this paper we have proposed a novel low power architecture for object detection based on dual tree complex wavelets. The proposed system is capable of tracking the moving object in video sequences. The novel gate level datapath architectures are proposed. The industry standard FPGA methodology is used to benchmark & demonstrate the proposed concepts. The design is synthesized in the Xilinx tool, and architecture is simulated using the model sim simulator, the targeted board is virtex II. The results show that the proposed architectures reduce all the design constraints area, timing & power..

KEYWORDS: Video analytics (Vo), Dual tree complex wavelet transform (DTCWT), Low power VLSI, Data path.

I.INTRODUCTION

Historically cameras have been steered by loss prevention staff to track suspected shoplifters, achieving high-resolution covert observation .Such streams are recorded to provide evidence for convictions. In addition, cameras not being actively controlled may be recorded to provide a record of activities in important areas, such as entrances and high-value item displays. The advent of digital video recorders has dramatically improved the access to this recorded video enabling faster investigation of past events by direct access based on recording time, when the time of an event is known. The development of intelligent video processing algorithms is bringing many new applications for video within stores, both in the traditional domain of loss prevention, and in store operations and merchandising. Closed Circuit Television (CCTV) has long been used within shops for the detection of shoplifting. CCTV systems have proved to have a variety of uses to justify investment as deterrent, record for insurance claims, public safety, stock tracking and employee fraud detection but they are still labour intensive and it is difficult to extract useful information from them. Video analytics are functions typically used in video surveillance applications that Automatically analyze live video streams to detect moments in time that are not based on a single image. They can be easily compared to an automated, artificial intelligence visual cortex of the brain – the part that assesses visual images. State-of-the-art video analytics algorithms or complex math functions made possible through a digital signal processor in a video camera, to detect, track and map the Positions of people, vehicles and other objects as they move and interact in the camera's field of view. Video analytics are commonly used in video security applications for retail stores, community venues and transportation points. Video analytics can also be used in entertainment and health care applications. So examples of the video analytics are:

- **Motion detection** is used to determine the presence of motion in an area being observed by a video camera or Motion detector. Motion detection is a common feature in video security alarm systems.
- **Object detection** determines the presence of people or objects being captured through video and relays what type of objects they are real-time. This type of video analytics can include fire and smoke detection.
- **Face recognition** can capture and possibly identify people, which is helpful for video airport security for terrorism or criminal detection. The same type of analytics can be used for automatic license plate recognition.
- **Tamper detection** enables an alarm to alert the proper entity when a camera or output signal has been compromised. Tamper detection is a popular feature in video security systems for retail stores.
- **Video tracking** determines the location of people or objects captured in a video signal and locates them on an External reference grid to find them.

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In recent years; many studies have been made on wavelets. Image compression is one of the most visible applications of Wavelets. The rapid increase in the range and use of electronic imaging justifies attention for systematic design of an image compression system and for providing the image quality needed in different applications.
In the DT-CWT, real valued wavelet filters produce the real and imaginary parts of the transform in parallel decomposition trees, permitting exploitation of well-established real-valued wavelet Implementations and methodologies. A primary advantage of the DT-CWT lies in that it results in decomposition with a much higher degree of directionality than that possessed by the traditional DWT. Rest of the paper is organized as follows: Section 2 of this paper gives overview of Video analytics, Section 3 describes the existing architecture and section 4 describes proposed low power architecture. Section 5 deals about results and Observations. At last, the Section 6 of this paper describes the conclusions and future scope.

II. VIDEO SURVEILLANCE SYSTEMS

Definition: "A video surveillance system monitors the behaviour, activities, or other changing information, usually, of people from a distance by means of electronic equipment."Video analytics can be described as following figure.

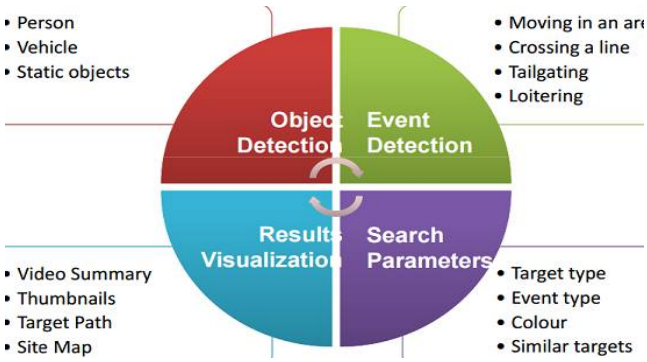

Fig: 1 Video Surveillance System

Video surveillance systems are typically installed to record video footage of areas of interest within a facility, around its perimeter or in outdoor areas which require observation, with a view to "catching" (allowing the user to be able to observe) and recording events related to security, safety, loss prevention, operational efficiency and even business intelligence. Video Analytics enhances video surveillance systems by performing the tasks of real-time event detection, post-event analysis and extraction of statistical data while saving manpower costs and increasing the effectiveness of the surveillance system operation. Below are the applications of Video Analytics:

- **Video Analytics for Real-Time Detections & Alerts**
- **Video Analytics for Investigation (Video Search)**
- **Video Analytics for Business Intelligence**

III. VIDEO ANAYLTICTS

Video surveillance systems produce massive amounts of video. The main part of that video is never watched or reviewed, due to lack of time or resources. As a result, security incidents will be missed and suspicious behaviour will not be noticed in time to prevent incidents. Video analytics is about reducing the vast amount of information contained in video, making it more manageable for systems and people. Video analytics surveillance systems automatically perform an analysis of captured video, making the resulting data useful by tagging it with appropriate labels. Incorporating video analytics into network cameras creates a versatile video surveillance system, drastically reducing workload for staff. Video analytics also makes it possible for an operator to use the surveillance system proactively, receiving early warnings about situations that could constitute potential risks. Video analytics can also be used for business intelligence purposes, for example, to analyse customer behaviour and improve customer experience.

Why to use video analytics**:** Video analytics offers a wealth of benefits, such as a more efficient use of staff, reduced costs for storage and servers, and faster access to stored video. By means of video analytics, systems can be set up to

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deliver far more targeted and specific information, creating increased business value. Video analytics automatically analyzes and tags surveillance video in real-time. Video analytics detects suspicious activities and initiates video recording, triggers alarms or other actions, alerting operators or field personnel. By automatically monitoring video for security incidents, video analytics can give users early warnings, making it possible for them to prevent crime rather than just react to it or analyze it after the incident. The various advantages of video analytics are Efficient use of manpower, Reduced network load and storage needs, Faster retrieval of stored video, New business opportunities.

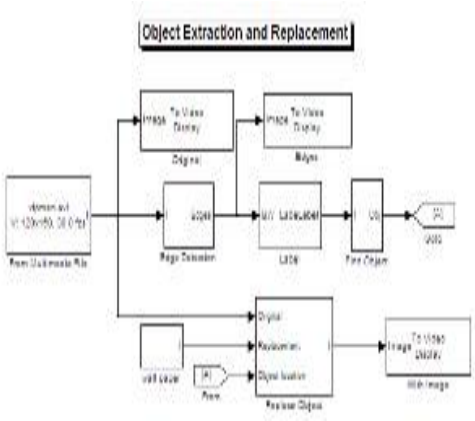

Fig 2 Extraction and Replacement Model

Figure 2 shows the object extraction and replacement model, it consists of edge detection, find object and object replacement algorithms. The input is taken from multimedia file, the Vipmen video in the avi format (size is 120*160 and 30 fps) is applied. There exists a different kind of edge detection algorithms, named like canny, Prewill, Robert, sobel. The resulted output is applied to the object algorithm in order to find the location of the object for replacement in the replacement algorithm. This algorithm supports the different kinds if the relational operators such as (==,>,>=, <,=<). The output of this model consists of three different videos such as original video, edge detected video for different edge detection algorithms and object replacement video for different relational operations performed on different edge detected algorithms

IV. ARCHITECTURE FOR DTCWT

DTCWT is a complex algorithm and consumes time, and hence requires suitable architecture for data processing in real time. In this work, efficient architecture for DTCWT is developed and implemented on FPGA.

Complex Dual Tree CWT: The CDTCWT generally composed of two separate decomposition trees among which one tree is considered to be as real tree and other is considered to be as imaginary tree, which is indicated in figure 2. Here the DTCWT uses H0 and H1 low pass and high pass filter respectively for the H tree computation, G0 and G1 the low pass and high pass filters for G tree computation.

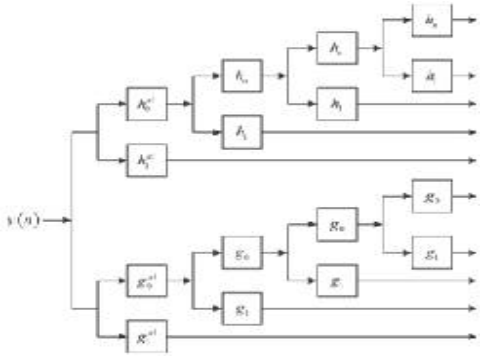

Fig 3 Kingsbury's dual-tree CWT

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Figure 3 shows the analysis or demodulation structure for dual tree CWT. The inverse dual tree CWT or the modulation structure is indicated in the figure 3.2. The computation of the inverse transform of CWT is done by inversing the real and imaginary part of the forward transforms filters.

The low pass filters in the H tree (g0) and G tree (h0) need to satisfy half sample delay property **[16]** as given in Equation (1).

$$G_0(e^{j\omega}) = e^{-j0.5\omega}H_0(e^{j\omega}), - - -(1)$$

The expression in Equation (1) can be rewritten in terms of magnitude and phase function as shown in Equation (2).

$$|G_0(e^{j\omega})| = |H_0(e^{j\omega})|$$
$$\angle(e^{j\omega}) = \angle H_0(e^{j\omega}) - 0.5\omega - - - (2)$$

The selected DTCWT filter coefficients have to satisfy the properties such as delay property, perfect reconstruction, good vanishing moments and linear phase.

Design Method: The DTCWT consists of multiple stages of filtering that are made up of filter bands H0 and H1. In the proposed DTCWT architecture the filter bank structure shown in Figure 4 becomes the basic building block and hence the structure is modular.

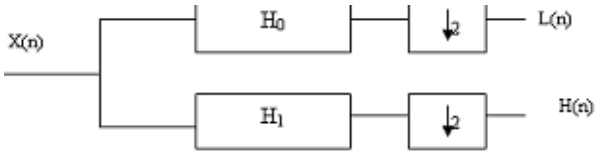

Fig: 4 Single stage dual trees CWT

By using the modified filter architecture a single stage modular unit is been designed to operate at high frequency, area and power optimizations. The proposed architecture is designed based on the symmetric property of filter coefficients, the filter bank output Y(n) for a given input signal x(n) can be expressed as in Eq. (11) and (12),

$$L(n) = \sum_{k=0}^{N-1} H_{0a}(K)\,X(n-K), \qquad n = 0,1,2,.....,N-1 \qquad \ldots \qquad (11)$$

$$H(n) = \sum_{k=0}^{N-1} H_{1a}(K)\,X(n-K), \qquad n = 0,1,2,.....,N-1 \qquad \ldots \qquad (12)$$

For $N = 18,\ n = 17,$ the above equations can be expressed as $L(17) = \sum_{K=0}^{17} H_{0a}(K)\,X(17-K)$ ... (13)

V. PROPOSED ARCHITECTRE

The proposed architecture is designed based on the symmetric property architecture consist of serial in serial out register (SISO), adder array and a multiplier array as shown in the figure 4.

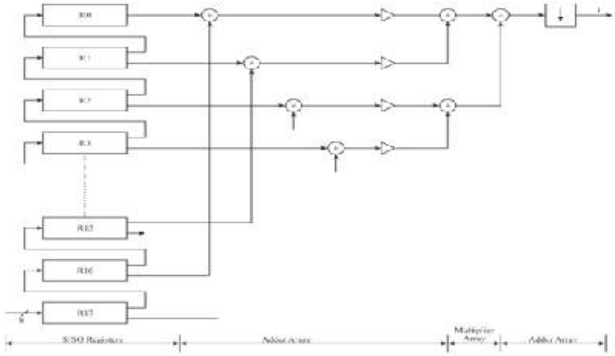

Fig: 5 Reduced DC DTCWT Architecture

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The SISO register is loaded with the input data serially from R17 to R0; this requires (17*3 bit) clock cycles after 51 clock cycles SISO register is designed to operate as SIPO register. At 52nd clock cycle the input data is processed by the adder array consisting of 8 adders, the bit size required to represent the adder output is 3 bits (1-bit for sign and 2-bit for magnitude). The output of adder array is 9 bit, the arithmetic operation has been designed such that overflow does not occur after accumulation. The arithmetic operations are designed to operate on 2's complement logic. With 51 clock cycles for loading data, and three clock cycles for addition, memory read and addition operation, the first sample is generated at the end of 54th clock cycle. During the last three clock cycles the architecture is designed to perform data load at the input SISO register and data path at the output stage. Thus a pipelined logic is designed for computation of modulated sub carries using inverse DTCWT. The proposed data path architecture stage 1 is represented in the figure 5.

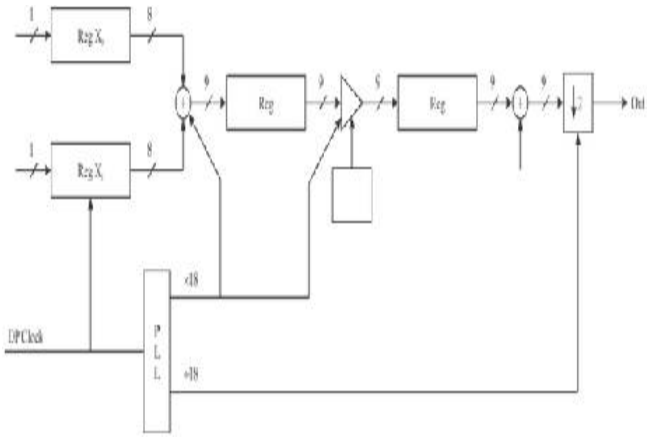

Fig 6: Data path logic for proposed architecture

The data path (DP) clock is the master clock for loading data, the PLL generates additional clock signals for control of adder, LUT, registers. The pipelined operation achieves latency of 54 clock cycles and throughput of 3 clock cycles. Computation of $H(n)$ is also carried out similarly and requires 54 clock cycles for computation of first output sample and another three clock cycle delay for computation of successive clock cycles. There are 11 filter coefficients for HPF, in order to match the LPF computation delay, the HPF filter coefficients are padded with zeros and the filter length is increased to 18. The data path logic for $H_{1a}(n)$ filter bank is also designed similarly. From the filter coefficients presented in table 1, $H_{0a}(n)$ is obtained from $H_{0a}(n)$ by Rotating by 2 samples. Similarly $H_{1b}(n)$ is obtained from $H_{1a}(n)$ by rotating by 2 samples. The filter equations for H_{0b} filter computation is as in equation 19.

$$K(n)=\sum_{K=0}^{N-1}H_{0b}(K)X(n-K), n=0,1,....,N-1 \qquad \ldots (19)$$

For $N=18,\ n=17$ $K(17)$ can be expressed as in equation 20.

$$K(17)=H_{0b}\left[X(17)+X(13)\right]+H_{0b}(1)\left[X(16)+X(14)\right]+H_{0b}(5)\left[X(12)+X(0)\right]+.....+H_{0b}(11)X(6)\ldots (20)$$

The symmetric property exists between $H_{0b}(0)$ t0 $H_{0b}(4)$ and $H_{0b}(5)$ to $H_{0b}(7)$. The filter coefficients for succeeding stages are also retained as that of first stage filter coefficients. The adders and multipliers used in above architecture will reduce the power consumption.

VI. IMPLEMENTATION

The concept of approximate arithmetic is used to develop various datapath components such as half adder, full adder, ripple carry adder & multiplier. Half Adder: In the proposed approximate based Full Half architecture, the half adder the sum path is approximated to only OR gate instead of XOR gate. Figure 7 a & b depicts the existing & proposed Half adder architectures.

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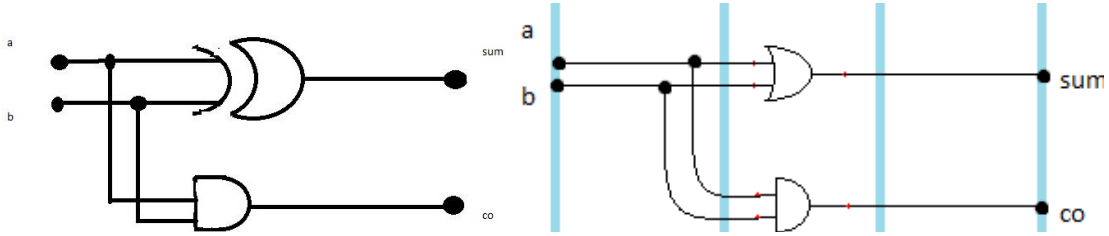

Figure 7a: Existing Half Adder Circuit

Figure 7b: Proposed Approximate Half Adder Circuit

Full Adder: In the proposed approximate based Full Adder architecture, the sum path of the full adder is approximated to a OR gate instead of XOR gate. This will result in both area & power reduction. Figure 8 a & b depicts the existing & proposed Full adder architectures.

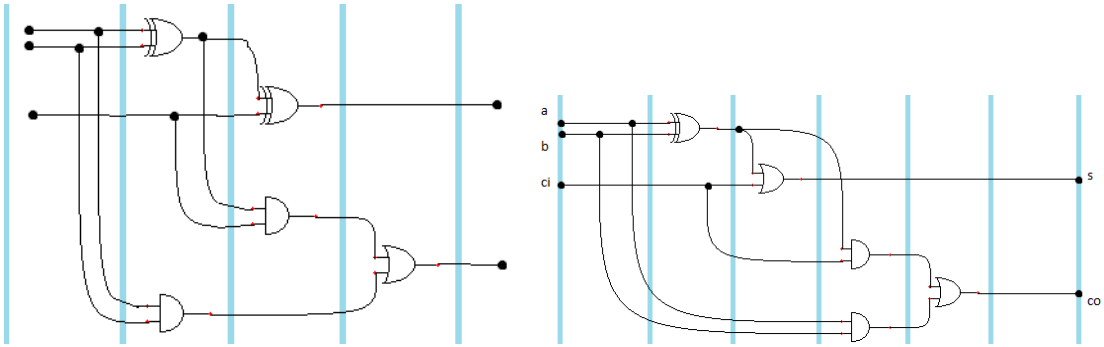

Figure 8a: Existing Full Adder Circuit

Figure 8b: Proposed Approximate Full Adder Circuit

Ripple Carry Adder: Both 8-bit & 9-bit ripple carry adders are implemented based upon the approximate full adders to optimize area & power.

Compressor: It is used in the multiplier to reduce the columns of partial products based on carry save concept. In the proposed approximate based compressor architecture, the compressor is built using two approximate full adders.

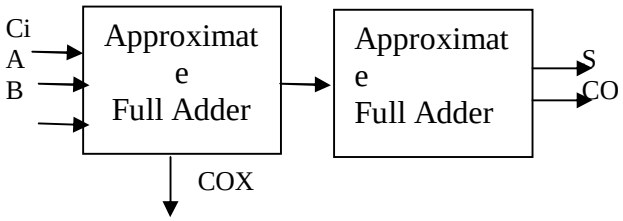

Figure 9: Proposed Approximate Compressor Architecture

Multiplier: The proposed multiplier is implemented based upon the approximate ripple carry adders. It is as depicted in figure 10.

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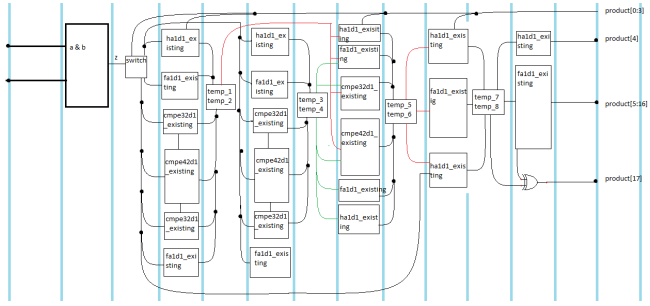

Figure 10: Proposed Approximate Compressor based Multiplier Architecture

The proposed approximate arithmetic concept is applied to the datapath logic architecture shown in figure 6. It consists of adder & multiplier as primary datapath components. Both the conventional and the proposed approximate architectures are designed and developed in gate level for synthesis, using the XIlinx ISE EDA tool. The designs were simulated using the Mentor Graphics Model-sim simulator and verified for functionality with the help of waveform editor. A standard FPGA design methodology was implemented to benchmark the results. The power analysis was performed using Xilinx XPOWER tool. The design is modelled using Verilog HDL, functionally verified using Modelsim & implemented using XILINX ISE. Power analysis is performed on the Post placed & routed netlist to get accurate results close to silicon values.

VII. RESULT AND DISCUSSION

Synthesis of the design is carried out using the Xilinx tool along with the post place, map and route simulation also have been carried out. The RTL simulation results are depicted in Figure 11.

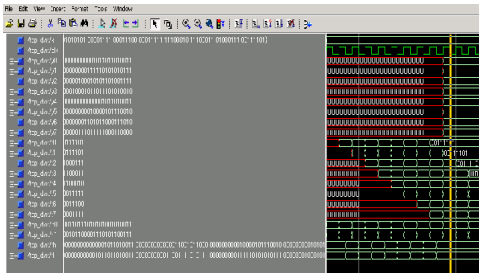

Figure 11: First stage simulation results of DTCWT processor using Modelsim.

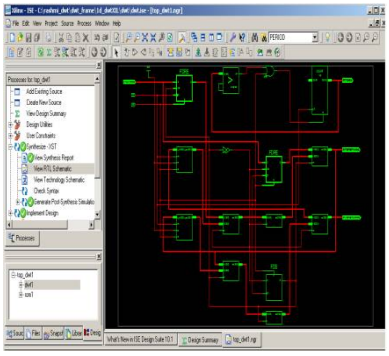

Figure 12: Synthesized netlist of DTCWT 'S snapshot

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The synthesized netlist of 1D DWT is shown in the Figure 12. This particular design is optimized for power, area and timing. RTL synthesized block diagram of DTCWT is obtained using the Xilinx ISE. The obtained results and synthesis report is analyzed for the estimation of the performance of proposed design is major parameters like area, power and timing. FPGA implementation of DWCWT s carried out and obtained results of DTCWT are tabulated in Table 1. From Table 1 it is proven that the proposed approximate arithmetic based architectures out performs the existing architecture in all the three corners of Area, Performance & Power corners. The area is reduced since we are using s smaller instead of larger gates (Ex OR instead of XOR). Since power is directly proportional to area, the power is also minimized in the proposed architecture.

Parameter	Existing	Proposed	%change
Area (BEL)	505	429	15
Delay (Nano Seconds)	8.719	6.762	22.9
Dynamic Power (Milli Watt)	28.28	25.95	8

Table 1: Implementation results of DTCWT

VI.CONCLUSION

This paper demonstrates the low power data path architectures for adder and multiplier. The novel approximate arithmetic architecture based DTCWT system is proposed & proven. The proposed architecture is designed with Xilinx ISE & mapped to Virtex7 device. The design is simulated using the Modelsim simulator.

In future, the proposed concepts & optimizations can explored at Transistor level of abstraction which will further improve the results.

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