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Low Power 4-Bit Ripple Carry Adder Design in 50nm Technology

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ABSTRACT: This paper presents the design of Ripple Carry Adder using modified-GDI technique. Modified- GDI technique is a new design technique that allows reducing power consumption, delay and area of digital circuit, while maintaining low complexity of logic design. The performance characteristics of M-GDI RCA are compared with GDI and traditional CMOS logic. The entire design has been performed in 50nm technology and the simulation of the proposed design has been carried out in LT spice tool.

KEYWORDS: M-GDI, Low power, Transistor count, RCA.

I.INTRODUCTION

In most of the VLSI application, arithmetic operations such as subtraction, multiplication, division are used. Which are based on addition. Adders are the basic building block for such operations. Thus the main objective is to improve the power consumption of adders. For this several techniques have been used. The main contribution of this paper presents the design of modified GDI cells. The modified GDI cells are designed and its parameters are compared with CMOS and GDI logic.

Static CMOS gates are slowed because an input must drive both NMOS and PMOS. CMOS logic style uses more no. of transistor which increases delay and area. GDI technique offer high speed, low power and less no. of transistor to implement the logic circuits. The main drawback of GDI technique is that it requires twin-well CMOS or silicon on Insulator process to realize a chip which increases the complexity as well as cost of fabrication. M-GDI technique offers less transistor count, reduced power consumption and delay. This technique is suitable for all types of circuit designing. In this paper 4-bit RCA has been designed using M-GDI technique, which reduces power more than that existing GDI and other traditional logic styles.

II.LITERATURE SURVEY

Authors [1] presented 4-input NAND gate using pseudo-NMOS logic gates, such type of designing can lead to decrease the area and input capacitance & no. of components has also reduced but its power dissipation is more and delays are also more as compared to conventional CMOS.

Authors [2] proposed 5 logic styles (SCMOS, pseudo NMOS, DCVSL, DCVSPG, PPCL) & compare their behaviour in the low region. The SCMOS had the best low voltage speed and power dissipation characteristics. In the process technology utilized for this analysis, the attractive point for circuit operation lies near 1.5v. in this voltage range, the propagation delay is approximately 3 times greater than with the nominal 3.3v supply voltage but the power dissipation is reduced by one order of magnitude.

Authors [3] compares three different logic styles for implementing arbitrary boolean functions of upto three input in terms of their layout area, delay and power dissipation. The three styles are NMOS pass transistor based design, NAND gate based design and CMOS complementary logic design. Result of the comparison shows that pass transistor based design is superior to NAND based design, but loses to CMOS complementary logic design.

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Authors [4] presented different implementation of a novel Gate Diffusion Input technique for low-power design. An 8-bit CLA adder was fabricated using GDI and CMOS. Measurements as well as simulation comparisons with PTL and CMOS techniques were carried out, showing an up to 45% reduction of power delay product in the test chip in GDI over CMOS and significant improvements in performance as well as decreased number of transistor in GDI circuit over CMOS and PTL.

Authors [5] presented various GDI techniques. In this paper basic building blocks of digital system are analysed and comparison are made based on complementary CMOS & GDI design techniques. The different methods are compared with respect to area, power dissipation & delay.

Authors [6] presented an enhanced GDI technique, namely the modified GDI for low power digital circuit design. Some important arithmetic modules and standard primitives have been realized using the traditional CMOS design style, GDI and m-GDI implementation styles. Comparing the present design methodology with CMOS realization logic and GDI design method, shows a minimization in power consumption by 54.97% and 47.8% respectively, while similar comparisons on the basis of transistor count shows a reduction by about 48.8% and 4.17% respectively.

Authors [7] designed logic gates, adders, multipliers based on four different logics and the results were compared. The four different logic styles are Gate Diffusion Input, CMOS, double pass transistor and transmission gate. It has been observed that GDI design style exhibit better characteristics as compared to other design style. Gate diffusion input design style can be considered to be the best logic design style with respect to parameter such as power and transistor count so gate diffusion input design style can be used in low power and high performance application.

Authors [8] consider various mixed full adder topologies and compare their performance. The proposed circuits have been tested in 0.18um CMOS technology. Based on the simulation results, the proposed design is 9% to 24% faster than the reported design topologies in term of worst case delay, consumes less power and more area efficient.

Authors [9] presented different adder circuits using MUX. The MUX are designed using three different techniques namely pass transistor, transmission gates and GDI. GDI technique results in maximum power saving almost 52% compared to pass transistor and 55% compared to transmission gate technique. Cadence 180nm was used to obtain the simulation results.

Authors [10] proposed the design of a full subtractor using Gate Diffusion Input procedure which simulation has been found to consume low power in conjuction with lesser delay time and fewer transistor while maintaining proper output voltage swing. Comparison with standard CMOS, transmission gate and CPL techniques showed a reduction of 72.00%, 63.16% and 58.82% in terms of transistor count, 99.68%, 88.78% and 99.99% in terms of average power consumption, 84.85%, 84.39% and 85.68% in terms of delay time respectively.

III.MODIFIED GATE DIFFUSION INPUT LOGIC STYLES

Power dissipation becomes most important restriction in high performance applications. Optimizations for basic logic gates are fundamental in order to get better the performance of a variety of low power and high performance devices. These limitations can be overcome by modified gate diffusion input (M-GDI) logic style. This technique allows reducing power consumption, delay and area of digital circuits.
The basic M-GDI cell consist 4 terminals – G (common gate input of NMOS and PMOS transistors), N (input to source of NMOS transistor), P (input to source of PMOS transistor) and OUT (output terminal). Bulk terminal of PMOS transistor connected to VDD and bulk terminal of NMOS transistor connected to GND. Fig 1 shows the basic MGDI cell-

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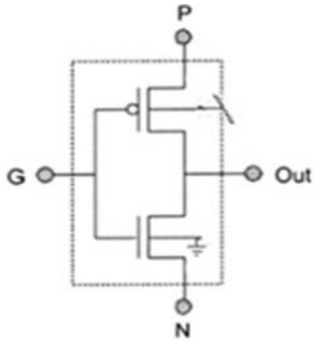

Fig. 1 M-GDI Cell

Table 1. Logic function implemented with MGDI technique

N	P	G	OUT	FUNCTION
0	B	A	A'B	F1
B	1	A	A'+B	F2
A	B	A	A+B	OR
B	A	A	AB	AND
B	A'	A	A'B'	NAND
A'	B	A	(A+B)'	NOR
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT
B	B'	A	A'B+AB'	XOR
B'	B	A	A'B'+AB	XNOR

IV.IMPLEMENTATION OF FULL ADDER AND RIPPLE CARRY ADDER

A ripple carry adder is chain circuit where carry output of one full adder is become the carry in signal of the consecutive full adder. So the carry at the input ripples through the each of the input to output. Implementation of RCA consist 4 full adders. Full adder is useful for addition that has multiple bits in each of its operand. It takes three inputs and creates two outputs, a sum and a carry out.

$$\text{sum} = (A \oplus B) \oplus C$$
$$\text{cout} = (A \oplus B)' \cdot A + (A \oplus B) \cdot C$$

1-Bit full adder using M-GDI: A 1-bit full adder is designed using CMOS, GDI and M-GDI Technique. 1-Bit full adder using CMOS technique contains 44 transistor and GDI and M-GDI Technique this circuit contains 18 transistors which contains 2-XOR gates and 1 multiplexer and buffers. The M-GDI technique suffers from low output swing so the full swing is achieved by adding buffers at the output. Figure shown is 1-bit full adder designed using buffers to increase the output swing.

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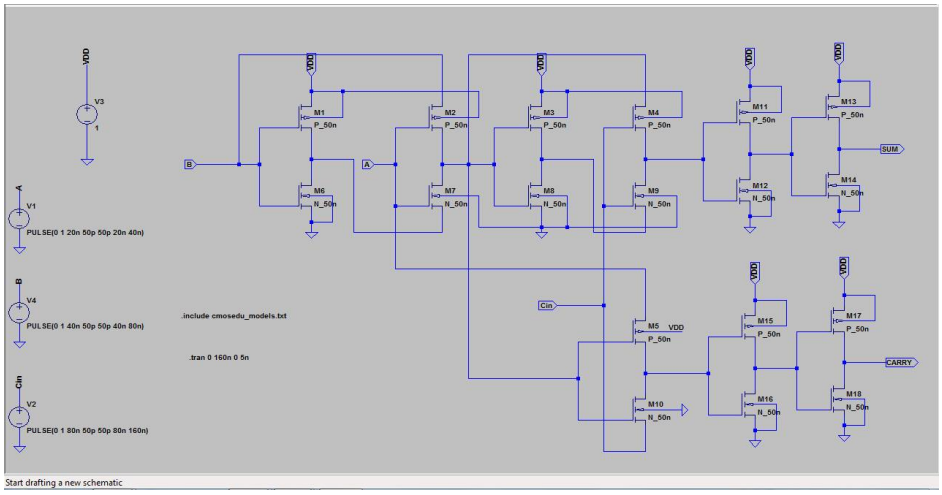

Fig. 2 Schematic Diagram of M-GDI Full Adder

4 bit Ripple Carry Adder: A 4-bit ripple carry adder is designed using 1 bit full adders. The ripple carry adder is having 4-bit input A [i] and B[i] where i vary from 0 to 3 and the sum output as sum[j] where j(=0…3)

$$Sum[j]=A[i]+B[i]$$

In the proposed methodology a 4-bit ripple carry adder will be designed using M-GDI technique. In which each of the 1-bit full adder will be designed using M-GDI technique.

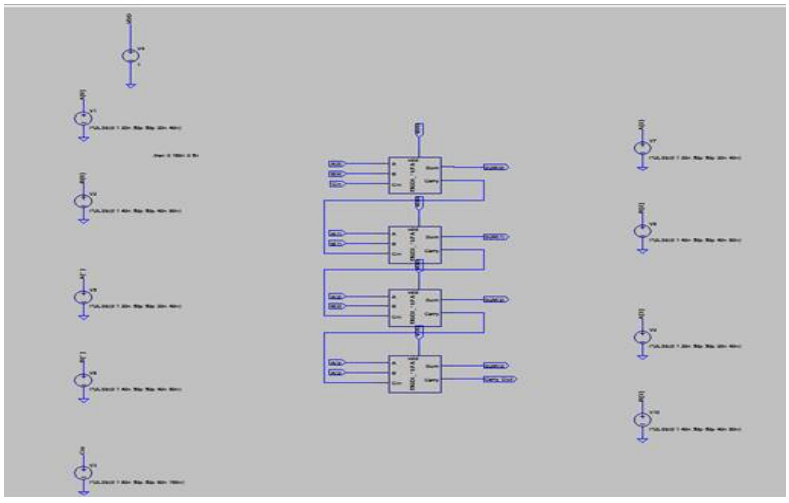

Fig. 3 Schematic Diagram of M- GDI 4-Bit RCA

V. SIMULATION AND RESULT

All the simulations are done in linear technologies LT Spice tool which is an industry standard fast and accurate tool. And the propagation delay is calculated according to 50% rise time of the input to 50 % fall time of the output. Tpd of the cells have been compared. The power consumption of the GDI and M-GDI cells are quite less compared to conventional complementary metal oxide FET's. All the input combinations are applied to get the desired output. The sizes of the transistors are calculated to equalize the rise and fall time of the output.

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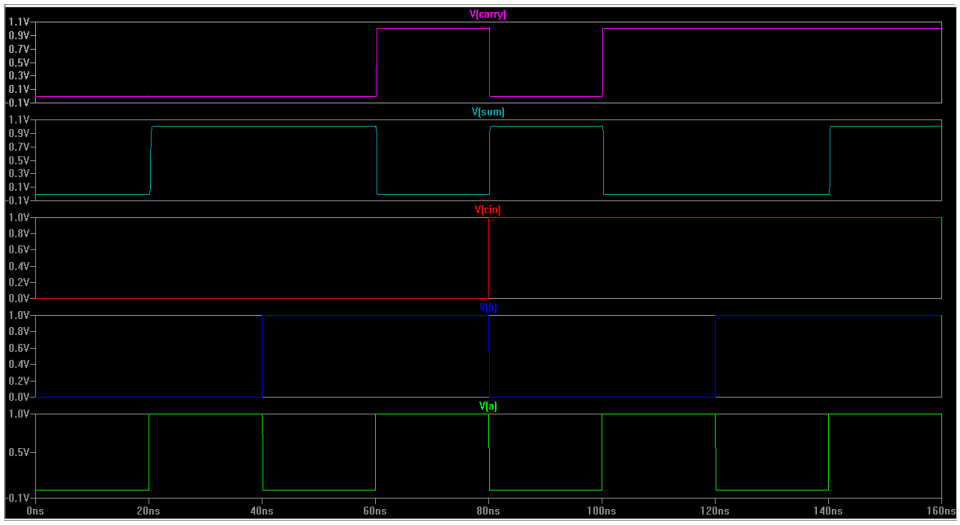

Fig. 4 Output Waveform of M-GDI Full Adder

Fig. 4 shows the output waveform of Full Adder. Here we applied all possible 8 combination of inputs to the full adder and corresponding sum and carry output are obtained.

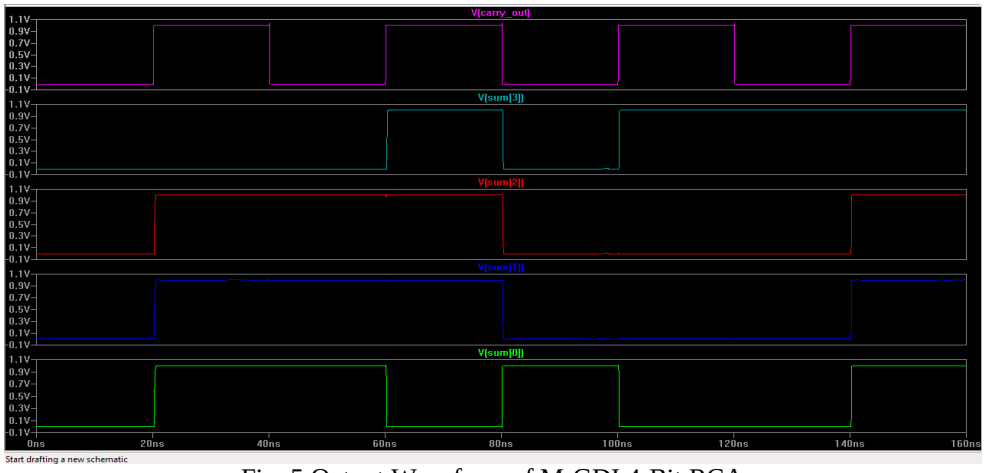

Fig. 5 Output Waveform of M-GDI 4-Bit RCA

Fig. 5 shows the output waveform of 4- bit RCA. Here the sum output of each block and final carry output are shown. The sum output of each block is given as carry input to next block.

Table 2. Technology Information

Technology	50nm
Power Supply	1 V
Operating frequency	12.5 MHz

Table 2 shows the some information about technology, power supply operating frequency. All the simulations are done in 50nm technology at 1V power supply and 12.5MHz frequency.

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Table 3. Comparison of Transistor Count, power and propagation delays have been shown

Logic Design	Transistor Count	Power	Delay(Tpd)
4-bit CMOS RCA	176	236 nW	0.38 ns
4-bit GDI RCA	72	89 nW	0.087 ns
4-bit M-GDI RCA	72	83 nW	0.079ns

Above results shows that the transistor count drastically reduces which consumes very less area with its CMOS counterpart, And results also shows reduced power and delay compared to its CMOS counterparts. M-GDI 1-bit Full adders have buffers at the output to provide a full rail to rail swing

VI.CONCLUSION

In this paper 4-bit ripple carry adder has been designed by using M-GDI Technique. The performance of the circuit shows a large difference in conventional CMOS circuits and the modified gate diffusion techniques. The modified GDI techniques uses less no. of transistors compared to their CMOS counterpart. 1-bit Full adders have been designed using the basic M-GDI based AND OR and XOR gates. A ripple carry adder is chain circuit where carry output of one full adder is become the carry in signal of the consecutive full adder. So the carry at the input ripples through the each of the input to output, which shows that the GDI logic style consumes lesser power compared to static CMOS logic. The operating voltage of the circuit is 1V. All the designs have been simulated in 50nm technology.

REFERENCES

[1] R.MEHRA & A. VERMA (Apr 2013) “Design And Analysis Of Conventional And RatioedCMOS Logic Circuit”, IOSR Journal Of VLSI And Signal Processing, Vol.2, Issue 2, Mar-Apr 2013, PP 25-29.
[2] M. KONTIALA, M.KUULUSA & J NURAMI (2001) “Comparison Of Static Logic Styles For Low Voltage Digital Design”, 8th IEEE International Conference On Electronics Circuit & System.
[3] M.PEDRAM, R.MEHROTRA & XUNWEI WU (Oct 1997) “Comparison Between Nmos Pass Transistor Logic Style vs. CMOS Complementary Cells” , IEEE International Conference On Computer Design: VLSI In Computer & Processor.
[4] A.MORGENSHTEIN,A.FISH & WAGNER (2002) “GDI- A Technique For Low Power Design Of Digital Circuit: Analysis And Characterization”, IEEE International Symposium On Circuit & System.
[5] P.VERMA & R.MANCHANDA (2014) “Review of Various GDI Technique for Low Power Digital Circuit”, International Journal of Emerging Technology & Advanced Engineering, Vol. 4, Issue 2, Feb 2014.
[6] P.BALASUBRAMANIUN & J.JOHN (Sep 2006) “Low Power Digital Design Using Modified GDI Method”, IEEE International Conference On Design & Test Of Integrated System In Nanoscale Technology.
[7] SHOFIA RAM & R.R. AHAMED (July 2013) “Comparison And Analysis Of Combinational Circuit Using Different Logic Styles”, 4th International Conference On Computing, Communication & Networking Technologies.
[8] A.K. AGRAWAL, S. MISHRA, R.K. NAGARIA (Dec 2010) “Proposing A Novel Low-Power High-Speed Mixed GDI Full Adder Topology”, IEEE International Conference On Control & Embedded System.
[9] S.HIREMATH & D,KOPPAD (Oct 2012) “Low Power Full Adder Circuit Using Gate Diffusion Input Mux”, 4th International Conference On Control & Embedded System.
[10] K.DHAR, A.CHATTERGEE, S.CHATTERGEE (2014) “Design Of An Energy Efficient, High Speed, Low Power Full Subtractor Using GDI Technique”, IEEE Conference On Technology Symposium.