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Design of a CMOS Comparator using 0.18um Technology

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ABSTRACT: The comparator is a critical part of almost all kind of analog-to-digital (ADC) converters. Depending on the type and architecture of the comparator, the comparator can have significant impact on the performance of the target application. This work represents a two stage open loop comparator which uses a differential topology with current mirror load and this circuit helps achieve low power dissipation of 0.23958uW along with a low propagation delay of 2.1468ns which is giving a unity gain bandwidth of 35.714Mhz. Apart from two stage CMOS comparator design, single stage comparator designs have also been discussed. Analysis such as DC, AC and transient have been performed to calculate values of parameters such as gain ,unity gain bandwidth , power and propagation delay. The schematic has been made using S-edit while the netlist was being created using T-spice and results were viewed using W-edit tool.

KEYWORDS: CMOS comparator, low Power, low Propagation delay

I. INTRODUCTION

A comparator is a circuit that compares the two analog input signals and decodes the difference into a single digital output signal. Figure 1 below shows the comparator symbol, where output is the single digital output as a result of comparison of two analog inputs Vin+ and Vin-.

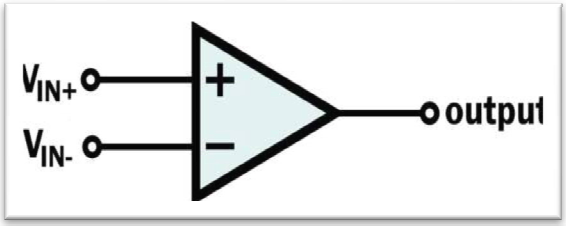

Figure 1: Comparator Symbol

$$\mathbf{Voutput} = \begin{cases} \mathbf{1}, \mathbf{if\ Vin+ > Vin-} \\ \mathbf{0}, \mathbf{if\ Vin+ < Vin-} \end{cases}$$

Many applications, such as analog to digital converters (ADCs), memory sensing circuits and recently also on chip transceivers are widely using comparators [1]. In the last years, most of the researches focus on the comparator with low power consumption, simple thermal management and high efficiency. The growth of the portable electronic devices makes the power consumption is critical issue to circuit designers because the low power and high speed comparators are the main building block in the front end of the radio frequency receiver in the most of the modern telecommunications system [2].

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The speed and resolution of an ADC is directly affected by the comparator input offset voltage, the delay and input signal range [4]. Depending on the nature, functionality and inputs, comparators are classified into different types i.e. voltage and current comparators, continuous and discrete time comparators etc. Some basic applications of comparators are analog-to-digital conversion, function generation, signal detection and neural networks etc.
This paper represents the work done in a proper sequence. Part I describes the introduction. Part II describes the CMOS comparator and its working and also describes the various methodologies used in this work such as common source amplifier with resistive load , a basic single stage comparator having current mirror as load using differential topology, then a latch topology has been implemented using cross coupled load and finally a two stage open loop comparator having differential topology and current mirror load has been presented which gives a low power dissipation along with low propagation delay. Part III discusses the simulation and result. Part IV concludes this work.

II.CMOS COMPARATOR & METHODOLOGIES USED

A. Op-amp Voltage Comparator:

An operational amplifier (op-amp) has a well balanced difference input and a very high gain. This parallels the characteristics of comparators and can be substituted in applications with low-performance requirements [3]. In theory, a standard op-amp operating in open-loop configuration (without negative feedback) may be used as a low-performance comparator. When the non-inverting input (V+) is at a higher voltage than the inverting input (V-), the high gain of the op-amp causes the output to saturate at the highest positive voltage it can output. When the non-inverting input (V+) drops below the inverting input (V-), the output saturates at the most negative voltage it can output. The op-amp's output voltage is limited by the supply voltage. An op-amp operating in a linear mode with negative feedback, using a balanced, split-voltage power supply, (powered by $\pm V_S$) has its transfer function typically written as: $V_{out}=A_o(V_1-V_2)$. However, this equation may not be applicable to a comparator circuit which is non-linear and operates open-loop (no negative feedback).

B.Methodologies Used:

Various design approaches have been used in this work. All the schematic designs have been made using S-edit tool of tanner EDA.
First a common source amplifier was implemented and its parameters have been calculated like gain , transconductance , bandwidth and power by performing various analysis like ac, dc and transient.
Second a single stage comparator was designed and its power , bandwidth and delay have been calculated .Third again a single stage comparator using another design approach has been implemented and its power, gain bandwidth and delay have been calculated. Finally a two stage comparator has been implemented and its gain bandwidth, power and delay have been calculated.
The figure 3 below shows a simple common source amplifier with a resistive load.

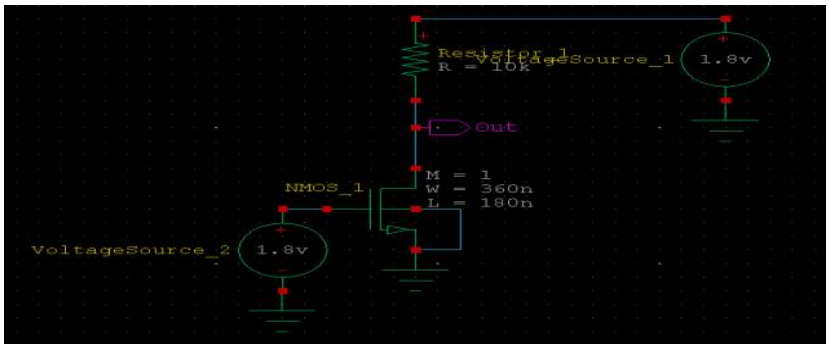

Figure 2 :CS with Resistive load

Here 180 nm technology has been used to carry out the simulation using T-spice. The voltage supply was 1.8v and value of resistor was 10K , width and length of the NMOS used were 360n and 180nm respectively. Here initially when the input voltage is low then NMOS_1 is in cutoff state and the output is 1.8v. as the input voltage starts to increase the

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transistor first goes in the saturation region and then in the active region and the output decreases accordingly. This design offered a high bandwidth.

Another topology uses a current mirror load which is shown below in Figure 4. Here technology used is 180nm.Bias voltage was calculated to be 0.5245volts .Width and length of the transistors used are 240n and 180nm respectively. Power supply of 1.8 volts was applied. This topology gives a low power consumption with a lower delay and a large bandwidth.

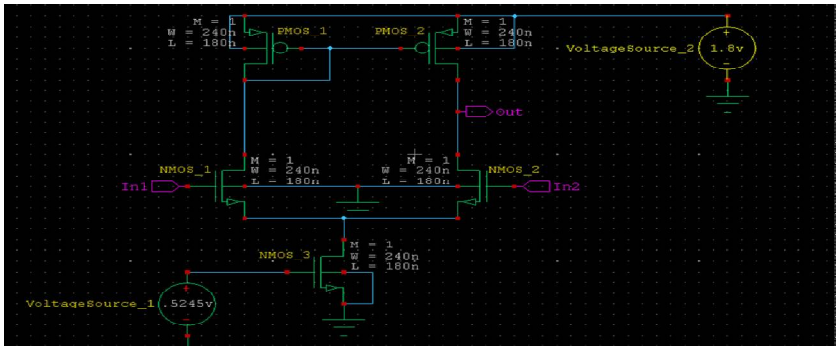

Figure 3: Current Mirror Topology of a single stage CMOS comparator

Then another topology shown in figure 5 was implemented using PMOS cross coupled load forming a latch topology with a bias voltage of 0.5245volts and a power supply of 1.8 volts. Width and length of the transistors used are 240n and 180nm respectively. This design has comparatively more delay than the previous one shown in figure .The bandwidth was also further reduced. So in the further design process current mirror topology (figure 3) has been used.

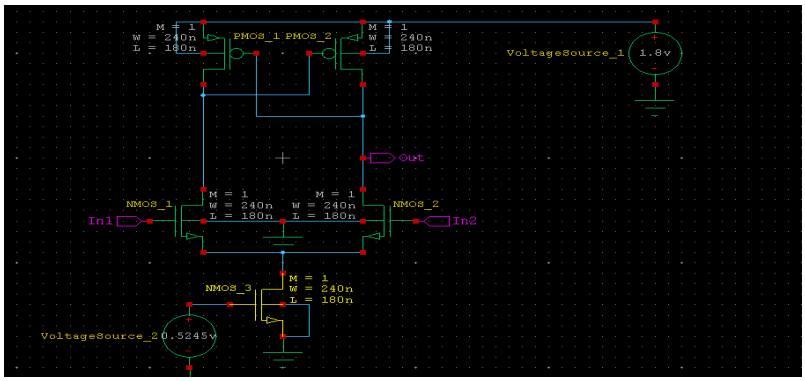

Figure 4: Cross Coupled Design of a single stage CMOS comparator

The Figure 5 below shows the final design of a two stage comparator design with open loop configuration with total 7 transistors in use. For second stage the aspect ratio of PMOS is twice to that of first stage. The bias voltage used is 0.616volts considering a current flow of 1uA in the circuit.

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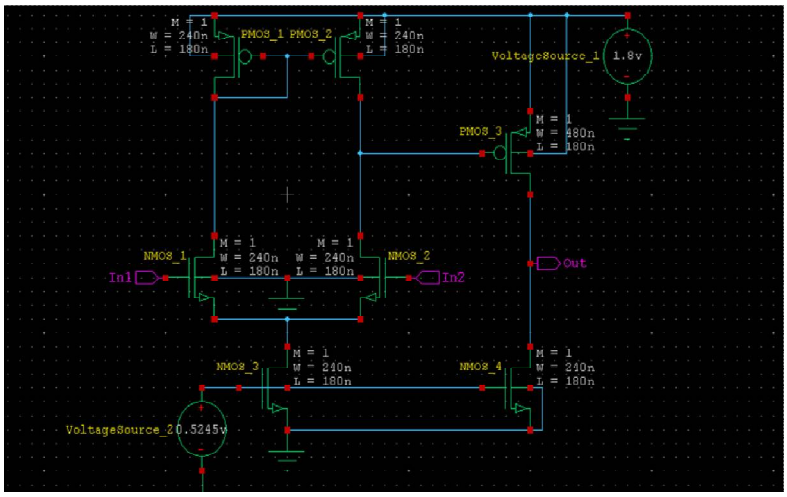

Figure 5: Two Stage CMOS Comparator

Here transistors M1,M2,M3,M4 form the first stage which is the differential gain stage and transistors M6 and M7 form the second stage which is the gain stage. In the first stage, transistor M5 provides the biasing to entire circuit, transistors M1 and M2 form the differential input pair actively loaded by a current mirror pair formed by transistors M3 and M4. In the second stage, transistor M6 is a common source amplifier actively loaded by transistor M7.
This design has comparatively lower power consumption along with a lower propagation delay.

III.SIMULATION RESULTS

All the results have been simulated in 180nm technology. Lower power consumption and lower delay hence more speed are the most useful part of this design.
In this work, AC analysis ,DC analysis and transient analysis have been performed to find values of various parameters such as unity gain bandwidth , power, delay .

A. Analysis of common source amplifier with resistive load:

In this part, DC and Ac analysis of a common source amplifier with resistive load have been done using 180nm technology.

The Figure 6 below shows the DC analysis of a common source amplifier whose schematic has already been shown in Figure3. The values deduced for the parameters such as gain and transconductance have been shown in the Table 1 below.

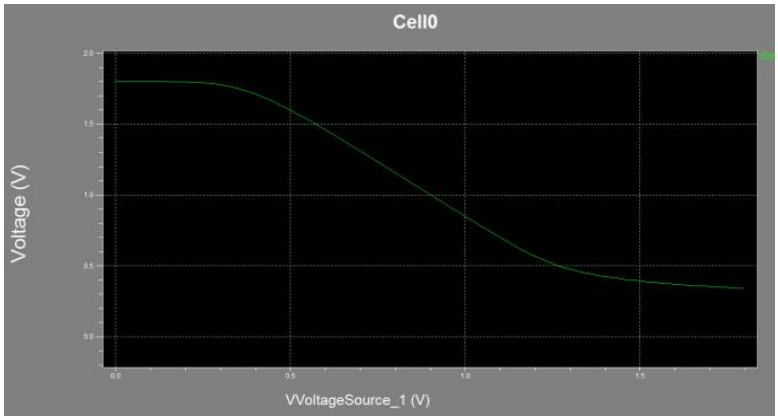

Figure 6: DC analysis of CS amplifier

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The figure 7 below shows the AC analysis of CS amplifier in 180nm technology. Here sine wave was given as the input of CS amplifier with peak value of 1.8 at a frequency of 50GHz.
The unity gain bandwidth was found using the voltage magnitude curve where it cuts the X- axis. The values deduced for the parameters has been shown in the Table 1 below.

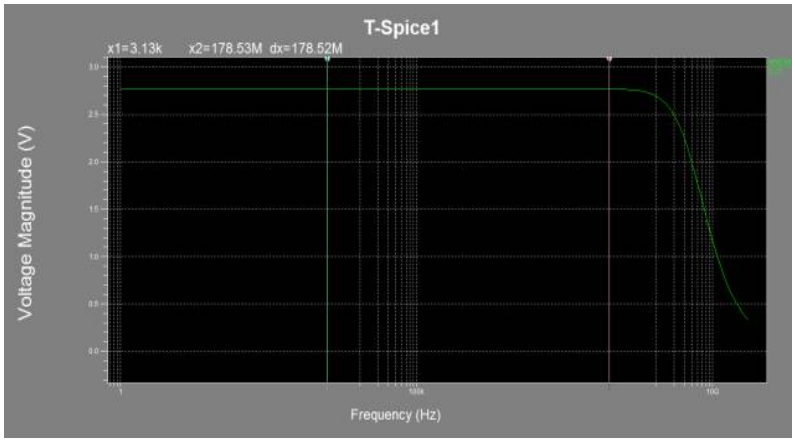

Figure 7: Ac analysis of CS amplifier

Output results:
The Table 1 below shows the parameter values achieved upon DC analysis and AC analysis in 180nm technology for a common source amplifier with resistive load. Upon Dc analysis values of gain and transconductance, g_m, were found and by performing AC analysis values of parameters such as unity gain bandwidth delay and power were found.

Table 1: Parameter values achieved for CS amplifier

Parameter	**Value**
Gain	3.6
Transconductance	3.645*10^3 mho
Delay	0.46794 nsec
Bandwidth	178.53MHz
power	0.547749 nwatts

B. Analysis of Single Stage CMOS Comparator:
In this part, transient and Ac analysis of a single stage CMOS comparator have been done using 180nm technology whose schematic has already been shown in Figure 4.
The Figure 8 below shows the transient analysis of single stage design with current mirror topology. Here the delay and power were found. Delay was calculated between first falling edge of input and first rising edge of output. The values deduced for the parameters has been shown in the Table 2 below.

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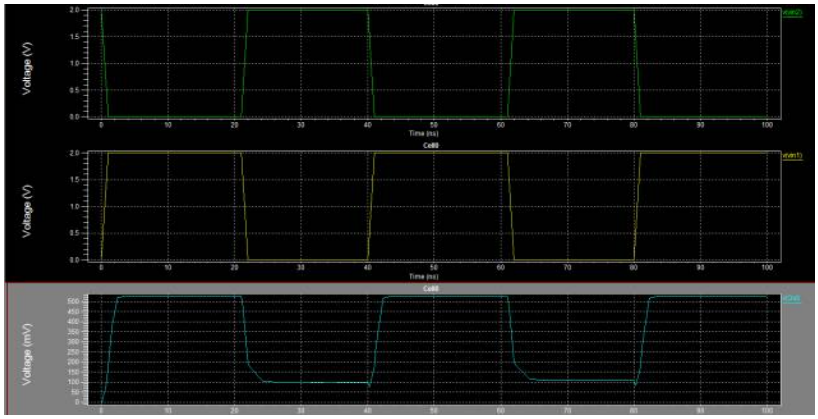

Figure 8: Transient analysis of Single Stage

The Figure 9 below shows the AC analysis of single stage design with current mirror topology. Here sine waves were given as the inputs of comparator with peak value of 1.8 at a frequency of 50Ghz. The values deduced for the parameters have been shown in the Table 2 below.

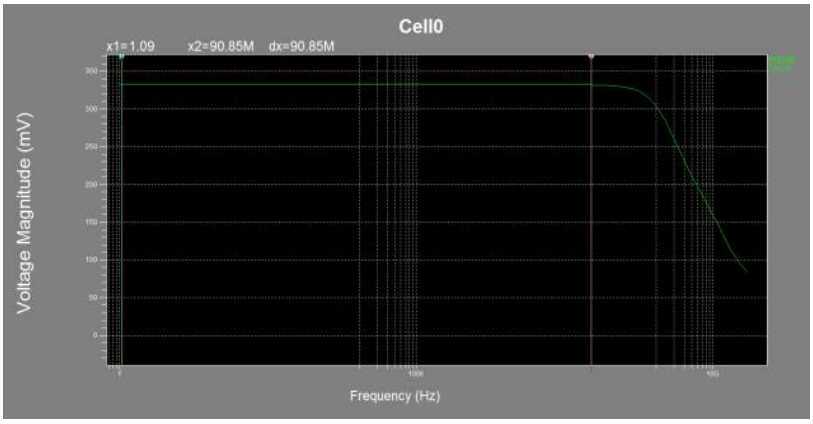

Figure 9: AC analysis of Single Stage

Output results:
The Table 2 below shows the parameter values achieved upon transient analysis and AC analysis in 180nm technology for a single stage CMOS comparator using current mirror topology. Upon transient analysis, values of delay and power, were found and by performing AC analysis values of unity gain bandwidth was found.

Table 2: Parameter values achieved for single stage CMOS comparator

Parameter	**Value**
Delay	0.34882 ns
Bandwidth	90.85Mhz
Power	0.0551768 nwatts

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C. Analysis of a Two Stage CMOS Comparator:

In this part, transient and Ac analysis of a two stage CMOS comparator have been done using 180nm technology whose schematic has been shown in Figure 6.

The Figure 9 below shows the transient analysis of two stage design with current mirror topology. Here the delay and power were found. Delay was calculated between first falling edge of input and first rising edge of output. The values deduced for the parameters has been shown in the Table 3 below.

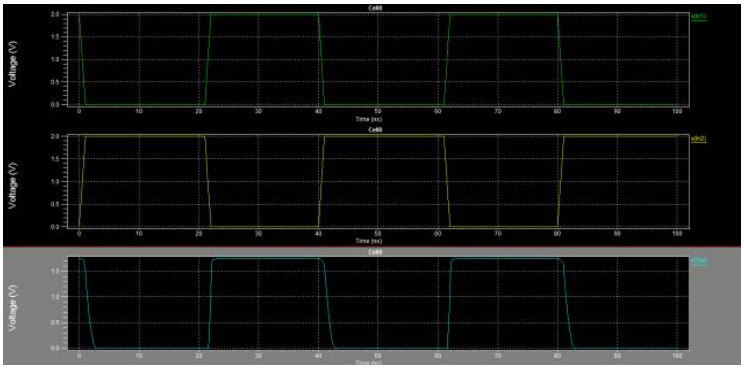

Figure 10: Transient Analysis of a two stage CMOS comparator

The Figure 11 below shows the AC analysis of two stage design with curren mirror topology. Here sine waves were given as the inputs of comparator with peak value of 1.8 at a frequency of 50Ghz. The values deduced for the parameters has been shown in the Table 1 below.

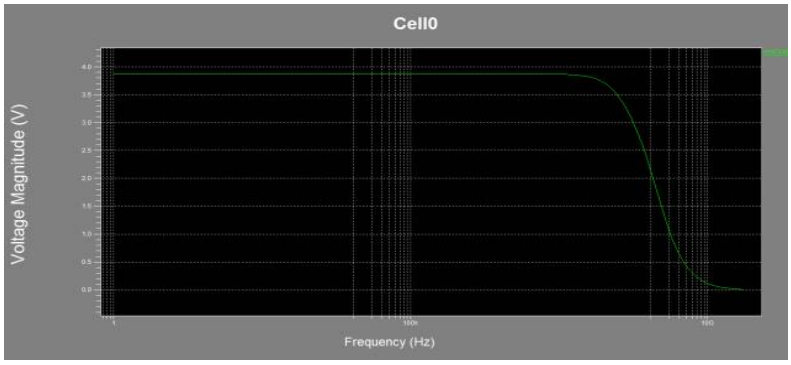

Figure 11: AC analysis of a two stage CMOS comparator

Output results:

The Table 3 below shows the parameter values achieved upon transient analysis and AC analysis in 180nm technology for a two stage CMOS comparator using current mirror topology. Upon transient analysis values of delay and power, were found and by performing AC analysis values of unity gain bandwidth was found.

Table 3: Parameter values achieved for a two stage CMOS comparator

Parameter	**Value**
Delay	2.1468 ns
Bandwidth	35.714MHz
Power	0.239581 nwatts

The Table 4 below gives a comparative analysis for all the approaches used in this work such as, CMOS comparator with single stage and two stage topologies respectively.

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From the table 4 it can be clearly seen that the power dissipated and delay is least in single stage design for CMOS comparator..

Table 4:Comparative Analysis of parameters for various approaches used

Approach used	Delay	Bandwidth	Power
Single stage	0.3488ns	90.85Mhz	0.05517 nW
Two stage comparator	2.1468ns	35.714MHz	0.23958 uW

IV.CONCLUSION

In this work, CMOS comparator has been implemented using T-Spice which is giving a low delay of 2.14ns along with a low power dissipation of 0.23958 u-watts. Also the comparative analysis for various methodologies such as CS amplifier with resistive load, single stage topologies of a CMOS comparator have been discussed which give bandwidth as high as 178.53 MHz and power as low as 0.05nwatts.The two stage CMOS comparator design implemented here gives low power dissipation but at the cost of a lower bandwidth of 35.714MHz so this design can be further modified to achieve a higher gain bandwidth which is an important characteristics of a comparator.

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