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Implementation of Low Power Inverter using Adiabatic Logic

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ABSTRACT: Adiabatic logic is low power logic, based on charge recovery principle. In this paper an Adiabatic logic based inverter are designed on the basis of Positive Feedback Adiabatic Logic (PFAL) and Two Phase Adiabatic Static Clocked Logic (2PASCL). We have proposed Adiabatic logic inverter circuit, and the power dissipation of proposed technique is compared with 2PASCL and PFAL technique according to the various values of input signal switching frequencies. The proposed circuit show lesser power consumption then the Positive Feedback Adiabatic Logic (PFAL) technique. Adiabatic logic is a low power circuit, which is a reversible logic and it is used to conserve energy. All design is to be simulated using TANNER EDA tool V15.0 simulation will be done at BSIM4 90nm technology.

KEYWORDS: Adiabatic technique, 2PASCL, PFAL, power saving, BSIM4, TANNER EDA V15.0

I.INTRODUCTION

The Demand of low power consumption in portable applications are highly important. The increased functionality of portable systems require lot of power which require high Hours of batteries. This demand is increase the size of the batteries. Another way to reduce power is to implement the circuit with power efficiency. In recent year variety of techniques and technologies have been developed, including the use of near- threshold and sub- threshold logic. Adiabatic logic is also known as reversible logic technique. It has also been reasoned an attractive low power alternative to standard CMOS logic circuits [1].Recently ultra low power system has attracted. Many researcher's interested into the growth of naturally and technically accepted low power VLSI design methodologies. In conventional CMOS circuit with the help of reducing the supply voltage, node capacitance and switching activity we have minimize the power consumption, but recently Adiabatic computing has been implemented in low power systems very successfully [2].

The term Adiabatic is taken from Greek word "impassable" and frequently used in thermodynamics, which means that there is neither loss nor gain of energy [4]. Adiabatic logic control by an AC power supply and it works with the concept of switching which is used to reduce energy dissipated by resistive heating of components and by allowing charge recovery [1].Efficient charge recovery logic (ECRL), positive feedback adiabatic logic (PFAL), two phase adiabatic static clocked logic (2PASCL), 2N2N2P logic etc. all these are families of adiabatic logic, which have been developed in recent years.

This paper proposes implementation of an inverter with standard CMOS, PFAL and 2PASCL based circuit and compared all these logic, and we found that proposed technique is more efficient in power saving than above other techniques.

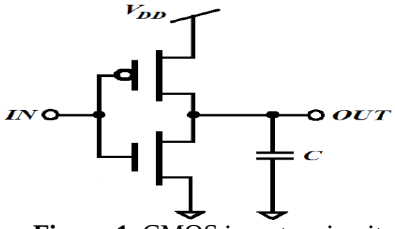

Figure 1. CMOS inverter circuit

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II.LITERATURE SURVEY

Author [1] present a 16-bit logarithmic signal processor and its implementation using Clocked Adiabatic Logic (CAL), to build hybrid logarithmic signal processor. The circuit is design using AMS 0.35µm CMOS process, circuit verified by the Spice simulator at frequency 250MHZ.
Author [2] simulated an energy efficient adiabatic logic technique using 0.18µm SPICE technology with two phase clocked scheme with operating frequency of 10 to 150 MHZ and observed that the inverter power dissipation was about 12% of the static CMOS inverter power dissipation.
Author [3] describe Adiabatic Logic in brief. The circuit designed and compared by adiabatic logic and CMOS logic. After comparison we have seen the fact that circuits get smaller and faster. Adiabatic logic is also known as reversible logic.
Author [4] has design and implement low power 4:1 Multiplexer using adiabatic logic the power dissipation of various Adiabatic circuits calculated and the circuit is simulated by T-SPICE tool.
Author [5] describes principles of CMOS VLSI design. The incredible growth comes from steady. For minimization of transistors and improvement in manufacturing process we have use Adiabatic logic.
Author [6] demonstrate adiabatic logic based low power Multiplexer and de-multiplexer, using the NI- Multisim software at 0.5µm CMOS technology for frequency range 200MHZ - 800MHZ. Proposed logic for the multiplexer have less energy requirement. Less area and transistor count then the other logic styles, the percentage power saving of 44.96% over PFAL, 60.39% over ECRL and 69.56% over 2N2N2P logic. Similarly in de-multiplexer the percentage power saving compared to the proposed logic is 27.66% over PFAL, 45.74% over 2N2N2P and 53.96% over ECRL.
Author [7] simulated the power saving analysis of adiabatic logic in sub-threshold region. The simulation is carried out by using the BSIM3v3 model at 0.18µm technology. Apply the sub-threshold device parameter and show that the energy dissipation of proposed 2PC2AL is the smallest then the 2N2N2P, CAL, ECRL, PAL, PECRL, PFAL, SAL logic family in the frequency range from 10KHZ to 10MHZ.
Author [8] demonstrated adiabatic logic based power efficient code converters, using the NI- Multisim software at 0.18µm, 1.8V CMOS standard process technology over a frequency range of 200-800MHZ. Proposed logic for the converter have less energy requirement. Less area and transistor count then the other logic styles. The percentage power saving of 2PASCL for BCD to Excess-3 is 41.95%, and for Gray to Binary converter is 31.19%.
Author [9] has design clocked CMOS adiabatic logic (CCAL) with low power dissipation, to demonstrate the performance and energy efficiency, eight inverter chain was implemented by CCAL, Using the Rohm 0.18µm process. Operation frequency can reach 500MH, below 100MHz CCAL eight-inverter chain always has lower power dissipation then the QSERL. CCAL eight-inverter chain saves about 40% energy at 200MHz

III.CMOS LOGIC

In CMOS inverter the drain of PMOS and NMOS is connected to the output and the gate terminal of both devices are connected to the input. The source terminal of the PMOS is connected to the supply voltage, and the NMOS is connected to the ground [5]. The CMOS inverter is shown in Figure 1.
Power dissipation in conventional CMOS circuit consumes due to device switching. When the input is low that time PMOS is ON and NMOS is OFF. Hence, direct path exist between supply voltage and output load capacitance. This stage is called charging stage [2].

$$E_{charge} = (1/2)\, C_L\, V_{dd}^2 \qquad (1)$$

If input is high that means '1' that time PMOS is OFF and NMOS is ON. So, there is no direct path between supply voltage and output load capacitance. This stage is called charging stage. That time charged output load capacitance will be discharge continuously [6].

$$E_{discharge} = (1/2)\, C_L\, V_{dd}^2 \qquad (2)$$

The total amount of energy dissipated during charging and discharging is given by:

$$E = E_{charge} + E_{discharg} = C_L\, V_{dd}^2 \qquad (3)$$

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IV.ADIABATIC LOGIC

In charging process of Adiabatic logic capacitor 'C' is in series with resistance 'R' and using constant current supply for charging the load capacitor [7]. In starting the voltage beyond capacitor will be zero. 'R' is the resistance of PMOS device in the pull up network, 'C' is the capacitor and V_c is voltage across capacitor is shown in Fig.2.
The charge of capacitor at time T is given by

$$Q = C\, V_C\,(t) \qquad (4)$$

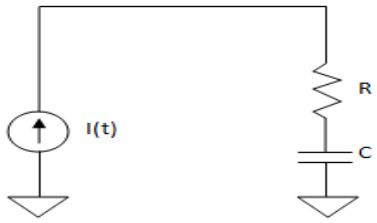

Figure 2. Adiabatic Logic circuit

Suppose that current is constant during the time period '0' to 'T'. So, the energy dissipation is given by

$$E_{dissipation} = R\, I^2(t)\, dt \qquad (5)$$

$$= R\, I^2(t)\, T \qquad (6)$$

We know that the constant current is : I(t) = Q / T , From equation (4)

$$I(t) = CV / T \qquad (7)$$

Put the value of I(t) from equation (7) to equation :

$$E_{dissipation} = R\,(CV/T)^2\, T$$

$$= (RC/T)\, CV^2 \qquad (8)$$

Where $E_{dissipation}$ is the total energy dissipate during the charging period.

A. PFAL

Positive Feedback Adiabatic Logic (PFAL) is also named as partial energy recovery circuit structure. PFAL has good lustiness against the technological parameter variations. PFAL is a dual rail circuit; adiabatic amplifier is the main part of all PFAL circuit. In this latch is used, and the latch is built by two NMOS and two PMOS transistors. The latch is ignoring logic level degradation on the output nodes. Fig.3 depicts the PFAL based inverter [3]-[4].

From Fig.3 the latch is made by two PMOS_1, PMOS_2 and two NMOS_3, NMOS_4, which is avoid a logic level degradation on the output nodes out and out1. There is two NMOS transistors NMOS_1 and NMOS_2 recognize the logic function. This logic family will be generating positive and negative outputs.

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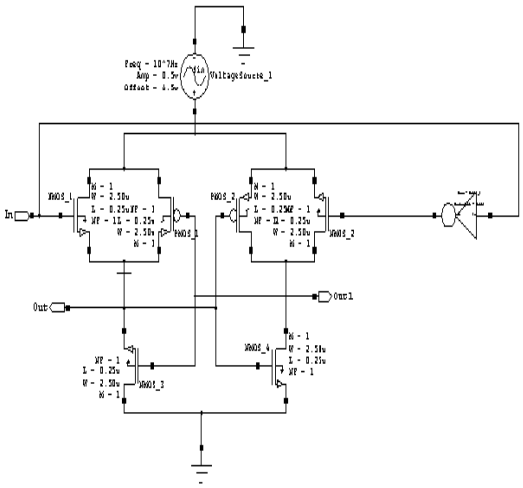

Figure 3. PFAL based Inverter

B. 2PASCL

Fig.4 shows circuit diagram of Two- Phase Adiabatic Static Clocked Logic (2PASCL) inverter. 2PASCL inverter is consist of two sinusoidal power supplies, these supplies are called power clock. In this one clock is in phase while the second clock is inverted, and the both power clock will be replace the constant power supply.

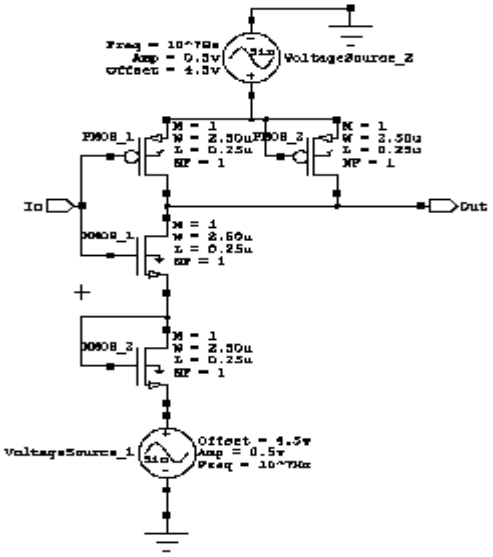

Figure 4. 2PASCL based Inverter

In 2PASCL inverter, when input voltage is low that time PMOS transistor which is connected to the input is ON and NMOS transistor is OFF, which is charge the output capacitor according to the magnitude of power clock. Whereas, if input voltage is high then NMOS transistor is ON and PMOS transistor is OFF which is connected to input. Basically 'evaluation' and 'hold' are two main steps of the circuit operation [8]-[9].

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V. PROPOSED ADIABATIC LOGIC INVERTER

The proposed Adiabatic logic inverter circuit is shown in Fig.5. An Adiabatic amplifier is the core of this proposed circuit. The latch is made by two PMOS_1 and PMOS_2, and two NMOS_3 and NMOS_4. The logic circuit NMOS_1 and NMOS_2 are in parallel with PMOS_1 and PMOS_2 respectively, and forms transmission gate. This circuit use two phase split level sinusoidal power supply which is donated as voltage source_1 (V_s_1) and voltage source_4 (V_s_4).

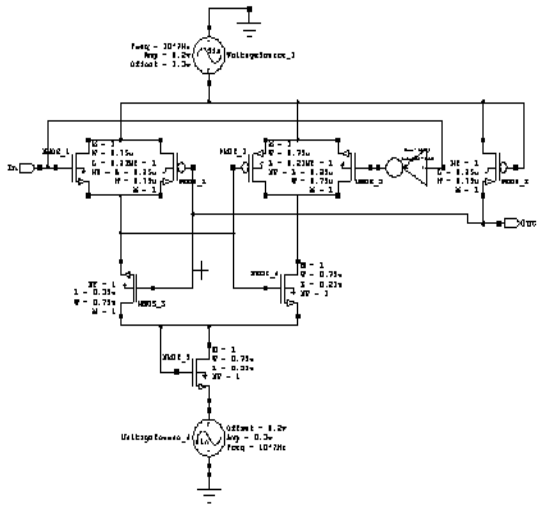

Figure 5. Proposed Adiabatic Logic Inverter

Basically 'evaluation' and 'hold' are two main steps of the circuit operation. In evaluation phase V_s_1 swings up and V_s_4 swings down, and in hold phase V_s_4 swings up and V_s_1 swings down.
Assume that during at evaluation phase the input (in) is high and input (/in) goes low, that time NMOS_1 is conducting and output (out) follows the power supply V_s_1, and at the same time PMOS_1 gets turned ON by output (out) and thus reduces charging resistance. During at the hold phase charge stored on the load capacitances flow back to power supply through PMOS_1.

VI.RESULT AND DISCUSSION

All design is to be simulated using W-Edit and T-Spice simulator with transient time 80ns. Simulations are done at 90nm technology.

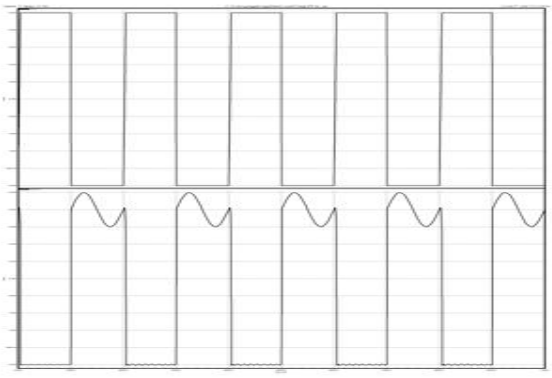

Figure 6. Waveform of PFAL based Inverter

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Figure.6 shows the waveform of PFAL based inverter. In this figure the above waveform is shows input of the inverter and lower waveform is output of the inverter. Output of PFAL based inverter is accurate, but power consumption of PFAL based inverter is very greater as compare to 2PASCL and Proposed adiabatic logic based inverter.

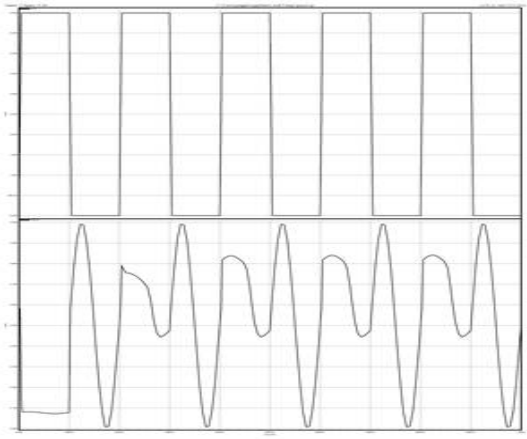

Figure 7. Waveform of 2PASCL based Inverter

Figure 7 shows the waveform of 2PASCL(Two Phase Adiabatic Static Clocked Logic) based inverter, in this figure the upper waveform is shows input and lower waveform is output of the inverter. The output of 2PASCL is not accurate. We have seen that, in figure 7 when we give input '1' inverter gives output '0', if input is '0' inverter gives output '1'. After that again we gave input '1' that time output of the inverter is not '0'. Power consumption of the 2PASCL based inverter is very less, but output is not accurate.

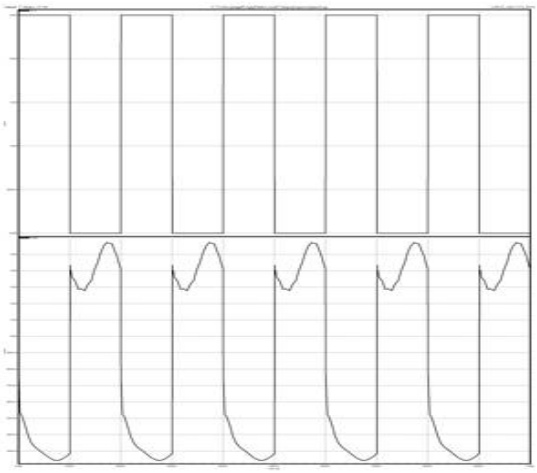

Figure 8. Waveform of proposed Adiabatic logic Inverter

Figure 8. shows Proposed Adiabatic logic based inverter. In this upper waveform is input of the inverter and lower waveform is output of the inverter. From above figure we have recognised that the output of these inverter is accurate, that means if we give '1' input that time output of the inverter is '0', and when input is '0' output of these inverter is '1'. Power consumption of proposed Adiabatic logic based inverter is less than PFAL based inverter.

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Table 1. Performance analysis of various logic styles for inverter at 90nm technology

S. NO.	LOGIC	POWER CONSUMPTION (µw)
1.	PFAL based Inverter	78.5
2.	Proposed adiabatic logic based Inverter	57.6

Power consumption of 2PASCL based inverter is lesser than the PFAL based inverter, but output of 2PASCL based inverter is not accurate, which is showed in Figure 7. For overcome to this drawback we have designed Proposed Adiabatic Logic circuit (Figure5). The output of this inverter is accurate which is shown in Figure 8, and the power consumption of this inverter is also lesser than the PFAL based Inverter.

VII.CONCLUSION

The main aim behind the whole work is to design and implement new low power digital circuits for inverter with the help of adiabatic logic family. The proposed circuit consumes quarter amount of power in comparison to the PFAL. 36.28% decrease power consumption of Proposed Adiabatic logic with respect to PFAL.

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