ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 6, June 2016

Dimensional Scaling Effect on Silicon Nanowire Based Field Effect Transistor

Rahul Kumar[1], S.B. Rana[2]

M.Tech. Student, Dept. of ECE, GNDU Regional Campus, Gurdaspur, India[1]

Assistant Professor, Dept. of ECE, GNDU Regional Campus, Gurdaspur, India[2]

ABSTRACT: Over the past three decades, by reducing the transistor lengths and the gate oxide thickness along with decrementing the supply voltage, there has been a steady amendment in transistor performance with a reduction in transistor size and a reduction in cost per function. The more an IC is down scaled, the higher becomes its packing density, the higher its circuit haste, and the lower its power dissipation. Recent developments of nanowires as small as possible have illustrated the progress possible in silicon nanowire technology. In this study we have explored the silicon nanowire FET as a possible candidate to replace the currently planar MOSFETs. In this research work silicon nanowire FET device is investigated. Various dimensional iterations were carried out and its characteristics were observed.

KEYWORDS: Nanowire, Silicon, FET, Scaling, IC.

I.INTRODUCTION

The word “nano” means that the size of object is 10^{-9} nm and the word "Science" meaning knowledge. So The Nanoscience is the branch of science which deals with the study of the objects with sizes in the 1 – 100 nm range. In the other words “Nanoscience” is a science of objects which are intermediate in size between the largest molecules and the smallest structures that can be fabricated by photolithography techniques and the science of objects with smallest dimensions ranging from a few nanometers to less than 100 nanometers [1-3]. Nanoscience and nanotechnologies are widely seen as having huge potential to bring benefits to many areas of research and application and are the attracting rapidly increasing investments from Governments and from businesses in many parts of the world. At the same time, it is recognised that their application may raise new challenges in the safety, regulatory or ethical domains that will require societal debate [3].

Nanomaterials refers to materials with internal structures and external dimensions within the size range measured in nanometers(nm) where 100 nm is frequently used as a delimiting size between the nanoscale and micro or macroscopic scales. In the nanoscale regime, some materials exhibit different features or properties as compared to the coarser materials with similar chemical composition. These materials are now used in a wide range of technological applications [4]. A nanowire is a nanostructure, with the diameter of the order of a nanometer (10^{-9} meters). It can also be defined as the ratio of the length to width being greater than 1000 [5]. Alternatively, nanowires can be defined as structures that have a thickness or diameter constrained to tens of nanometers or less and an unconstrained length. At these scales, quantum mechanical effects are important which coined the term “quantum wires” [5]. Silicon nanowires are quasi one-dimensional (1D) structures with a diameter of less than 100 nm. The very small diameter results in a large surface to volume ratio. This can be exploited in many ways in electronic devices . When a gate is wrapped around the nanowire, the optimum control of the nanowire potential by the gate potential is ensured. This makes nanowires an excellent choice for the ultimate silicon metal insulator semiconductor (MIS) devices . However, the same feature also allows implementing device concepts that would have very poor properties in a conventional planar configuration. The junctionless transistor and tunnel field effect transistors are two prominent examples. Additionally, new types of functionalities can be exploited by making the devices reconfigurable . When it comes to sensing devices, the small volume will allow effectively controlling the potential of the nanowire by even a very small input signal, making the approach very sensitive specifically for chemical sensing and bio-sensing. But also the field of energy generation and storage can benefit from the quasi 1D structure [6-7]. In the solar cells the nanowires allow to more efficiently collect the incoming solar radiation whereby in Li-ion batteries the structure allows for volume expansion. A transistor is a device that regulates current or voltage flow and acts as a switch or gate for electronic signals. Transistors

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 6, June 2016

consist of three layers of a semiconductor material, each capable of carrying a current. A transistor is a semiconductor device used to amplify or switch electronic signals and electrical power. Today, some transistors are packaged individually, but many more are found embedded in integrated circuits. The transistor is the fundamental building block of modern electronic devices, and is ubiquitous in modern electronic systems.[3] The field-effect transistor, sometimes called a unipolar transistor, uses either electrons (in n-channel FET) or holes (in p-channel FET) for conduction. The four terminals of the FET are named source, gate, drain, and body (substrate). On most FETs, the body is connected to the source inside the package [3].

In a Field-effect Transistors (FET), the drain-to-source current flows via a conducting channel that connects the source region to the drain region. The conductivity is varied by the electric field that is produced when a voltage is applied between the gate and source terminals; hence the current flowing between the drain and source is controlled by the voltage applied between the gate and source [3]. One of the important examples of nanowires is field effect transistors (FETs). Nanowires can be used for transistors. Transistors are used widely as fundamental building element in today's electronic circuits. As predicted by Moore's law, the dimension of transistors is shrinking smaller and smaller into nanoscale. One of the key challenges of building future nanoscale transistors is ensuring good gate control over the channel. Due to the high aspect ratio, if the gate dielectric is wrapped around the nanowire channel, we can get good control of channel electrostatic potential, thereby turning the transistor on and off efficiently [8].

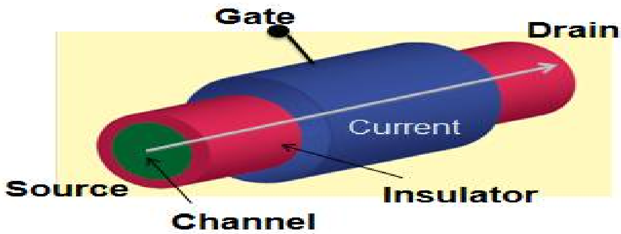


Fig. 1 Nanowire based FET

II.METHODOLOGY

Simulation of electronic devices generally involves self consistent solution of the electrostatic potential and carrier distribution inside the device. Over the years device engineers have improved our collective knowledge of carrier transport and semiconductor physics. Earlier treatment of electrons and holes as semi-classical particles with an effective mass was good enough to predict semiconductor device behavior and the drift diffusion equation was adequate to describe carrier transport. MuGFET is a simulation tool for nano-scale multi-gate FET structure. It provides self-consistent solutions to the Poisson and drift-diffusion equation. At the nanometer scale, quantum transport approaches. PADRE] is also developed in Bell Laboratories and a device-oriented simulator for 2D/3D device with arbitrary geometry. It provides many useful plots for engineers and deep understanding of physics. Many options are provided with respect to the numerical methods and semiconductor device physics.

In the research work Si materials nanowire are used as channel in the FET. For this work, the subthreshold characteristics and other device performance characteristics of the device are simulated. Simulation was carried out with channel diameter and oxide thickness is varied as shown in Table 1 and various characteristics parameters are simulated.

Table 1: Dimensional parameters for first set of simulation.

Channel Diameter (nm)	Oxide Thickness (nm)
5	2.5
10	5
20	10
30	15
40	20
50	20

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 6, June 2016

III. RESULT AND DISCUSSION

Effect of channel diameter and oxide thickness is simulated for Si nanowire channel based FET. Various characteristics parameters such as transfer characteristics and transconductance is simulated. Transfer characteristics: The drain current versus gate voltage is plotted in Fig. 2 for various dimension of nanowire channel diameter and oxide thickness. At x-axis gate voltage is taken from 0V to 1V and a y-axis drain current is plotted. It is observed from the graph that at lower dimensions the forward characteristics shows linear behavior upto 0.4 V and afterwards shows constant current.

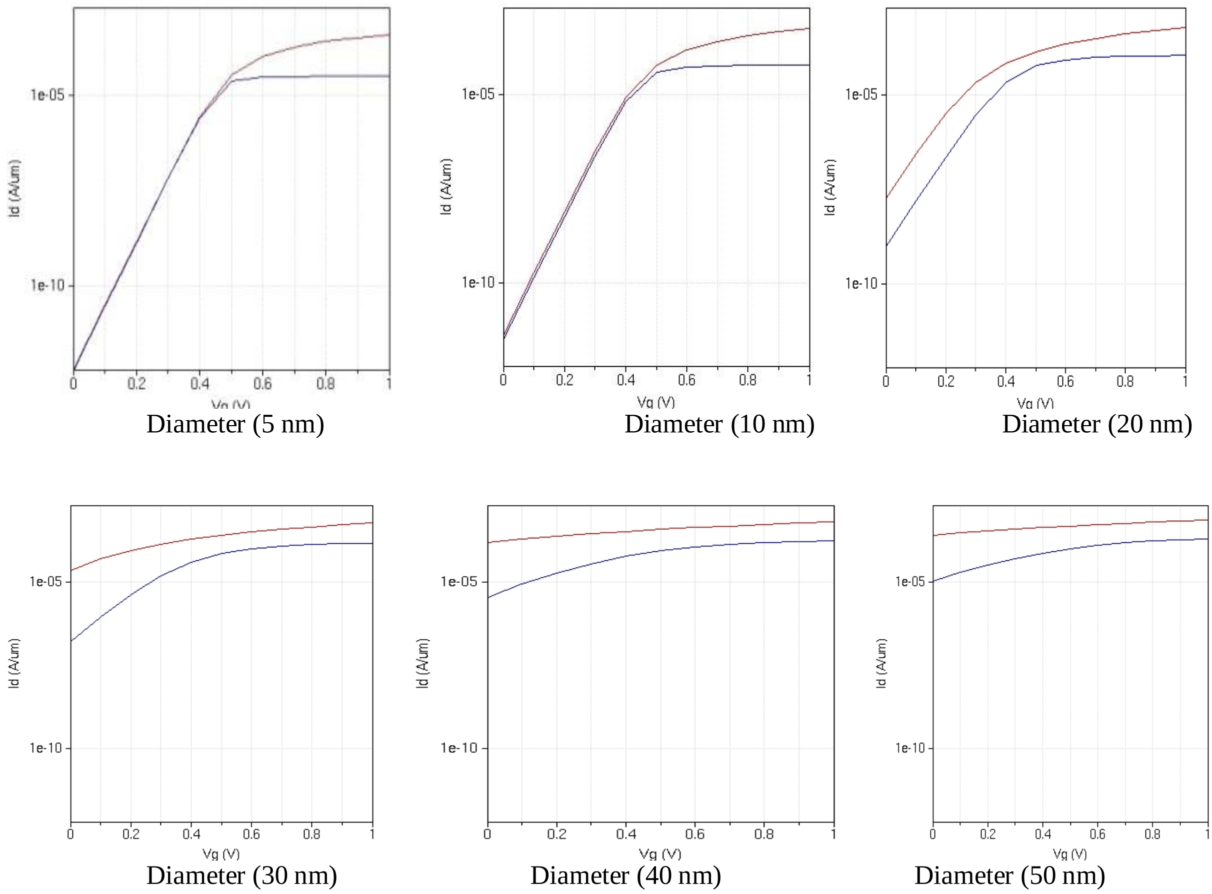


Fig. 2 Transfer characteristics.

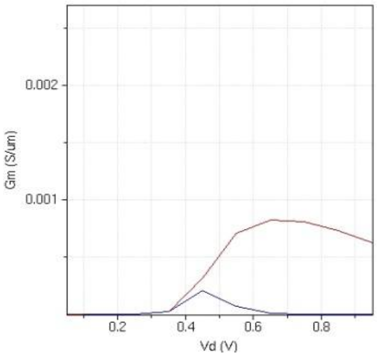
Transconductance: It is observed from the graph that transconductance is higher for low dimensional device for V_d ranging from 0V to 1V and it is maximum for 10 nm diameter and higher dimension of channel diameter the transconductance has lower value as shown in Fig. 4.2. A sharp increase is seen in case of lower dimension of channel. Maximum 0.001 S/µm is obtained for 10 nm channel diameter.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

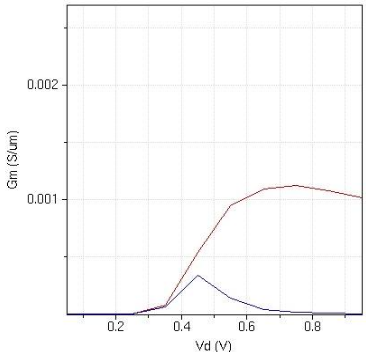
International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

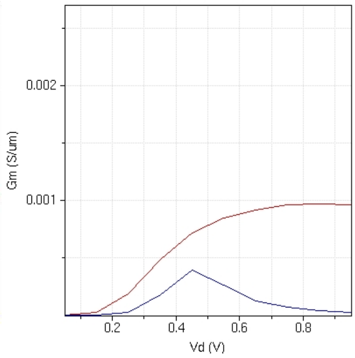
Vol. 5, Issue 6, June 2016



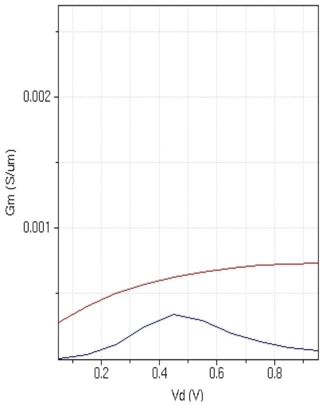
Diameter (5 nm)



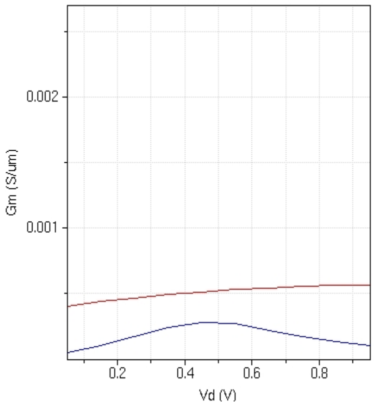
Diameter (10 nm)



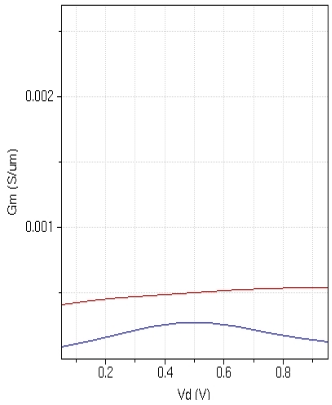
Diameter (20 nm)



Diameter (30 nm)



Diameter (40 nm)



Diameter (50 nm)

Fig. 3 Si nanowire channel based FET transconductance.

VI.CONCLUSION

In this study we have investigated the electrical characteristics of an Silicon Nanowire Field Effect Transistor (FET) using the quantum-ballistic transport model. As a starting point a comparative study was done between various simulated devices. The ON current for the simulation result was higher. The results were impressive which provided us confidence to move on with further simulations. Later, a simulation study was conducted to assess the advantages of silicon nanowire FET. It was found that nanowire FET exhibited superior current characteristics and controlled short channel effects better. In conclusion, the simulation study revealed that the silicon nanowire FET is an attractive candidate for FET device design for future technology nodes.

REFERENCES

[1] S. A. Yousaf and S. Ali "Why Nanoscience and Nanotechnology? What is there for us?", Journal of Faculty of Engineering & Technology, pp.11-20, 2008.

[2] T. Sands "Nanotubes and Nanowires- One-dimensional Materials, Nanotubes Materials", *Nanoletters*, 2006.

[3] C. Ngo and M. Voorde "Nanomaterials: doing more with less", *Nanotechnology in a nutshell*, pp. 67-82, 2011.

[4] P. Yang, R. Yan, M. Fardy "Semiconductor Nanowire: What's Next?", *Nanoletters*, Vol. 10, pp. 1529-1536, 2010.

[5] T. Mikolajick and W. Weber "Silicon Nanowires: Fabrication and Applications", *Springer International Publishing Switzerland*, pp.1-25, 2015.

[6] A. Cao, E. J. R. Sudholter, L. C P. M. de Smet, " Silicon Nanowire ‐ Based Devices for Gas Phase Sensing Sensors", *Sensors*, Vol. 14, pp. 245-271, 2014.

[7] J. Goldberger, A. Hochbaum, R. Fan, P. Yang "Silicon Vertically Integrated Nanowire Field Effect Transistors", *Nano letter*, Vol. 6, pp. 973-977, 2006.

[8] Abbass Hashim "Nanowires -Fundamental Research", *InTech*, 2011.