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Innovative System of Multilevel Inverter Employing a DC Voltage Source with Reduced Number of Switches

K.Rajasri, S.Karthikeyan

PG Scholar, Department of Electrical and Electronic Engineering, J.J College of Engineering and Technology, Trichy, India [1]

Assistant Professor (Senior Grade), Department of Electrical and Electronic Engineering, J.J College of Engineering and Technology, Trichy, India [2]

ABSTRACT: Recently, multilevel inverters are researched to apply various high power and high- voltage applications. By synthesizing several dc voltages, it generates an output voltage close to a sinusoidal wave. Switching loss and voltage rating of a switching device can be reduced by increasing the number of output voltage levels, which ensures a high quality output voltage with low THD. Multilevel inverter is well known as the most useful circuit topology to increase the number of output voltage levels in an efficient manner. It also shows a good characteristic on modularization. Many researchers focus on developing effective circuit topologies, which can reduce the number of components even though increasing the number of output voltage levels. It has introduced a modified H-bridge inverter, which is useful to reduce the number of switching devices by adding an upper switching device at series connected voltage sources. It is a good solution to save switching devices. In this paper, we propose a new multilevel circuit topology, which is suitable for reducing switching devices even though increasing the number of output voltage levels.

KEYWORDS: Inverters, multilevel systems, phase disposition(PD), pulse width modulation (PWM), total harmonic distortion (THD).

I. INTRODUCTION

RECENTLY, Multilevel Inverters Have Received Great Attention From the Industry Using High-Voltage And High-Power Applications**.** The proposed modified H-bridge multilevel inverter topology can be used in two possible motivations depending on the requirement of applications. The first motivation of multilevel inverter which are studies. The second motive is that multilevel inverters can synthesize stepped output voltages similar to a sinusoidal wave. Many numbers of voltage levels ensure a high-quality output voltage, which shows a good total harmonic distortion (THD) with low dv/dt stress and a small size of output filter. However, it needs a large number of circuit components. When dc voltages are scaled in power of three, it can maximize the number of output voltage levels. However, it still increases independent dc voltage sources to generate higher output voltage levels. To solve this problem, a multilevel inverter employing a cascaded transformer was introduced in Static Var compensator and active power filter with power injection capability, using 27-level inverters and photovoltaic cells. It also uses a combination of asymmetrical voltage sources to synthesize multilevel output voltages. Usually, these kinds of multilevel inverters were modified and developed from the CHB. . In a packed U-cell multilevel inverter was presented. It shows very good performance in the reduction of circuit components. However, it increases conduction losses when it generates each voltage level because the circulating current passes through three switching devices in each level generation. Multilevel inverters employing bidirectional switches and series-connected capacitors were proposed in [1] and [2]. Theoretically, they can generate a large number of output voltage levels over 125 levels with a reduced number of circuit components. However, each capacitor needs individual dc-to-dc converters to obtain dc voltage sources. A modular multilevel converter was introduced in [3]. It has a good modular characteristic; thus, it is easy to be extended to high voltage levels. It consists oflevel-generating stage and a polarity selection part to reduce the switching losses.However, it fails to reduce the

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number of dc voltage sources when it increases the output voltage levels. A multilevel inverter using switched series/parallel dc voltage sources was introduced in [4]. Although it can increase the number of output voltage levels, the switching pattern is complex, and it increases conduction losses. A photovoltaic multilevel inverter using series-connected capacitors was investigated in [5]. Now a day's many industrial applications have begun to require high power. Some appliances in the industries however require medium or low power for their operation. Using a high power source for all industrial loads may prove beneficial to some motors requiring high power, while it may damage the other loads. Some medium voltage motor drives and utility applications require medium voltage. The multilevel inverter has been introduced since 1975 as alternative in high power and medium voltage situations.

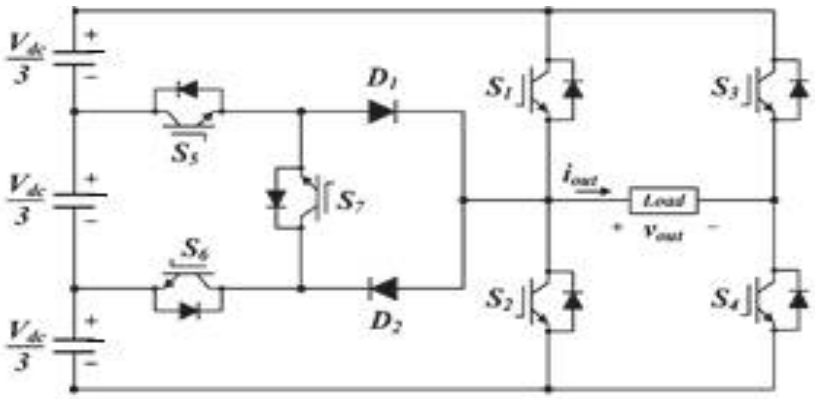

Fig.1. Circuit configuration of the proposed seven-level PWM inverter

In this paper, we present an effective circuit configuration of a multilevel inverter that can increase the number of output voltage levels with a reduced number of circuit components. It consists of a dc voltage source series connected voltages, two diodes, three switches for synthesizing output voltage levels, and an H-bridge cell. To verify the validity of the proposed approach, we carry out computer aided simulations and experiments. Here, we also introduce a modified pulse width modulation (PWM) control scheme to solve the capacitor voltage unbalancing that occurred in series connected capacitors. Fig. 1 shows a circuit configuration of the proposed seven levels PWM inverter. It has dc voltage source, which is divided by three source connected in series. Let us assume that all components are ideal and that the circuit is in a steady state. Each source voltage is equal to *V*dc/3. Then, we can obtain seven levels in the output voltage wave that is Vdc/3, 2vdc/3, and Vdc. For negative path -Vdc/3,-2vdc/3, and –Vdc. The switches are an H bridge cells work to determine thepolarity of the output voltage with the highest or lowest voltage level. Each voltage source consists of 150v supply as input.

II. PROPOSED SEVEN LEVEL MULTILEVEL INVERTER

The proposed 7-level symmetric inverter topology consists of H-bridge cell, PWM inverter, IGBT gate, Diode, DC source. The serious connection of dc source with IGBT switches are S1 to S11. Diodes D1, D2 are connected in antiparallel. It has a three dc voltage source, which is connected in series. Let us assume that all components are ideal and that the circuit is in a steady state. Each capacitor voltage is equal to *V*dc/3. Then, we can obtain seven levels in the output voltage wave, i.e., *V*dc, 2*V*dc/3,*Vdc*/3, 0, −*V*dc/3, −2*V*dc/3, and −*V*dc. The switches in an H-bridge cell (*S*1∼*S*4) work to determine the polarity of the output voltage with the highest (or lowest) voltage level, i.e., *V*dc(or −*V*dc).Other voltage levels are generated by *S*5, *S*6, and *S*7.It consists of 150v supply as input

2.1 Generation of Output Voltage Levels

For better understanding, every current path for generating Seven levels is given in

Fig. 2(a). Here, the highlighted line Level Vdc: shows a current path when the output voltage is Vdc. Three sources connected in series supply energy to the output load. It discharges through S1 and S4. If a load is an inductive load and the direction of the load current is opposite, the current flows through DS1 and DS4, and it charges the capacitor stack.

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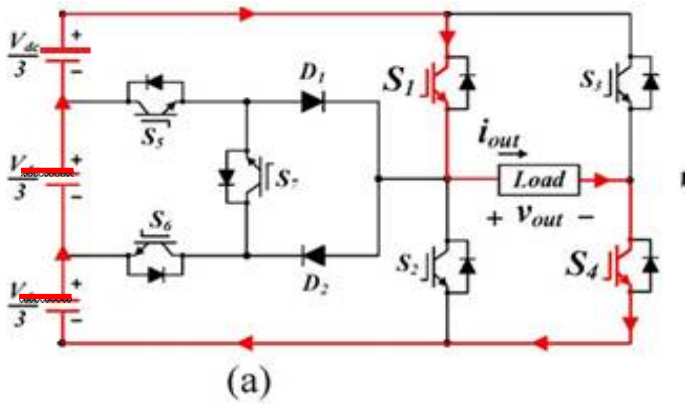

Fig. 2(b). Level 2Vdc/3: A current path when the output voltage is 2Vdc/3. Two voltage sources Vdc2 and Vdc3 feed the output load. It discharges through S5, D1, and S4. When the direction of the load current is opposite, there is no current path under this switching state. Regardless of the load current flows, the output voltage is clamped as the 2Vdc/3 level by the switching state.

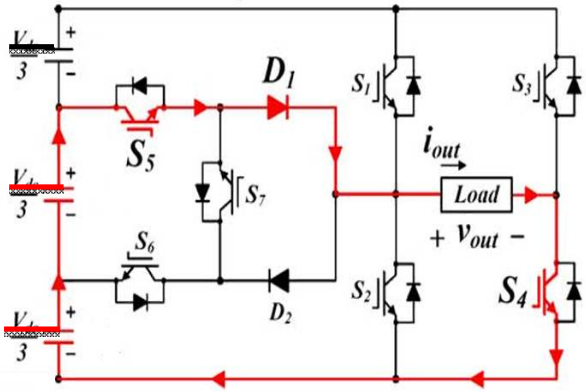

Fig. 2(c). Level Vdc: A current path when the output voltage is Vdc/3. The three voltage sources supplies energy to the output load. It discharges through S1, S4. If the direction of the load current is opposite, the load current flows through S3and S2.

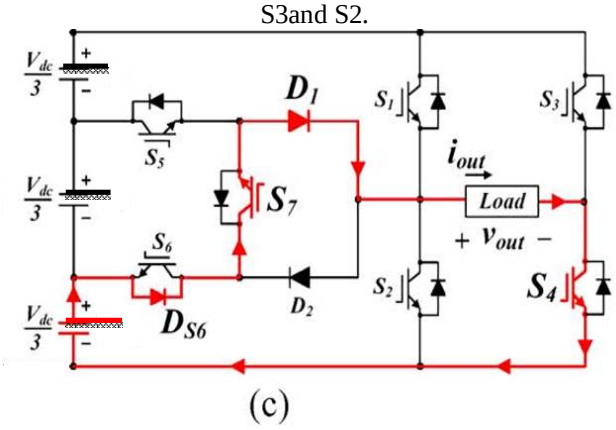

Fig. 2(d). Level 0: to generate a zero level, two switching schemes can be considered. The basic idea to generate a zero level is voltage cancelation. When s2 and s4 turn on simultaneously, the output voltage becomes zero. The other method is to turn s1 and s3 on at the same time. When the direction of the load current is opposite, the current will flow in zero level. Level-vdc/3

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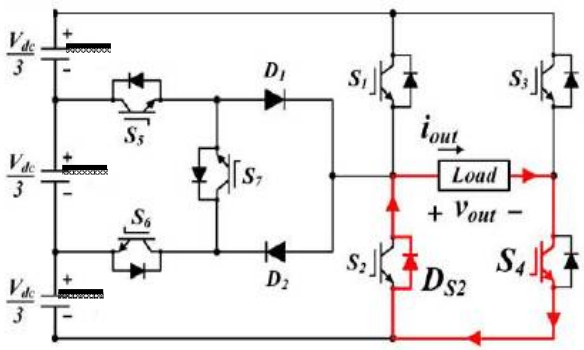
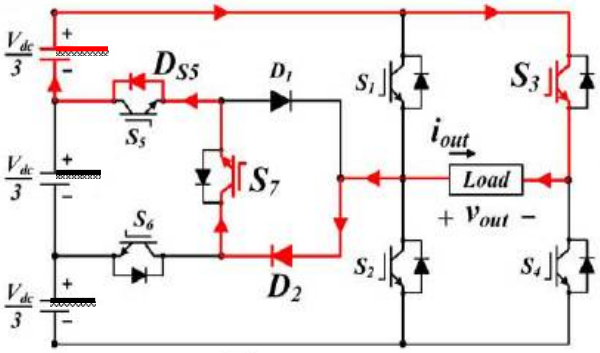


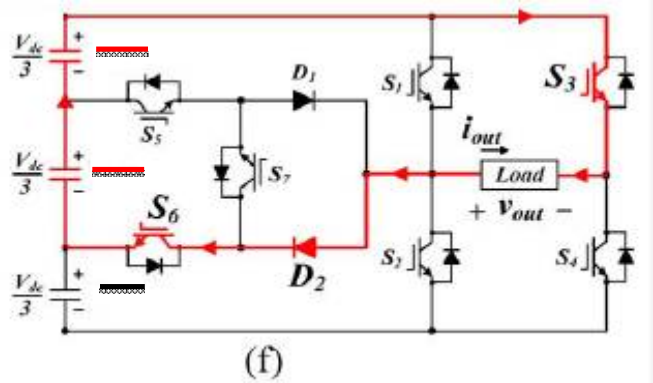
(d)

fig. 2(e) shows a current path when it produces the -Vdc/3 level. The upper capacitor (c1) supplies energy to the output load. Level-2vdc/3.



(e)

fig. 2(f) shows a current path when the output voltage is -Vdc/3. Two capacitors c1 and c2 supply energy to the output load. Level-Vdc/3



(f)

fig. 2(g) shows a current path when the output voltage is -vdc/3. three capacitors connected in series supply energy to the output load.

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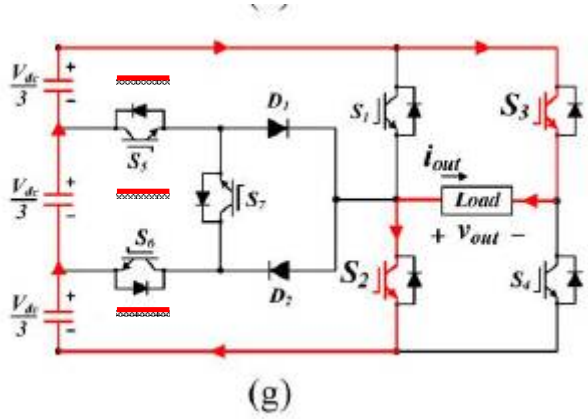

(g)

2.2 General Switching Scheme

Fig. 3 shows a general phase-disposition switching scheme for controlling the proposed seven-level PWM inverter. It uses a reference and three carrier waves, which have the same frequency and amplitude but different offset voltages. Table I lists the switching patterns for generating seven output voltage levels. By comparing the reference and each carrier wave, it produces command signals. One cycle of the reference voltage is divided into six modes according to voltage.

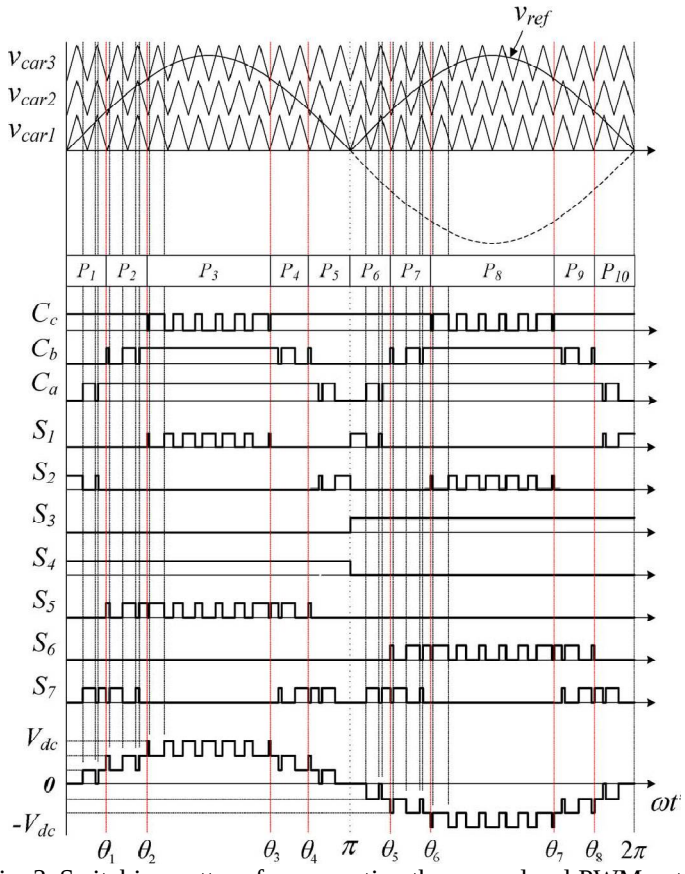

Fig. 3. Switching pattern for generating the seven-level PWM output voltage

The reference signal comparing with carrier generating pulse which is then modified feeding to logic gates in order to get the required pattern to trigger the switches at the proper instant. For examples switches S1 needs to have a pulse so as to obtain +Vdc and −3Vdc and S2 requires +2Vdc and −2Vdc. S3 conducts +3Vdc and −Vdc. Also, switches S5 and S4 conduct positive and negative half cycles, respectively.

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III. RESULTS AND DISCUSSIONS

3.1 SIMULATION AND EXPERIMENTAL RESULTS

0To verify the validity of the proposed seven-level PWM inverter, we carried out computer-aided simulations using PSIM and experiments using a prototype of 1 kW. The input dc voltage is set to dc 150 V; hence, each capacitor voltage is divided into dc 50 V in an ideal case. The frequency of an output voltage is set to 60 HZ.

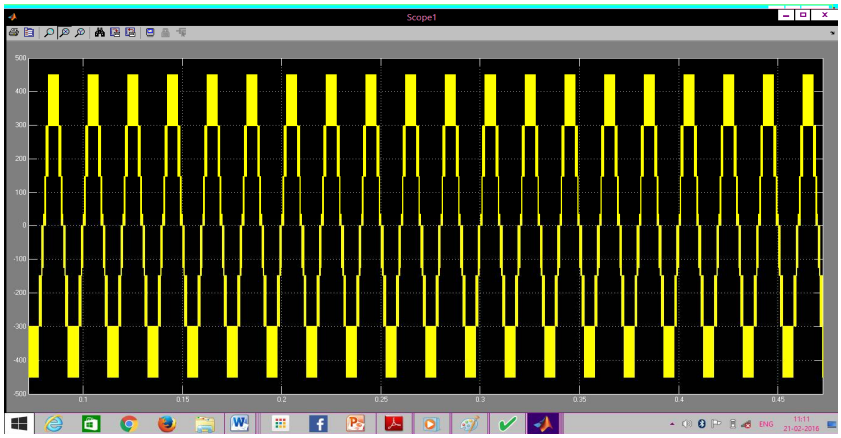
TABULATION FOR PARAMETER USED

Parameter	Symbol	Simulation & Experiment
Input Voltage	V_{dc}	150 [V_{DC}]
Output Voltage	v_{out}	110 [V_{AC}], 60 [Hz], 1 [kW]
Carrier wave Frequency	f_s	10 [kHz]
Capacitor	C_1 C_2 C_3	1100 [μF]
LC Filter	L_o C_o	8 [mH] 2.2 [μF]
Controller	-	TMS320F28335 (DSP)
Gate-amp	-	TLP250 (Photo-coupler)
Switch	$S_1 - S_7$	IRF360 (Power MOSFET)
Diode	D_1 D_2	MUR1540 (Ultra Fast Recovery)
Voltage Sensor	-	HCPL-7800A (Isolation)

The simulation results of the output voltage and the capacitor voltage with a general switching method Fig. 6(a), we can find that the middle voltage levels (±2*V*dc/3) disappeared as time goes by. At 0.25 s, the output voltage level shows just five levels similar to that of a five-level PWM inverter, which has two series-connected voltages.

SIMULATATION RESULTS OF SEVENLEVEL MULTILEVEL INVERTER

This shows the experimental waveforms of the output voltages when the proposed inverter connects to an inductive load. The output voltages according to the modulation index are the same resistive load. The difference is that the load current lags to the output voltage due to the intrinsic characteristic of the inductive load. Thus, the proposed circuit topology is unsuitable to apply high-voltage applications.



In addition, we need careful attention to reduce the conduction losses in the middle switches and reverse the recovery losses caused by the turning off of the diodes during switching. To input dc voltage. Fig. 6 shows the simulation results of the output voltage with a general switching method. We can find that the middle voltage levels (±2*V*dc/3) disappeared as time goes by. At 0.25 s, the output voltage level shows just five levels similar to that of a five-level PWM inverter. This has two series-connected capacitors. The output is shown in Fig 6. Each supply of voltage source is 150v. The series connection of input voltage is very important to generate the proposed multilevel inverter.

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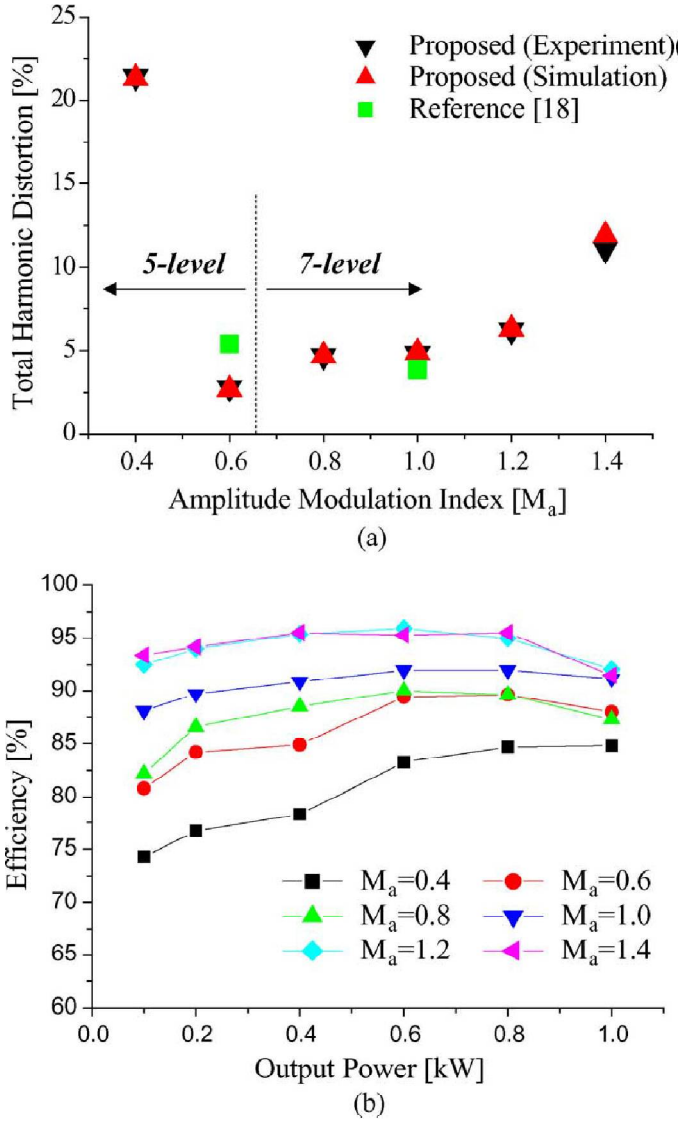

Fig.5 Comparison of THD*v* and the efficiency. (a) Comparison of THD*v* according to the modulation index. (b) Efficiency according to the modulation index and the output power.

TABULATATION II
COMPARISON OF THE NUMBER OF CIRCUIT COMPONENTS

No. of components	FC	DC	CH	Ref [12]	Ref [13]	Ref [16]	Ref [18]	Proposed
Switch	12	12	12	6	10	10	6	7 (+1)
Diode	0	6	0	0	0	0	8	2 (+2)
Capacitor	6	3	3	1	3	0	3	3 (+3)
Input DC source	1	1	3	1	3	3	1	1 (0)

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In Table II, we compare the number of circuit components with its counterparts, i.e., flying capacitors (labelled as FC), diode clamped (labelled as DC), cascaded H-bridge (labelled as CH), [3], and [5] when they generate a seven level output voltage. In Table IV, the minimum number of components is in bold, and the parentheses of the proposed mean the comparison results with the best case. In this comparison, the best approaches in the viewpoint of saving the number of switches are the works in [6] and [5]. However, the work in [6] has a higher conduction loss and voltage across the capacitor and has big ripples, although it employs a bulky capacitor of 5000 μF . The work in [5] is also good in reducing the number of switches, but it needs eight diodes. In the case of the proposed approach, it increases one switch, two diodes, and three capacitors compared with the best case of the counterparts. We can say that the most advantage of the proposed approach is the number of independent dc voltage sources.

IV. CONCLUSION

We proposed a multilevel PWM inverter that can effectively increase the number of output voltage levels with a single dc voltage source. In order to synthesize the seven-level output voltage, the proposed multilevel inverter needs a single dc voltage source with a series connection of three voltage source, two diodes, three active switches for synthesizing the output voltage levels, and an H-bridge cell.

TABULATATION III

we implemented computer-aided simulations to verify the validity of the proposed approach. Here, we introduced a modified switching scheme to solve the voltage unbalancing that occurred in the series-connected voltages. Finally,

COMPARISON OF THE BLOCKING VOLTAGE ON THE SWITCHING DEVICE

No. of components	FC	DC	CH	Ref [12]	Ref [13]	Ref [16]	Ref [18]	Proposed
Switch	12	12	12	6	10	10	6	7 (+1)
Diode	0	6	0	0	0	0	8	2 (+2)
Capacitor	6	3	3	1	3	0	3	3 (+3)
Input DC source	1	1	3	1	3	3	1	1 (0)

we carried out experiments using a 1-kW prototype, and we compared the number of main components, the blocking voltage on the switching devices, and THD*v* with previous multilevel inverters. As a result, we claim that the proposed seven-level PWM inverter can be a good candidate, which can substitute for the conventional PWM inverters in the power rating of a common use.

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