ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

VLSI Based Quality Analysis of Analog to Digital Converters

Sitara.S.H

PG Student [VLSI & Embedded Systems], Dept. of ECE, MA College of Engineering, Ernakulam, Kerala, India

ABSTRACT: This paper introduces a new technique for measuring the static electrical parameters of an analog to digital converter (ADC). ADCs are widely used in various applications, ranging from control logic to fully integrated systems. It is of high importance that ADC's functionality is tested before realizing into the practical circuit. The testing can be done in industrial as well as laboratory fields. VLSI testers are also used to fulfill the purpose. They have the capability and flexibility to test a number of digital, analog and mixed signal components. But they are large machines that take up their own room and are very expensive. In this paper, the proposed system has a standalone feature and mainly focuses on the testing of ADC parameters. FPGA is the main controller of the system. It performs data capture, data storage and data transfer. The HDL development of interfaces is done using Xilinx platform. The test software in computer is developed using MATLAB.

KEYWORDS: Analog to Digital Converter, Differential Nonlinearity, Integral Nonlinearity, Graphical User Interface.

I.INTRODUCTION

The complexity of electronic device testing varies widely, from simplest manual type testing to the most complex, large scale automatic test equipment(ATE). Manual testing requires digital multimeters, oscilloscopes and other equipments, setup in a particular configuration, together with the test setup designed in automation tools such as cadence. When the device to be tested changes, it requires a change the test setup. ATE testers on the other hand, provides flexibility, allowing different types of components to be tested without changing the test hardware. Software changes can reconfigure these type of testing to accommodate different types of device. Moreover, it allows electronic testing with great complexity, although at a price. These testers can cost upwards a million dollars. In between the manual testing and ATE lies the low budget and medium scale testing. These type of test systems are usually dedicated for a particular component, under the control of a personal computer (PC).

II.STATIC PARAMETERS OF ADC

In ideal case, an ADC converts continuous analog signal into digital, usually binary coded. The minimal change of input signal that causes a change at the output side is related to ADC bitness. This quantity is known as least significant bit (LSB) and it determines resolution of ADC. The LSB value can be estimated as:

$$\text{LSB} = \frac{\Delta_{FS}}{2^N}$$

where Δ_{FS} is range of input signal, N is the ADC bitness. Δ_{FS} defines whether the ADC operates in unipolar or bipolar mode. In the first case input signal voltage ranges between 0 and FS, where FS denotes full scale voltage. It is often related to reference voltage of ADC. In case of bipolar operation mode, Δ_{FS} ranges between – FS and FS. Today, converters available in market vary in terms of price, resolution, performance and quality. The quality is defined by set of parameters, which can be divided into static and dynamic.

Differential non-linearity (DNL) is defined as the difference between the step width of actual transfer function and the perfect transfer function. It is illustrated in figure 1. If DNL is greater than | 0.5|LSB, then it indicates a missing code.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

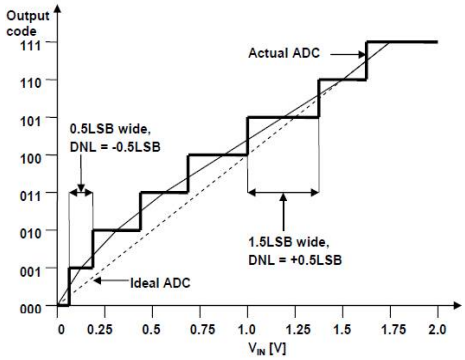


Fig. 1 Graphical representation of DNL

Integral non-linearity (INL) is defined as the maximum vertical difference between the actual and the ideal transfer functions. INL can also be interpreted as the sum of DNLs. So we can say that distribution of DNL determines the INL of an ADC. It is graphically represented as shown in figure 2.

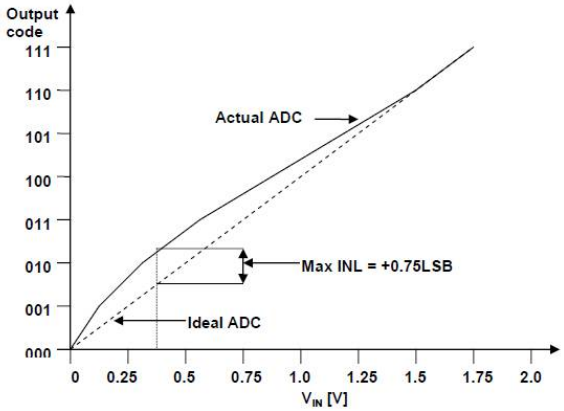


Fig. 2 Graphical representation of INL

III.SYSTEM OVERVIEW

In this proposed system, FPGA is the main controller. It is interfaced with memory and device under test(DUT). The basic flow of this system starts with the command from PC to initiate operations. DUT waits for the instruction from controller. When the valid instruction is obtained, DUT starts communicating with the controller. The obtained values are stored in a memory. As soon as the controller obtains a termination command from the DUT, controller starts transferring obtained data to the PC. Various verilog modules used in the system are listed below:

- UART Receiver and Transmitter
- Memory module
- Decoders
- Counters

In addition to these modules developed on the Xilinx platform, we also require a MATLAB graphical user interface from where we send the commands to the FPGA, as well as perform the computations. The overall block diagram of the system is shown in figure 3.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

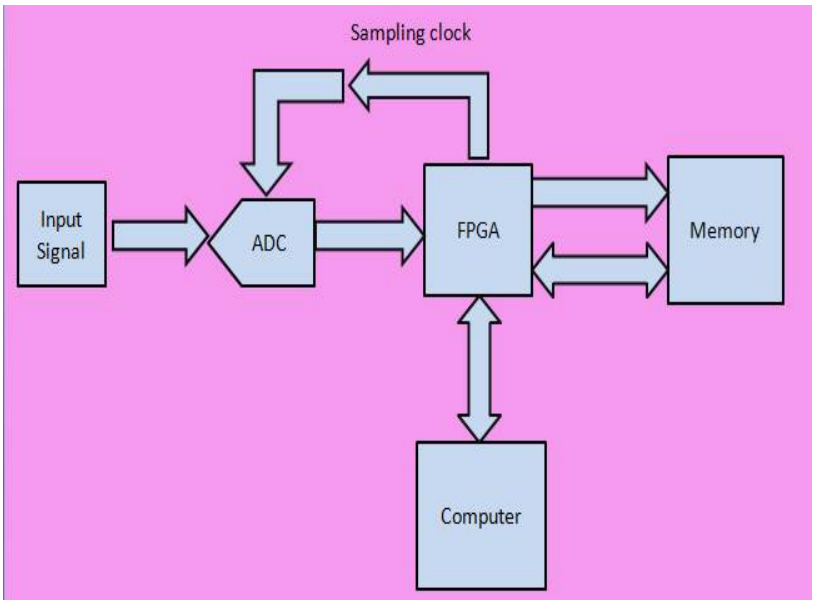


Fig. 3 Block diagram of the system

IV.IMPLEMENTATION OF HISTOGRAM METHOD

Different methods exist to evaluate the performance of an ADC based on finding points of code transitions. But the main problem is to define these points due to the presence of noise. Whereas, the histogram method can be used for the evaluation of any static parameters of ADC with any level of noise. For *k* code words ranging from 1 to 2*N* – 2, and if there are *M* samples, then occurrence of each codeword is calculated. Overload codes, such as all zeros and all ones are not included for calculations. Theoretical number of occurrences for each code is then:

$$n(k)_{theoretical} = \frac{M}{2^N - 2}$$

If n(k)actual is the actual number of occurrences for *k*'th codeword, then the DNL for this code word is calculated as

$$DNL_k = -\frac{n(k)_{actual}}{n(k)_{theoretical}}$$

DNL for the complete ADC is then:

$$DNL = \max(|DNL_k|)$$

Once the DNL is known, it is possible to calculate the INL as:

$$INL = \sum_{k=1}^{m} DNL_k$$

So, it can be said that distribution of DNL determines the integral nonlinearity of ADC. The simplest way to calculate histogram using programmable logic is to use the output code word as an address for corresponding counter. Each time

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

the code word is being read, the value of respective counter is increased and thus it is possible to form required histogram. When using such an approach the system requires N-to-2^N decoder and 2^N counters, where N is the resolution in terms of bits.

UART is a protocol that translates data between serial and parallel form. In the proposed system, operation starts with the command from the PC to start conversion. This command is generated using MATLAB's graphical user interface(GUI). The UART receiver on the FPGA receives this command and send the start of conversion(SOC) signal to the ADC. Similarly, after the conversion completes and acquiring the histogram values, they are send via UART transmitter to the PC.

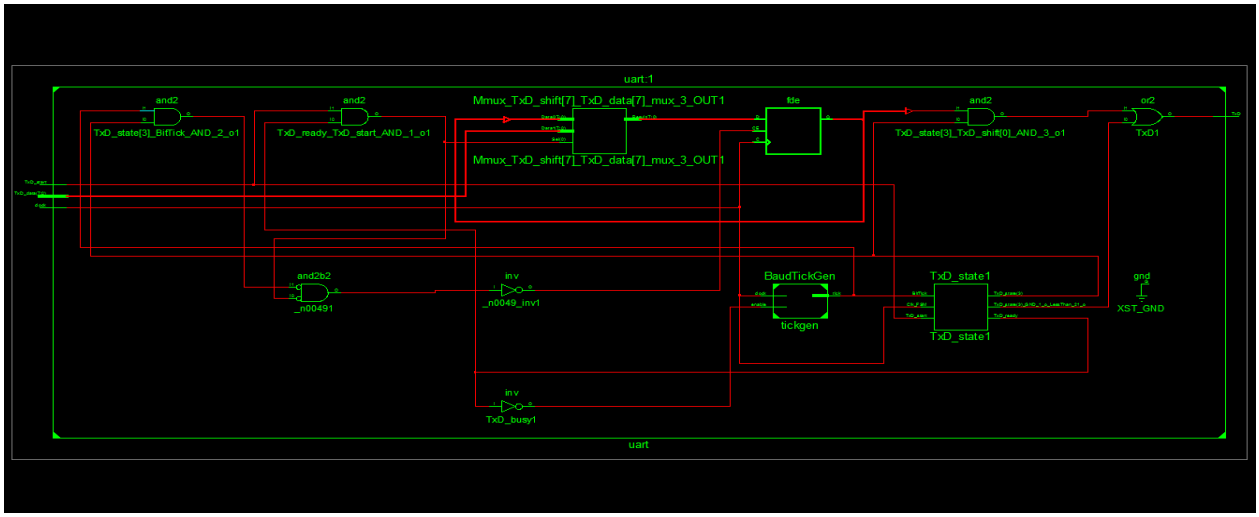


Fig. 4 RTL Schematic of UART transmitter

In the PC, histogram is plotted, which is then normalized to find the DNL. Once the plot for DNL is obtained, INL is simply the addition of DNLs. Data is commonly sent as group of 8 bits, called byte and is serialized. The speed of communication is specified in baud, i.e. how many bits-per-seconds can be sent. In this paper, an UART interface is designed with 1 start bit, 2 stop bits and a baud rate of 11520. The RTL schematic and simulation result of UART transmitter are shown in figure 4 and 5 respectively

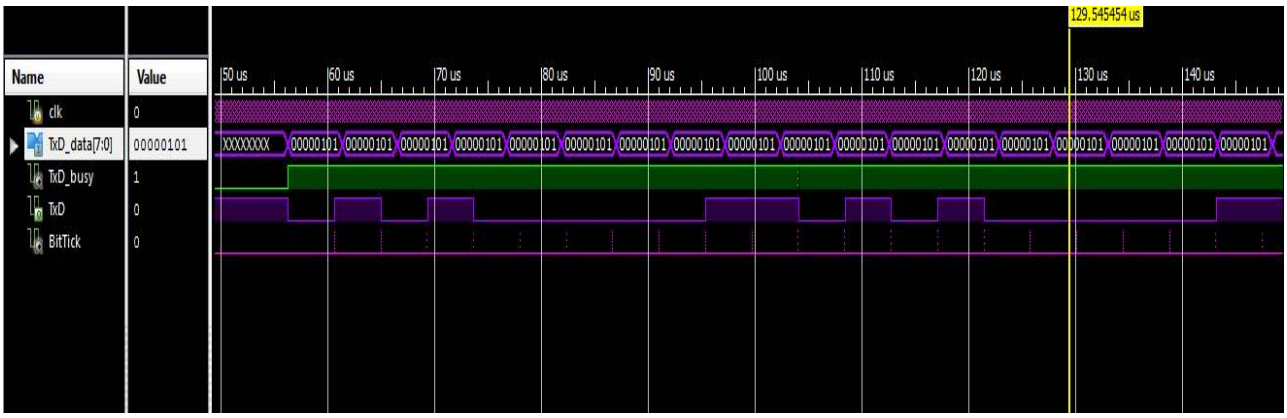


Fig. 5 Simulation result of UART transmitter

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

There are several important factors to be considered while performing histogram test. The most important is number of samples required to effectively measure DNL and INL. The number of samples determine the size of memory module. Assume an 8-bit, 1-MSPS ADC, and that it is desired to obtain an average of 100 hits in each code bin. With 100 hits per code bin, a DNL resolution of 1/100 = 0.01 LSB can be obtained. This implies that the input ramp should sweep through all of the 2^8 = 256 levels, dwelling on each code long enough to produce 100 hits per level. The total number of samples required is therefore M = 100 × 256 = 25,600 samples. So we can say that 8*25600 sized memory module is required. The memory can be designed using verilog coding, or can be directly taken from the IPcore. The simulation result of the memory module is given in figure 6.

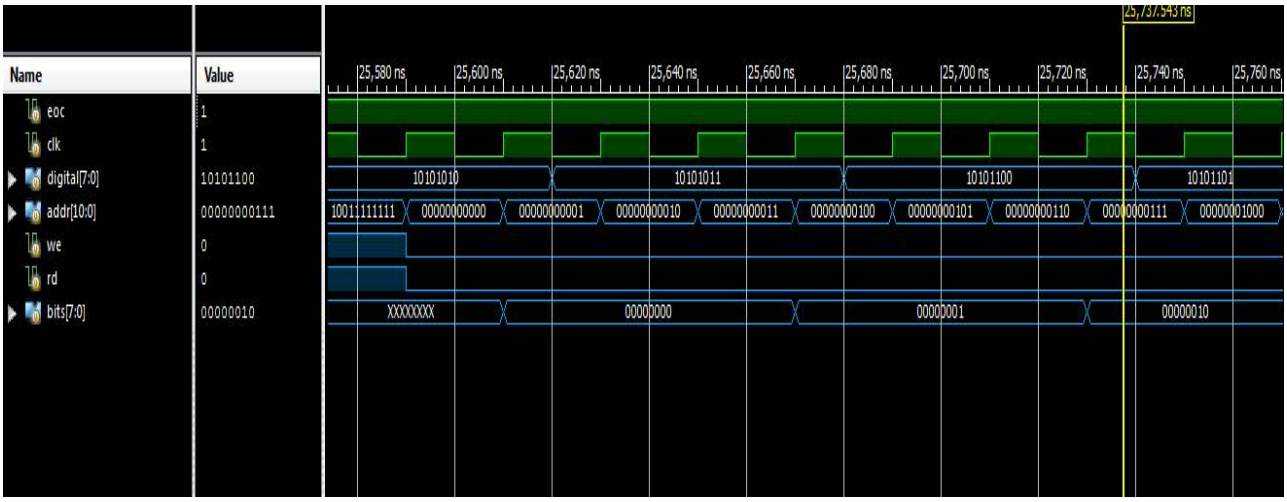


Fig. 6 Simulation result of memory module

The data read from the memory module is an 8 bit data whose value may vary from 0 to 256. So to decode the data we require an 8 to 256 decoder. In usual case, an 8 to 256 decoder requires 8 input lines and 256 output lines. In the proposed method, same is implemented using 4 lower order decoders having 6 input lines, 64 output lines and 2 select inputs. The two higher order inputs are taken as the select inputs. Depending on these select inputs, one out of the four decoders will be enabled and then one out of the 64 outputs will be asserted high. The simulation result of first decoder, decoding from 0 to 63 are shown in figure 7.

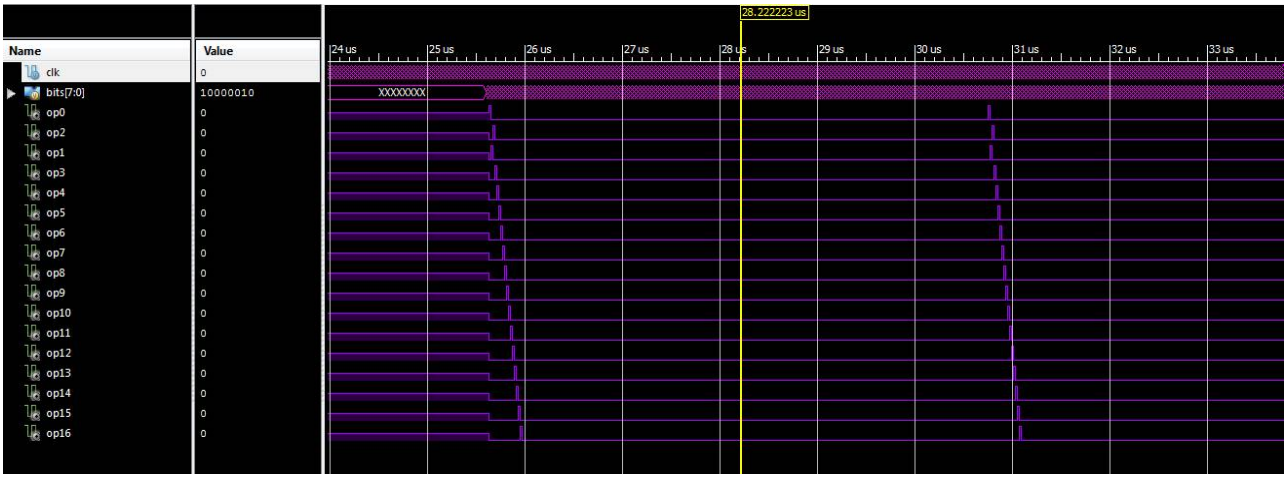


Fig. 7 Simulation result of decoder section

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

The decoder outputs should then be counted to determine the actual number of occurrences for each code word. These counter values are plotted as a histogram, which is then processed to determine the required parameters. So, for an 8 bit ADC it requires 256 counters. In this paper, 256 8 bit counters are designed so that each counter can count upto 256. Simulation result corresponding to the counter is shown in figure 8.

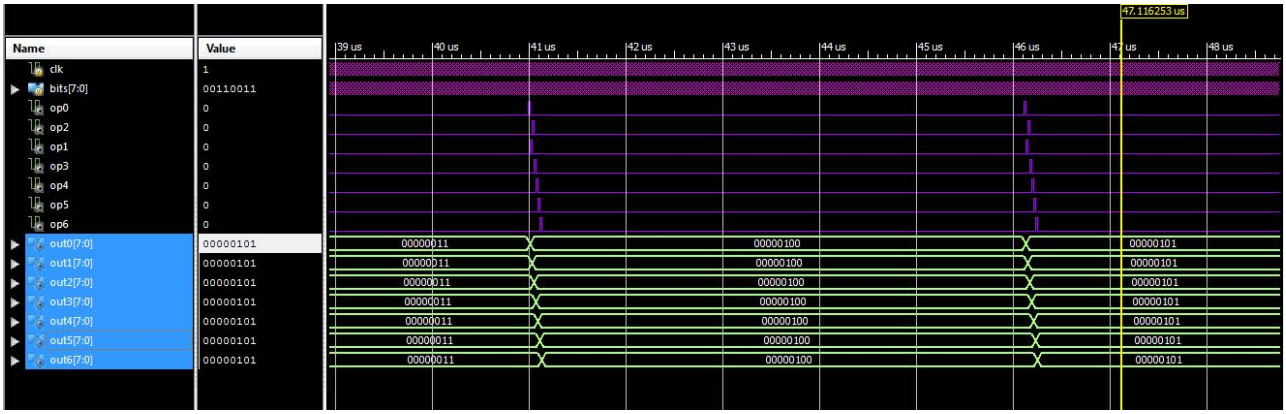
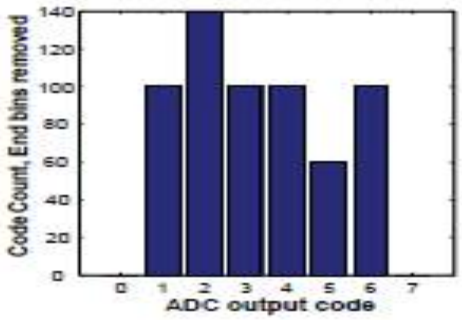


Fig. 8 Simulation result of counters

The parameter extraction steps can be summarised as follows:

I. Remove the over-range bins i.e. 0 and full scale



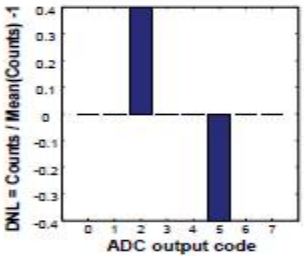
II. Compute average count/bin (25600/256=100, in this case)

III. Normalize

- Divide histogram by average count/bin. Ideal bins have the exactly average count/bin, which after normalization becomes 1.
- Non ideal bins have count/bin greater than or less than 1.

IV. Subtract 1 from the normalized code count

V. Result gives DNL (0.4 LSB for the figure shown)



ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

V. RESULT AND DISCUSSION

A graphical user interface (GUI) was developed in MATLAB where the final results are displayed. Figure 9 shows the simulation result of the overall system.

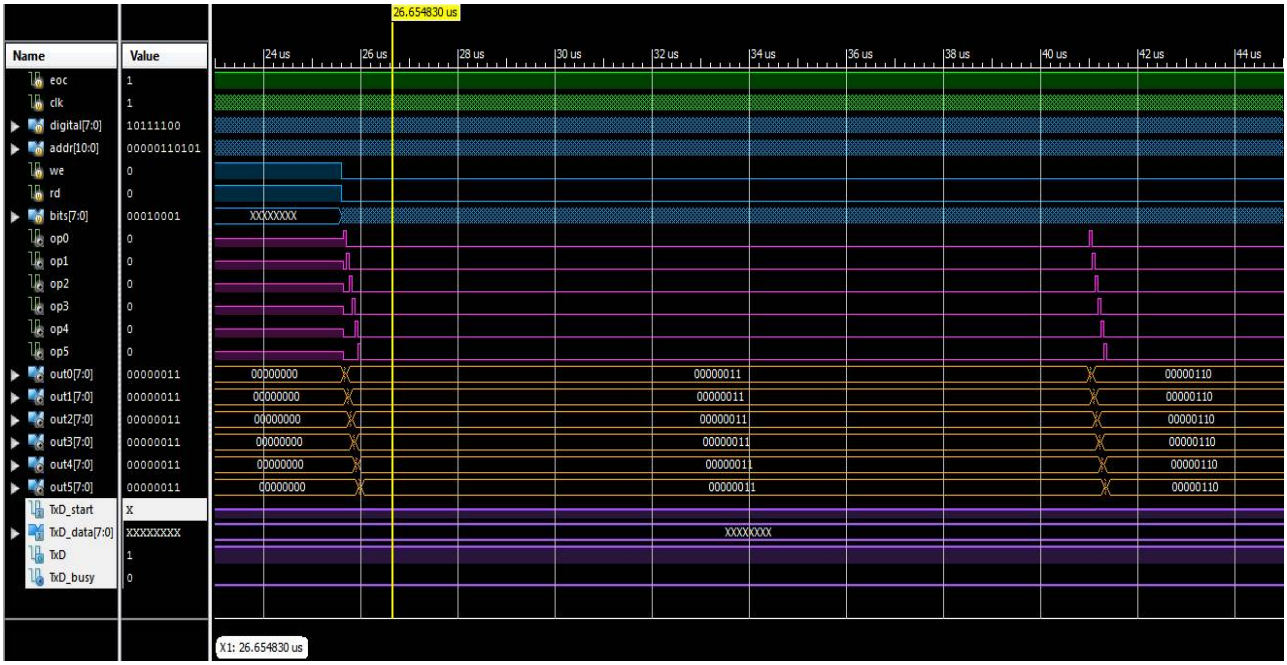


Fig. 9 Simulation result of the overall system

Device utilization summary of Spartan 3xc3s700an-4fg484 board is given in figure 10. From the synthesis report generated using Xilinx ISE design suite v14.5, it is evident that the proposed technique is an efficient method for measuring the static electrical parameters of ADC.

top Project Status (06/19/2016 - 18:49:55)			
Project File:	TEST.xise	**Parser Errors:**	No Errors
Module Name:	ADCTEST	**Implementation State:**	Synthesized
Target Device:	xc3s700an-5fgg484	**• Errors:**	No Errors
Product Version:	ISE 14.5	**• Warnings:**	11 Warnings (5 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	4216	5888	71%
Number of Slice Flip Flops	4676	11776	39%
Number of 4 input LUTs	7314	11776	62%
Number of bonded IOBs	11	372	2%
Number of BRAMs	1	20	5%
Number of GCLKs	1	24	4%

Fig. 10 Device utilization summary

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

VI.CONCLUSION

VLSI based test setup for Analog to Digital Converter was designed and implemented using verilog on Spartan 3 FPGA. Every module was constructed independently and was later combined to form the whole system. The whole system was simulated successfully and implemented on the Spartan 3 FPGA board. Since ADCs are widely used in most of the fields, it is necessary to measure its parameters to assure its quality. . At present, it is required to measure the static and dynamic parameters, but in future, as one step further it is required to design the data converter as required for the specified application.

REFERENCES

[1] Alegria F., Arpaia P., da Cruz Serra A.M, Daponte P. " Performance analysis of an ADC Histogram test using small triangular waves ," IEEE Transaction on Instrumentation and Measurement, 2002, vol. 51, no.4, pp. 723-729.
[2] Kester W.A., "The data conversion handbook", 2005, Oxford: Elsevier. 976 p.
[3] Robert H. Walden., "Analog to digital converter survey and analysis," IEEE Journal on Selected Areas in Communication, 1999, vol. 17, no. 4, pp. 539-550.
[4] Andreas Lechner & Andrew Richardson, "Test of A/D converters," From converter characteristics to built-in self-test proposals.
[5] Dr R. A. Cobley, "Onchip testing of ADCs".
[6] Shridhar Atmaram More., "ADC Performance Parameters - Convert the Units Correctly ,Mayl 2013.
[7] Alfred K. Susskind, "Notes on Analog-Digital Conversion Techniques," John Wiley and Sons, 1968.
[8] P. D. Capofreddi, B. A. Wooley: "The Efficiency of Methods For Measuring A/D ConverterLinearity", IEEE Trans. Instrum. Meas., 1999, vol. 48, No. 3, pp. 763-769.
[9] Open Verilog International, Inc.: Verilog-A Language Reference Manual, Version 1.0, August 1996
[10] C. Wegener: Applications of Linear Modeling to Testing and Characterizing D/A and A/D converters, Ph. D. Thesis, University College Cork, Ireland, 2003.
[11] T. Linnenbrink: Effective bits: is that all there is?, IEEE Transactions on Instrumentation and Measurement, 1984, vol. IM-33, no. 3, pp. 184-187
[12] G. Pretzl: Dynamic testing of high speed aid converters, IEEE Journal of Solid-State Circuits, 1978, vol. 13, pp. 368-371
[13] O. J. Downing & P. T. Johnson: A method for assessment of the performance of high speed analog / digital converters, Electronics Letters, 1978, vol. 14, no. 8, pp. 238-240
[14] J. Doernberg, H. S. Lee and D. A. Hodges: Full-speed testing of A/D converters, IEEE Journal of Solid-State Circuits, 1984, vol. 19, no. 6, pp. 820-827
[15] Maxim Application Note A177: INL/DNL measurements for high-speed analog-to-digital converters (ADCs), Maxim Integrated Products, September 2000