Design of Parallel in Parallel out Shift Register using Clocked Pass Transistor Logic

K.Chandra Sekhar[1], S.Suresh[2], P.V.K.Durga Prasad[3], M.Loknath[4], P.Pydi Reddy[5]

Assistant Professor, Dept. of ECE, RAGHU Institute of Technology, Visakhapatnam, Andhra Pradesh, India[1]

Assistant Professor, Dept. of ECE, RAGHU Institute of Technology, Visakhapatnam, Andhra Pradesh, India[2]

Associate Professor, Dept. of ECE, RAGHU Institute of Technology, Visakhapatnam, Andhra Pradesh, India[3]

Associate Professor, Dept. of ECE, RAGHU Institute of Technology, Visakhapatnam, Andhra Pradesh, India[4]

Assistant Professor, Dept. of ECE, RAGHU Institute of Technology, Visakhapatnam, Andhra Pradesh, India[5]

ABSTRACT: The major Power consuming component in most of the VLSI Circuit is Clock System. It consumes almost half of the total system power. It is necessary to reduce the power consumption because power budget is limited on portable digital circuits. In this paper, a new Low Power Clocked Pass Transistor Flip-Flop is proposed, which will considerably reduce the number of transistors in the discharging path and also reduces the capacity of the clock load by minimizing number of clocked transistors leading to reduction in clocking power which will improve the overall power consumption. Proposed reduced clock power flip flop is compared with conventional flip flops. Simulations are done using Microwind & Tanner software tools.

KEY WORDS: Flip-Flop; Low Power Clocking System; Pass transistors; Tanner; Micro-wind.

I. INTRODUCTION

Flip-Flops are extremely important circuit elements in all VLSI circuits. They are not only responsible for the correct timing, functionality and performance of the chip[1], but are also responsible for other clock distribution networks which consume a significant portion of the total power of the circuit. It is estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–45% of the total system power. Moreover, flip-flops have a large impact on circuit speed. The performance of the Flip-Flop is an important element that determines the performance of the entire circuit.

Flip-Flops are the basic elements for storing information and they are the fundamental building blocks for all sequential circuits. Flip-flops have their content change only either at the rising or falling edge of the enable signal. But, after the rising or falling edge of the enable signal, the flip-flop's content remains constant even if the input changes. Conditional Discharging Flip Flop (CDFF) uses 14 clocked transistors and Conditional Capture Flip Flop [2] (CCFF) uses 14 clocked transistors. In conventional D Flip Flops like the clock signal always flows in irrespective of whether the input changes or not. Part of the clock energy is unnecessarily consumed by the internal clock buffer to control the transmission gates. Hence, if the input of the flip-flop is identical to its output, the switching of the clock can be suppressed to conserve power. A large part of the on-chip power is consumed by the clock drivers. It is desirable to have less clocked load in the system.

II. CONDITIONAL DATA MAPPING D FLIP-FLOP
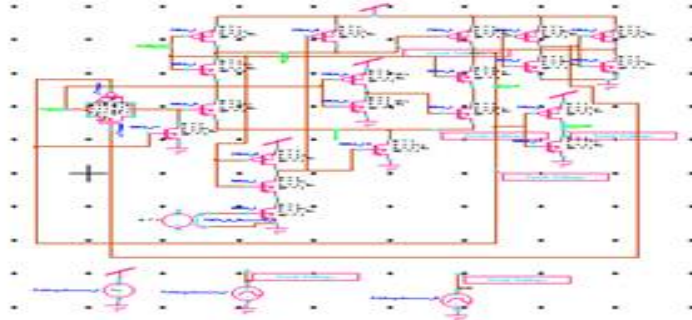
Fig 1. Conditional Data Mapping Flip flop   Design

Conditional Data Mapping Flip Flop (CDMFF) [3] used only 7 clocked transistors, resulting in about 50% reduction in the number of clocked transistors. The Fig.1 shows the Conditional Data Mapping Flip Flop Design. There is redundant clocking capacitance in CDMFF. When data remains 0 or 1, the pre-charging transistors, P1 and P2, keep switching without useful computation, resulting in redundant clocking. Clearly, it is necessary to reduce redundant power consumption here. Further, CDMFF has a floating node on critical path because its first stage is dynamic. When clock signal CLK transits from 0 to 1, CLKDB will remain 1 for a short period of time, which produces an implicit pulse window for evaluation. During that window, both P1, P2 are off. In addition, if D transits from 0 to 1, the pull down network will be disconnected by N3 using data mapping scheme (N6 turns off N3); If D is 0, the pull down network is disconnected from GND. Hence internal node X is not connected with Vdd or GND. During pulse windows, it is essentially floating periodically. With feature size shrinking, dynamic node is more prone to noise interruption because of the un-driven dynamic node. If a nearby noise discharges the node X, PMOS transistor P3 will be partially on, and a glitch will appear on output node Q. In a nano scale circuit, a glitch not only consumes power but could propagate to the next stage which makes the system more vulnerable to noise. Hence, CDMFF could not be used in noise intensive environment.

III. CLOCK PAIR SHARED FLIP-FLOP DESIGN
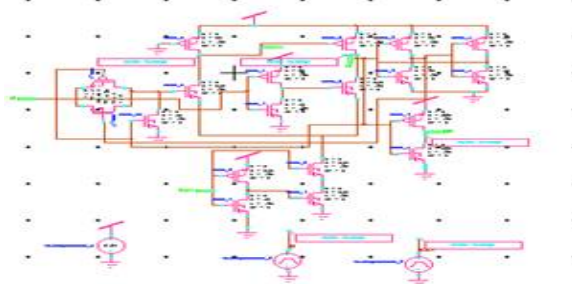
**Fig 2. Clock Pair Shared Flip-Flop Design**

Clocked Pair Shared Flip Flop (CPSFF) [4] used only 4 clocked transistors. Clocked Pair Shared flip-flop (CPSFF) showing in Fig.2 uses less clocked transistors than CDMFF and overcomes the floating problem in CDMFF. In the clocked-pair-shared flip-flop, clocked pair is shared by first and second stage. The p-MOS transistor P1is always ON and is used to charge the internal node rather than using the two clocked pre charging transistors (P1,P2) in CDMFF. Comparing with CDMFF, a total of three clocked transistors are reduced, such that the clock load seen by the clock driver is decreased, resulting in an efficient design. CPSFF uses four clocked transistors rather than seven clocked transistors in CDMFF, resulting in approximately 40% reduction in number of clocked transistors [6].

IV. PROPOSED LOW POWER CLOCKED PASS TRANSISTOR FLIP-FLOP DESIGN
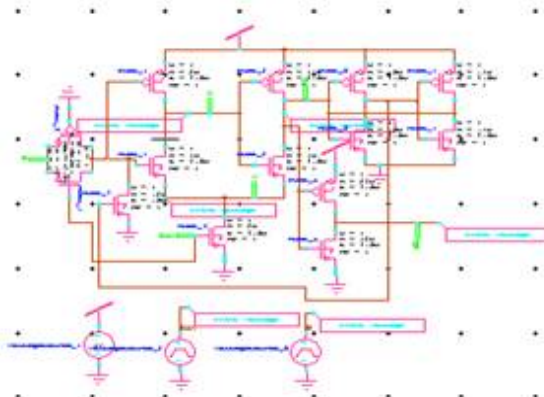
**Fig 3. Proposed Low Power Clocked Pass Transistor Flip-Flop**

Proposed Low power Clocked Pass Transistor Flip-Flop is Designed [5-9] by using Pass Transistor Logic family, In this design only one clocking transistor is used so that it will consume less power in the clock network of the Flip flop. When clock signal CLK transits from 1 to 0, P1 is conducting then node X is precharged and Q is'0', QB is '1', at that time Data 0 or 1. When clock signal CLK transits from 0 to 1, P1 is not conducting then node X is discharged and Q is'1', QB is '0', at that time Data '1'.By using the proposed flip flop, power consumption and area required are reduced compared to other conventional flip flops, and also delay factor is reduced due to the reduced number of transistors. Therefore, the low power flip flop can be used in design sequential circuit when compared to other flip-flop designs for low power and area requirements.

V.SHIFT REGISTERS

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All flip-flop is driven by a common clock.The storage capacity of a register is the total number of bits (1 or 0) of digital data it can retain. Each stage (flip flop) in a shift register represents one bit of storage capacity. Therefore the number of stages in a register determines its storage capacity.

B. PARALLEL IN PARALLEL OUT SHIFT REGISTER
For parallel in parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits.
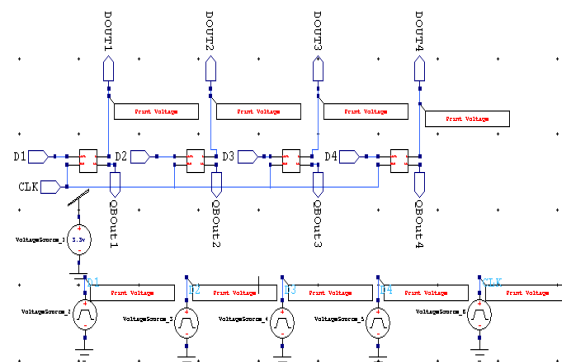
Fig 4. Schematic of Parallel in Parallel out Shift Register

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VI.SIMULATION RESULTS

To evaluate the performance, Shift Registers discussed in this paper are designed using 90-nm CMOS technology. All simulations are carried out using MICROWIND simulation tool at nominal conditions with 1GHz frequency range. Flip-Flop based Parallel in Parallel out Shift Register layout design is shown in Figure 7. The Simulation results are Shown in Figure 5 and Figure 6. The Comparison tables are shown in Table 1 , Table 2.
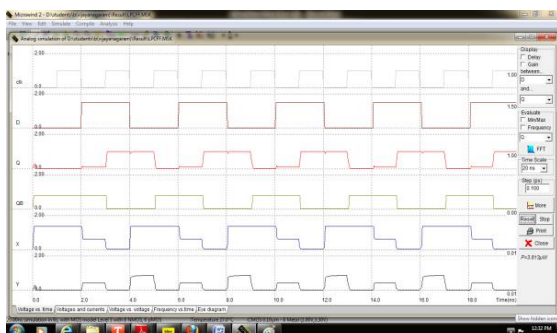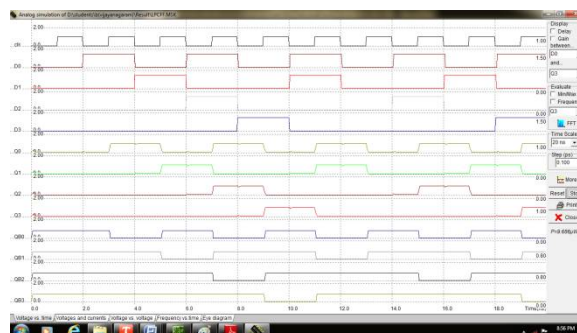

Fig.5 . Power consumed by LPCPFF.

Fig 6. Power consumed by PIPO Shift Register using LPCPFF

TABLE I. COMPARISON OF VARIOUS P-FF DESIGNS.

Parameters	CDMFF	CPSFF	LPCPFF
No. of Transistors	22	19	14
Area	130.8	123.6	107.7
D to Q Delay (ns)	1.13	1.32	1
Avg Power	5.54	4.83	2.87
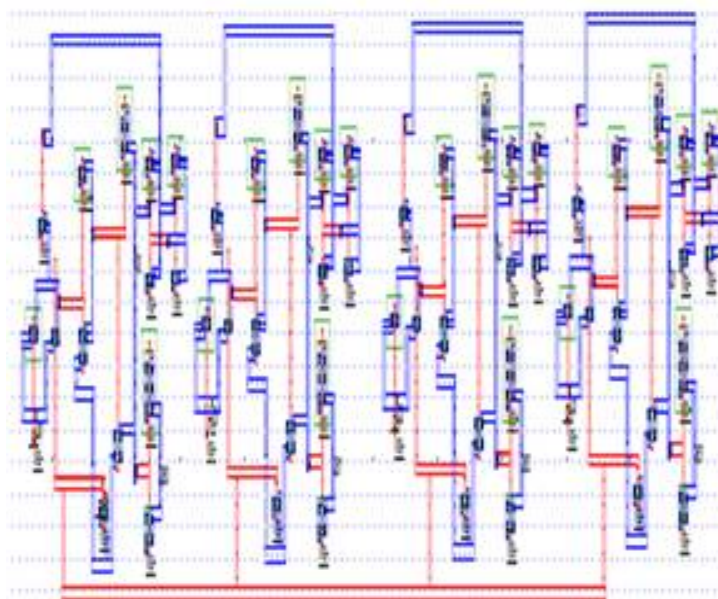
Fig 7. Parallel in Parallel out Shift Register using LPCPFF in Soft Ware Microwind tool

Table 2. Comparison of various Parallel in Parallel out Shift Register designs.

Parameters	PIPO Shift Register Using Cdmff	PIPO Shift Register Using Cpsff	PIPO Shift Register Using Lpcpff
No. of Transistors	88	76	36
Area(um^2)	677.3	623.7	98.2
Average Power (uw)	15.243	12.227	9.686

VII. CONCLUSION

The Low Power Clocked Pass Transistor Flip Flop (LPCPTFF) design in the clocked load resulting in reduction in number of Transistors and Power consumption and Delay. LPCPFF uses less number of transistors compared to CDMFF and CPSFF resulting in reduced area and delay. Power consumption in LPCPFF is reduced by 51.8% compared to CDMFF and 59.4% compared to CPSFF. From the results it is evident that LPCPFF is more power efficient, speed and occupies less area. This flip flop is very much useful in computer systems and in SOC applications.

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