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Design of SAR Logic for Low Power High Speed SAR ADC

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ABSTRACT: Analog-to-digital converters (ADCs) are chief design blocks in today's microelectronic digital communication systems. In simple word, ADC acts as a bridge between the analog and digital worlds. With time the advancement in CMOS technology, more & more signal processing functions are incorporated in the digital field for low cost, low power consumption and dissipation, higher yield, & higher reconfigurability.
It is an essential device whenever data from the analog world, through sensors or transducers, should be digitally processed or when transmitting data between chips through either long-range wireless links or high-speed transmission between chips on the same printed circuit board.
Different types of ADC applications can be found in various systems like data acquisition and data logger systems, bio-medical systems, digital communication systems also imaging, instrumentation systems, etc.
There is a wide variety of different ADC topologies present today based on the requirements of the application. They can be extended from high-speed, low resolution flash converters to the high-resolution, low-speed oversampled and noise shaping delta-sigma ADCs. Among various ADC topologies, we opted to implement a Successive Approximation Register (SAR) ADC that is one of the best suited for low power. We target a resolution of 4-bit and a power consumption of few mill watts. The SAR ADC is implemented in 45 nm CMOS technology with a power supply of 1V.

KEYWORDS: ADC, SAR, CMOS Technology, Low power, High speed.

I. INTRODUCTION

With an advancement in IC fabrication technology, more analog signal processing have been replaced by digital blocks, analog-to-digital converters (ADCs) hold-up an important role in most of the today's advanced electronic systems because most signal with important interest are analog in characteristics and must to be converted to digital form for future signal processing in the digital domain. Analog to Digital Converters (ADCs) are currently adopted in many application fields to improve digital systems, which achieves high degree of performances with respect to analog solutions.
There is a wide variety of different ADC topologies available depending on the requirements of the application. Successive approximation and algorithmic ADCs are one of the best examples. Successive-approximation analog-to-digital converters (SAR-ADCs) have recently become very interesting to study and use in terms of energy efficient, moderate-resolution, moderate-sampling frequency applications due to their minimal active analog circuit needs. In a SAR- ADC, a digital-to-analog converter (internal-DAC) tries to calculate the value of each sample of the input analog signal through successive approximations and comparisons.
Based on the ADC resolution, after a specific number of cycles, the digital word being stored in the successive-approximation register (SAR) corresponds to the analog sample with a specific quantization error. It basically generates one bit per clock cycle, the merits are the low area needed for the implementation. ADCs of this type have good resolutions and quite wide ranges.
SAR type analog-to-digital converters (ADCs) represents a lot of or majority of the ADC market for moderate-to-high-resolution ADCs. SAR ADCs provide up to 5 Msps sampling rates with resolutions from 8 to 16 bits. The SAR architecture allows for high-speed; typically low-power ADCs to be packaged in small form factors for today's high demanding applications. With Microwind 3.5, we have designed 4 bit low power SAR ADC with 45 nm technology.

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II.SAR ADC

The architecture of a successive approximation ADC is shown in Figure 1. It consists of four parts as, a Sample and Hold, a Comparator, a DAC and a successive approximation register (SAR). The successive approximation ADC applies a binary search algorithm to determine the closest digital code for an input signal. When an input signal is applied to the converter, the comparator simply tells whether the input signal is greater or smaller than the DAC output and gives one digital bit at a time starting from the MSB. The SAR stores the produced digital bit and uses the information to alter the DAC output for the next comparison. This operation is repeated until all the bits in the DAC are decided. In order to achieve N-bit resolutions, a successive approximation ADC needs N clock cycles. As the performance is limited by DAC linearity, the calibration of the DAC is required to gain high resolution.

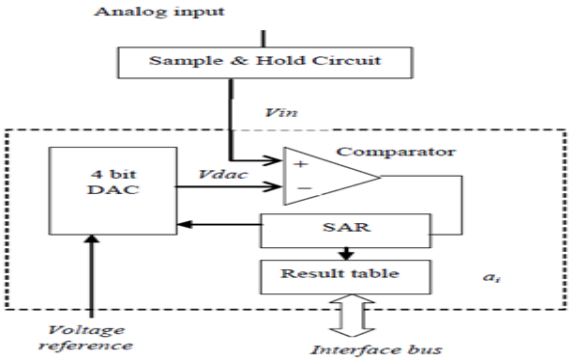

Figure 1: SAR ADC

Because the difference between input signal and reference by turn gets smaller, circuit noise will limit the achievable resolution. A faulty comparator decision means that further iterations will not provide additional information of the input signal.

Successive Approximation Register ADC represents the majority of the ADC market for medium to high resolution. This architecture requires just single comparator; an N-bit SAR ADC will require N comparison clock cycles and will not be ready for the next conversion until the current one is complete.

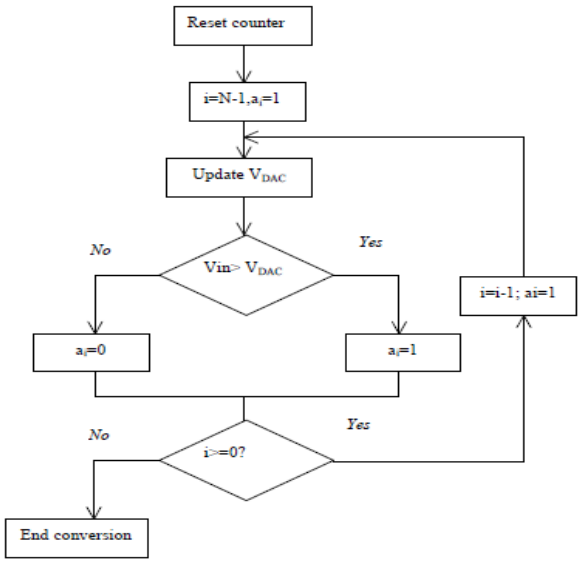

Figure 2: Iterative converter algorithm and a simple implementation

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The SAR-ADC circuit typically consists of four primarily important sub circuits:

A. A sample and hold circuit is needed to acquire the input voltage (V_{in}).

B. An analog voltage comparator compares V_{in} to the output of the internal DAC and gives the output of the comparison to the successive approximation register (SAR).

C. A successive approximation register sub block is designed to provide an approximate digital code of V_{in} to the internal DAC.

D. An internal DAC sub-circuit that provides the comparator with an analog voltage similar to the digital code word of the SAR for comparison with V_{in}.

The SAR is initialized so that the most significant bit (MSB) is activated to a digital 1. This code is fed into the DAC, which then supplies the voltage equivalent of the digital word (Vref/2) to the comparator circuit for comparison with the sampled Vin. If this analog voltage exceeds Vin the comparator makes the SAR to reset this bit; otherwise, the bit remains to 1. Then the next bit is set to 1 and the same test is performed, continuing this binary search until each and every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is ultimately output by the DAC at the end of the conversion (EOC).
Using Microwind and DSCH, we have designed SAR components and analysed their simulation results to design SAR architecture.

III.BLOCK DIAGRAM DESCRIPTION

A. Sample and Hold circuit

Mostly, Sample and hold circuit (SHC) contains a switch and a capacitor. In the tracking mode, while the sampling signal is high and the switch is connected, it tracks down the analog input signal. Then, it holds the value when the sampling signal changes to low in the hold mode.
Sample and hold circuit (SHC) mainly used in ADC. It samples analog input signal & holds value between clock cycles. Stable input is required in many ADC topologies, which is provided by sample and hold circuit. It reduces ADC-error caused by internal ADC delay variations. Sometimes, it referred as Track and Hold (T/H) .The important parameters of S/H circuit are: hold step, signal isolation in hold mode, input signal tracing speed in sample mode, drop rate in hold mode, aperture jitter. The basic schematic of sample and hold circuit is as shown in figure 3.

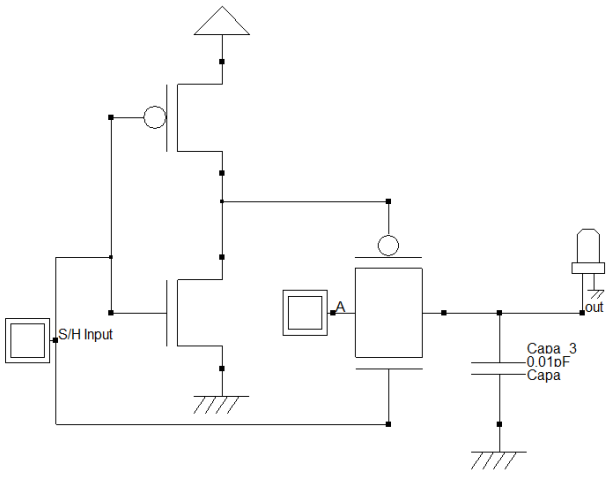

Figure 3: Sample and Hold Circuit

Figures 3 and 4, gives the schematic and physical layout of Sample and Hold Circuit respectively.

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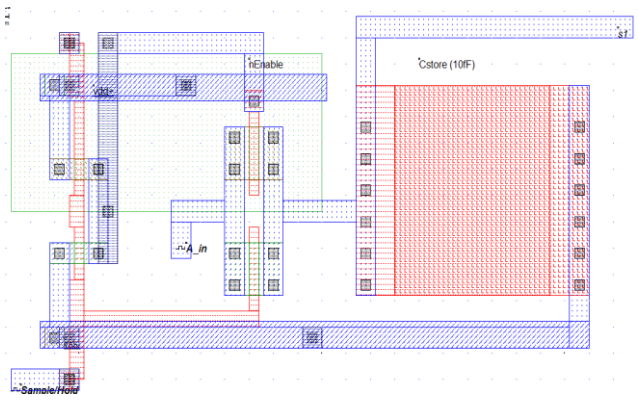

Figure 4: Physical layout of Sample and Hold Circuit

B. Comparator

In order to precisely slice the input data, a reference voltage may be transmitted, on a different signal path, along with the data. In the alternative, the data may be transmitted differentially (an input and its compliment). In the simple case one input to the input reference is DC voltage, say 0.5 V (Vref in fig). When the other input (Vin) goes high above 0.5 V, the output of the buffer changes states (goes from low to high or vice versa).

Vref > Vin out = '1' ➔
Vref < Vin out = '0' ➔

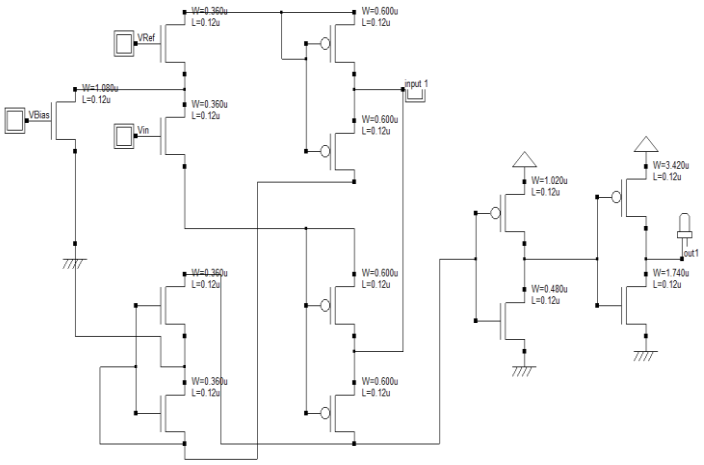

Figure 5: High speed Comparator schematic

Figures 5 and 6, gives the schematic and physical layout of High Speed Comparator respectively.

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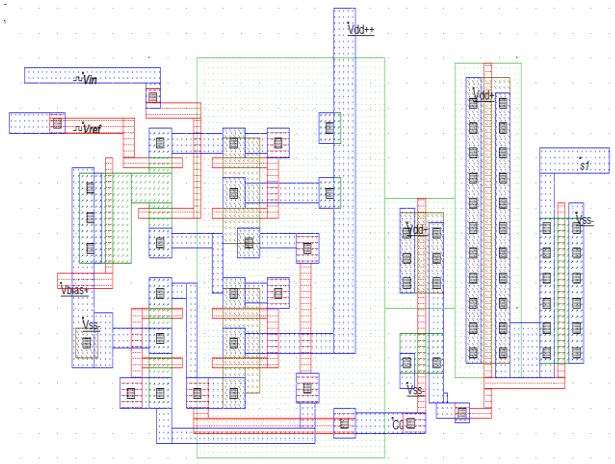

Figure 6: Physical layout High speed comparator

Simulation Parameters

VRef : input with some delayed clock
Vin : random clock between V to 0.1V to 0.9V.
Vbias: Biasing voltage as 0.720 V.
For the transient response the input voltage source (Vin) is a pulse voltage source and the reference voltage source (VRef) is a DC voltage source.
The response is shown below.

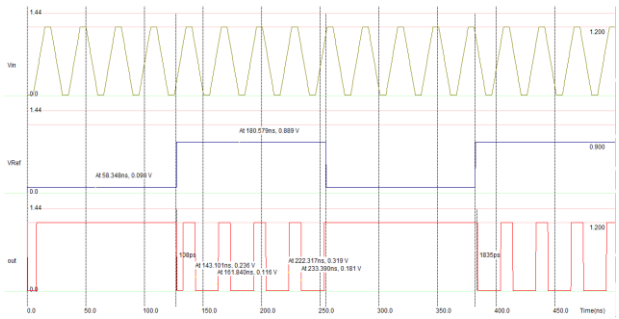

Figure 7: Transient Response of Comparator

Figure 7, shows the transient response of the High Speed Comparator and gives the expected results during simulation process.

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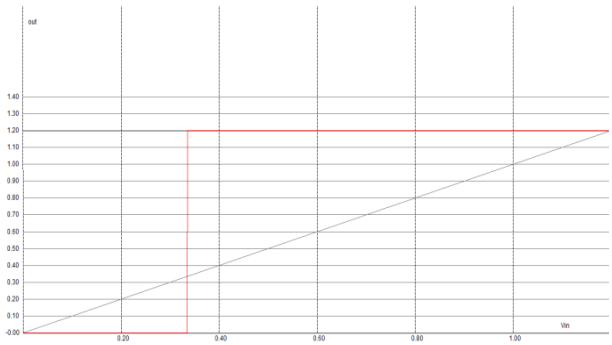

Figure 8: DC Transfer Response of Comparator

Figure 8, shows the DC analysis of the High Speed Comparator. For the DC analysis, both input and reference voltage are taken as DC voltage source. Input voltage is swept from 0V to 1V.

C. SAR Logic Design

In SAR ADC, it sets MSB. Then convert MSB to the corresponding analog output by using DAC. Then guess output will compare with the input. If Vin > half of ADC then it set the bit otherwise test the next bit. SAR ADC is capable of high speed and high resolution. They have low power consumption and low cost. They have medium accuracy and better tradeoffs between speed & cost. They have no pipeline delay.

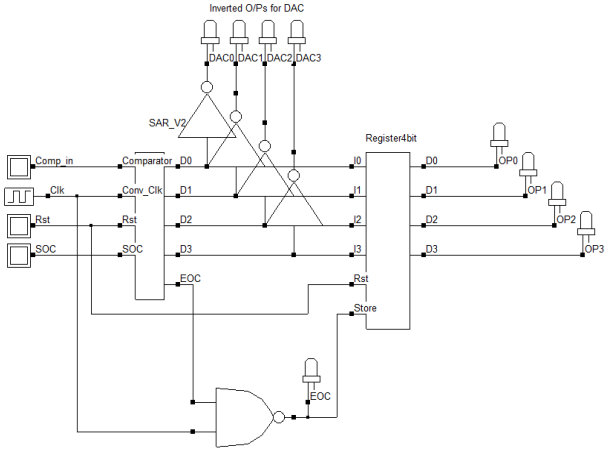

Figure 9: Design of SAR ADC

Figure 9, shows the overall schematic view of SAR ADC when integrated all the parts of it together.

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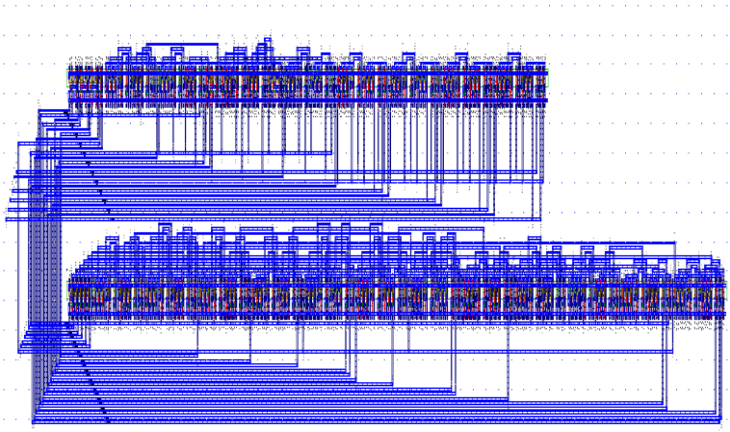

Figure 10: Physical Layout of SAR

Figure 10, is the physical layout representaion of SAR ADC built using Microwind Electronic Design Automation (EDA) Tool

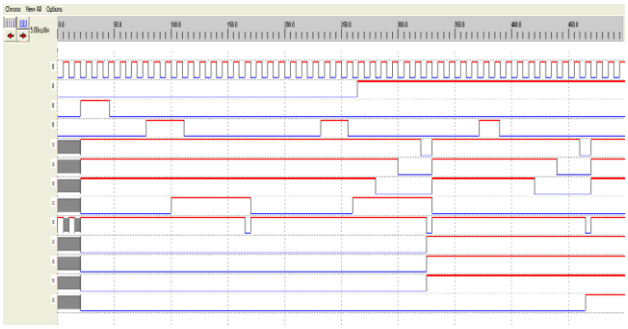

Figure 11: Simulation Results of SAR logic

D. Digital to Analog Converter (DAC)

Resistor ladder networks provide a simple, affordable way to perform digital to analog conversion (DAC). Most passable circuits are the binary weighted ladder and the *R* /2*R* ladder. These two devices will convert digital voltage information to analog, but then also the *R*/2*R* ladder has become the most prevalent because of the network's inherent accuracy.

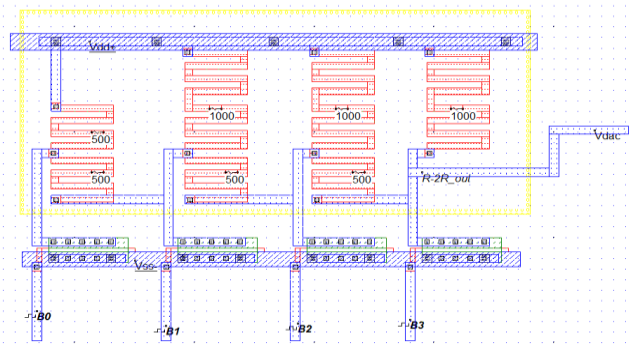

Figure 12: Physical Layout DAC

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After attempting to design the perfect physical layout of 4 bit R-2R ladder DAC, with 45 nm technology and the input given to this converter is from 0000 to 1111. We have achieve the following simulation result as there are in all 16 combinations of input for this DAC, here below in figure, we have shown the behaviour of DAC for the any of the two possible inputs faction from the total of 16 i.e. for 0100 (B3,B2,B1,B0) and 1000 (B3,B2,B1,B0). And after performing simulations using Microwind an Electronic Design Automation (EDA) tool the different performance parameters differs based on the type of DAC that we are using. These performance parameters include power consumption.

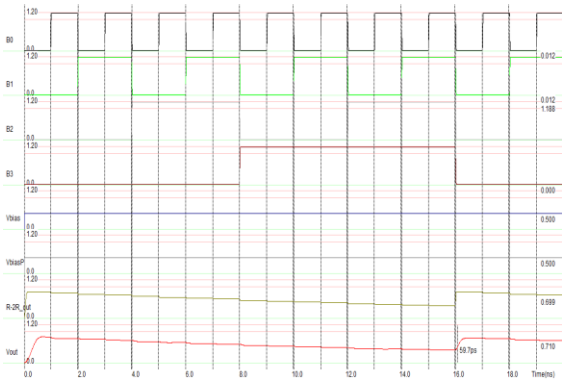

Figure 13: Simulation Results of R2R Based DAC

Figure 13, is the simulation results of R2R Based DAC in Microwind

IV. SAR ARCHITECTURE BASED ADC

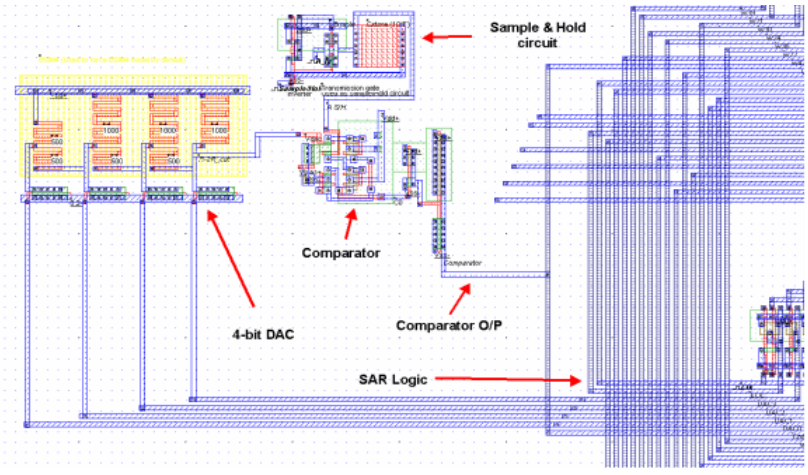

Figure 14: Physical Layout of SAR Based ADC

Figure 14, gives the overall view of SAR Based ADC when integrated together with different components of the block diagram for SAR ADC.

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V. SIMULATION RESULT FOR SAR BASED ADC

Transient Analysis/ Voltage vs. Time:

Analog Input Voltage is Triangle waveform

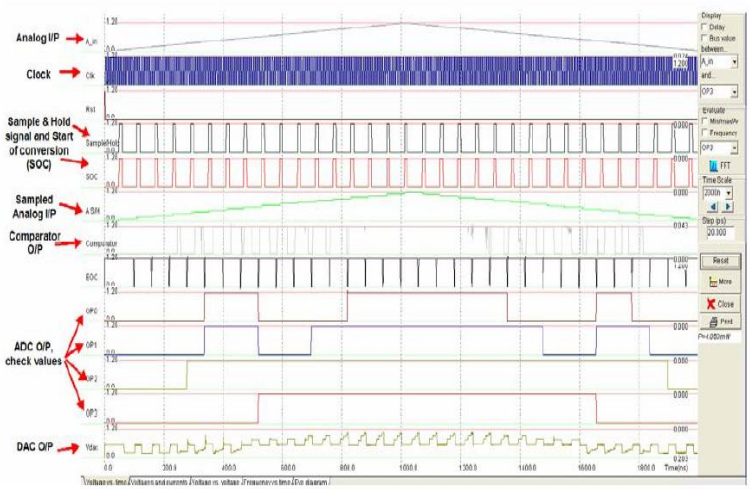

Figure 15: Simulation result of SAR Based ADC

Figure 15, gives the results of simulation for the overall SAR design and also represents the individual block results.

VI.CONCLUSION

In this paper, low power and high speed SAR ADC is proposed and designed in 45 nm CMOS technology. We presented high speed/performance and typically low power consumption design of Successive Approximation Logic for ADC and by using the same we designed ADC architecture whose speed of operation is nearly doubled with more output stability. Also we presented design of High speed CMOS comparator circuit where the Input voltage is swept from 0V to 1 V. An area efficient DAC architecture strictly based on the *R-2R* ladder topology is designed.
On the input side, we designed Sample and Hold circuit with an input as triangular waveform. Stable input is required in many ADC topologies, which is provided by sample and hold circuit. It reduces ADC-error caused by internal ADC delay variations. Finally, we club up all the working modules of the SAR based ADC is designed in 45nm CMOS Technology with 4 bit resolution. It consumes different power values for the various range of input variations, as for triangular waveform as input, it consumes, 4mW for running simulation for 2usec of power. Its rate of conversion is 25Ms/s.

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