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Optimization of Full Adders: A Survey

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ABSTRACT:Full adder is the basic and most common element in the designing of basic arithmetic circuits like Adders, Substractors, Multipliers, and Dividers etc. It is the heart of Arithmetic and Logic Unit. Any change in the adder cell will degrade the overall performance of the designed circuit, so high care must be taken while designing these adder cells.Power consumption and speed are two important but conflicting design aspects; hence a better way to evaluate circuit performance is power delay product (PDP). In this paper The different full adder circuit design are studied and evaluated. Each of these circuit cell exhibits different power consumption, delay and power delay product. This survey paper discussed different technologies for low power.

KEYWORDS: Full Adder, Delay,Low Power,High speed,Power Delay Product,VLSI.

I. INTRODUCTION

Adder is one of the most important components of a CPU (central processing unit). Arithmetic logic unit (ALU), floating-point unit and address generation like cache or memoryaccess unit use it. In addition, Full-adders are important components in other applications such as digital signal processors (DSP) architectures and microprocessors [16]. Arithmetic functions such as 'addition', 'subtraction', 'multiplication' and 'division' are some examples, which use 'adder' as a main building block. As a result, design of a high-performance full-adder is very useful and important. On the other hand, increasing demand for portable equipments such as cellular phones, personal digital assistant (PDA), and notebook personal computer, arises the need of using area and power efficient VLSI circuits. Low-power and high-speed adder cells are used in battery-operation based devices.Designing a circuit of low power has been in challenge from a long time.now it is one of the most important goals of today's CMOS design.

In this paper, The main focus is to compare different CMOS full adder design methodologies.Different techniques have been presented for low power full adder. The structure of the rest of this paper is organized as follows:Basic full adders in section II, related works are shown in section III and finally the conclusion are presented in sectionIV.

II. BASICFULL ADDER

Full Adder is a combinational circuit with three inputs i.e. A, B and C and two outputs i.e. SUM and CARRY. It is one of the basic building blocks of the digital design[8]. The truth table of full adder is shown in table I.

TABLE I.TRUTH TABLE OF FULL ADDER

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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The full-adder functionality can be summarized by the following equation, given the three I-bit input A, B, and Cin, it is desired to generate the two I-bit outputs sum and Cout, where

$$Sum = (A \text{ XOR } B)XOR.Cin \quad (1)$$

$$C_{out}=A.B+C_{in.}(A \text{ XOR } B) \quad (2)$$

III. RELATED WORK

A.Low voltage high performance hybrid full adder

First we introduce Low voltage high performance hybrid full adder .In the proposed structure, the selection of sum and carry outputs are made under the control of input signal C. This signal is not generated internally and therefore provides full output voltage swingswith no additional delay. It has good driving capability and used to drive the multiplexers at the output of the full adder cell[1].The transistors schematic of the proposed design is shown inFig. 1 .

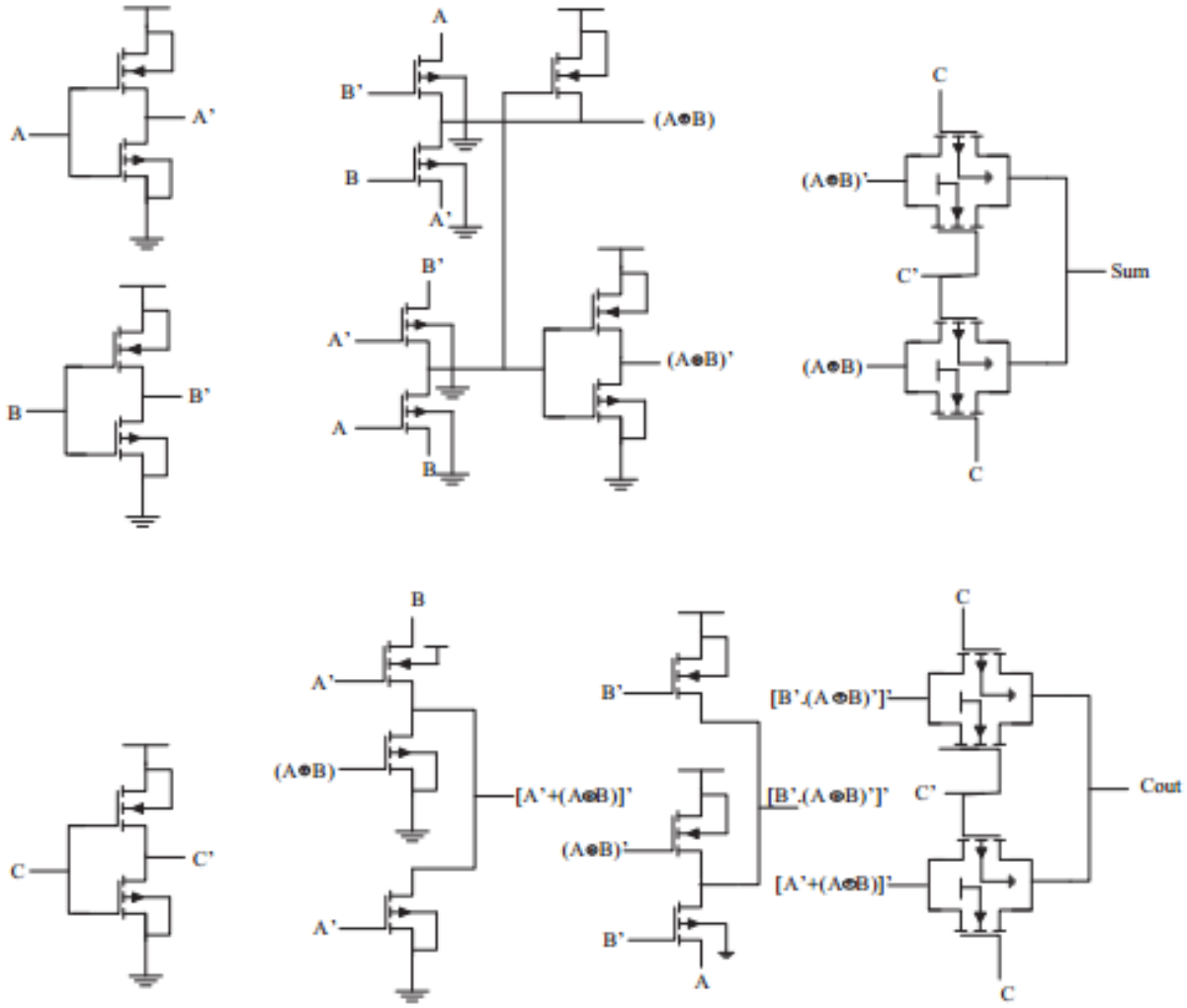

Fig.1Low voltage high performance hybrid full adder [1]

B.a new fault-tolerant full-adder for quantum-dot cellular automata

A novel fault-tolerant full-adder for quantum-dot cellular automata is presented. Quantum-dot cellular automata (QCA) is an emerging technology and a possible alternative for semiconductor transistor basedtechnologies [2].The novel proposed design for fault-tolerant full-adder is shown in Fig.2 .

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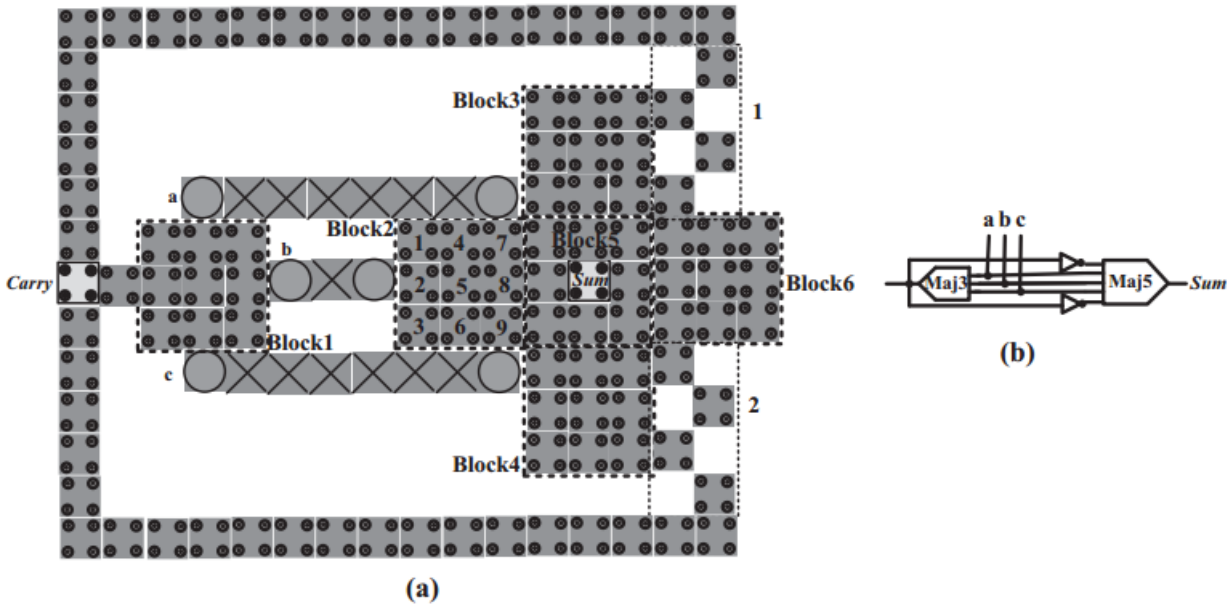

Fig. 2.(a) Layout of the proposed fault-tolerant full-adder. (b) Schematic of new QCA fault-tolerant full-adder [2]

C.A Novel Quaternary Full Adder Cell Based on Nanotechnology

This paper presents a novel high performance quaternary full adder cell based on carbon nanotube field effect transistor (CNTFET)[3]. The proposed Quaternary full adder is designed in multiple valued voltage mode. CNTFET is a promising candidate for replacing MOSFET with some useful properties, such as the capability of having the desired threshold voltageby regulating the diameters of the nanotubes, which make them very appropriate for voltage mode multiple threshold circuits design.The proposed quaternary full adder is shown in Fig. 3.

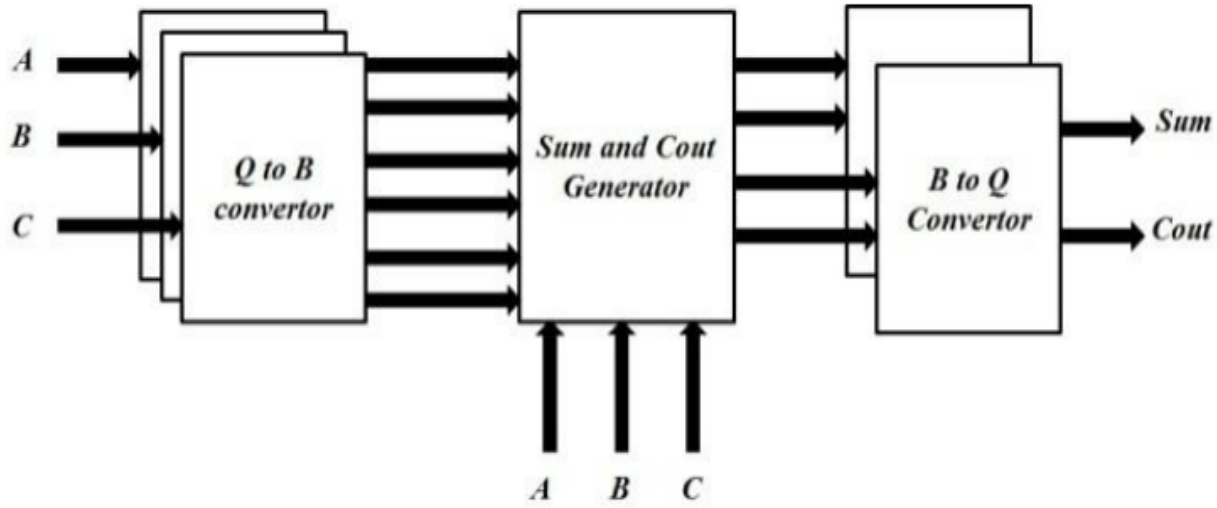

Fig. 3 The proposed quaternary full adder (CQFA) [3]

D.Ultra high speed full adders

In this section Two novel 1-bit Full adder cells based on majority function and the similarity between the minterms of the $\overline{Cout}$ and Sum functions, are introduced [4].two Ultra high speed full adders is shown in fig.4.

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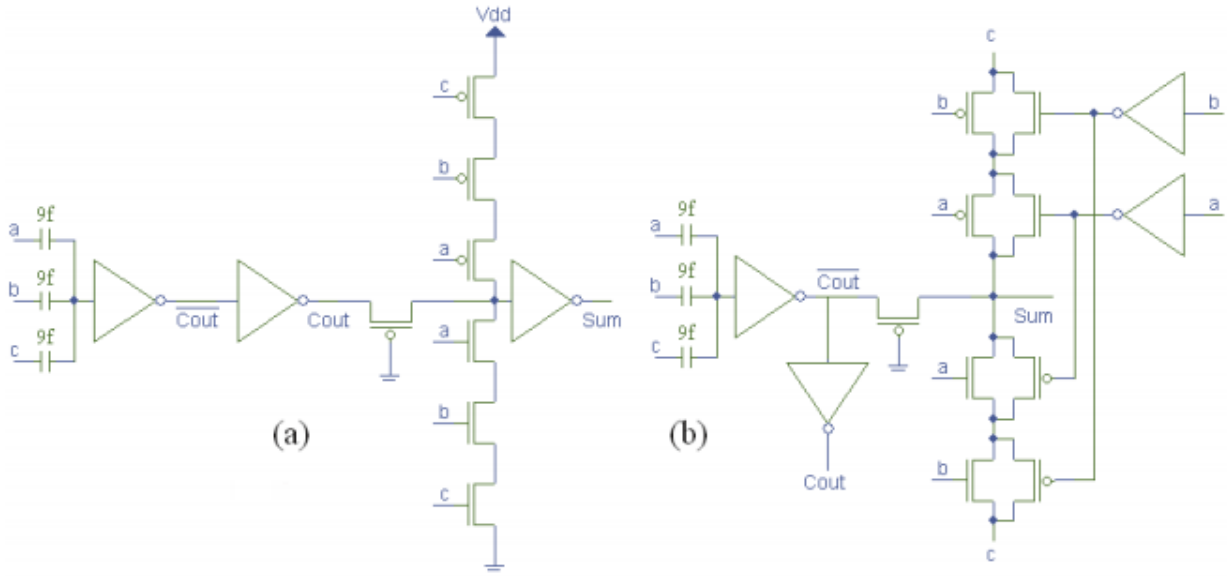

Fig. 4two ultra high speed full adder cell [4]

E.Full Adder based on XNOR-XNOR hybrid CMOS design

In this section an area efficient design for highly compact, low power 1-Bit Full adder is presented [5]. The proposed Full Adder is based on XNOR-XNOR hybrid CMOS design styles with 32nm and 120nm CMOS process technologies. The XNOR gates used in the design are implemented using 3Mosfets only along withproper W/L ratio among them.The new Full adder successfully operates at low voltage upto 0.35V and operating frequency range between 2MHz to 400MHz with excellent linearity, signal integrity and driving capability.Schematic of Proposed PTL based 3T XNOR gate is shown in fig.5.

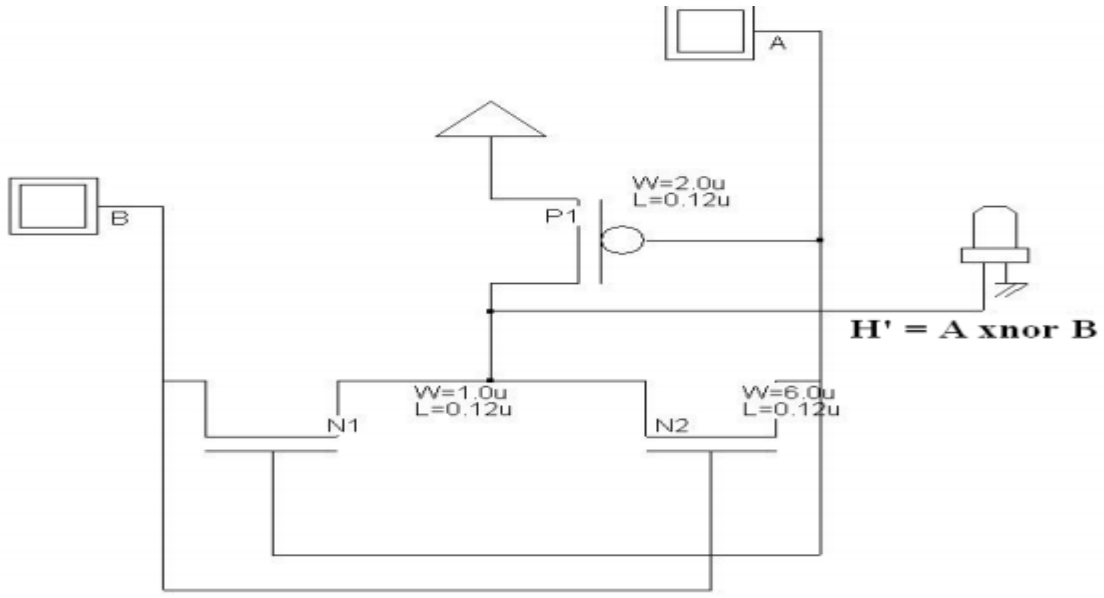

Fig. 5 Schematic of Proposed PTL based 3T XNOR gate [5]

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F. 9 transistor 1-bit full adder

In this section we propose a new 9 transistor 1-bit full adder. The proposed circuit performs efficiently in subthreshold region to employ in ultra low power applications [6].This is shown in Fig.6.

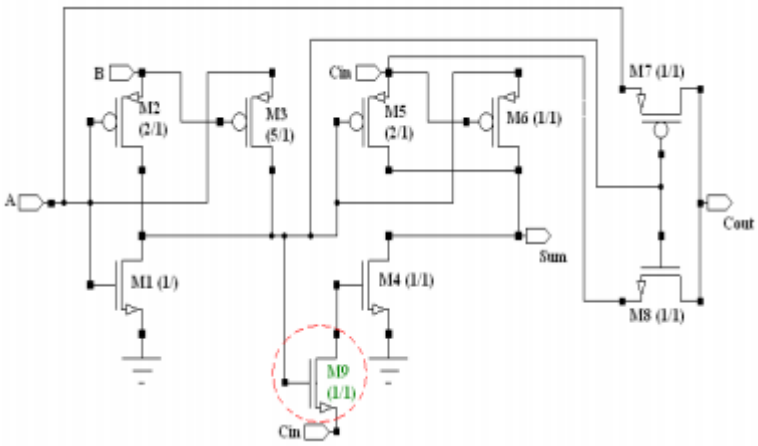

Fig. 6Proposed 1-bit 9T Full Adder [6]

G.**Full Adder Cell with the GDI Technique Based on 0.18µm CMOS Technology**

The Gate Diffusion Input (GDI) technique has been used for the simultaneous generation of XOR and XNOR functions [7]. Fourteen states of the arts 1-bit full adders and one proposed full adder are simulated with HSPICE using 0.18µm CMOS Technology at 1.8v supply voltage.As a result, the full adder works at the 100 MHz speed with 0.78 µw power consumption.This is shown in Fig.7.

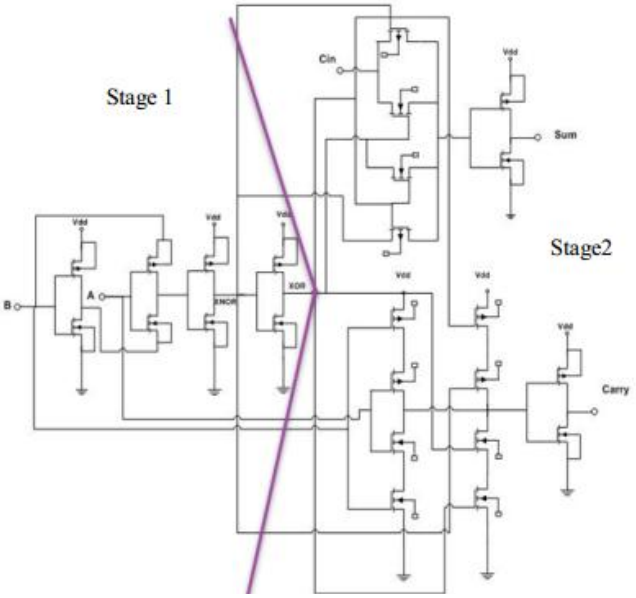

Fig. 7The proposed full adder cell with GDI technique [7]

H.SERF Full Adder

Static Energy Recovery Full adder (SERF) is a 10 transistor (10T) adder shown in Fig. 8 .The circuit is claimed to be extremely low power consuming because it does not contain direct path to the ground [8]. The elimination of the path to he ground reduces the total power consumption by reducing the short circuit power consumption..This is shown in Fig.8.

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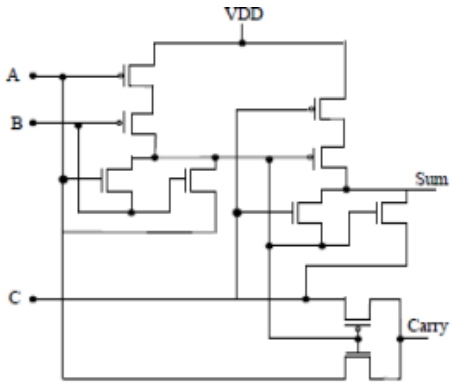

Fig. 8 SERF Full Adder [8]

I.A new design using PT and TG logic

A new design using PT and TG logic is proposed here which requires 16 transistors The lesser number of transistor realization is possible using pass transistor logic for Sum[9] .The full adder carry designed using transmission gate consists of PMOS and NMOS connected in parallel controlled by the gate. The design proposed will have less area and a better power delay product..This is shown in Fig.9 and fig.10.

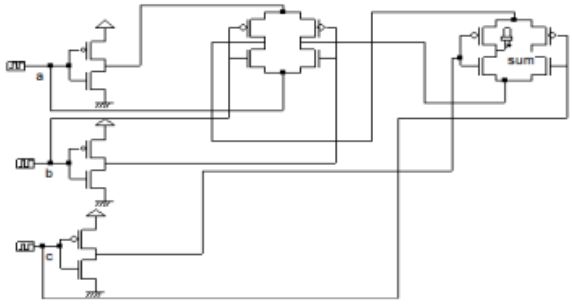

Fig. 9 Sum Function Circuit of new design using PT and TG logic [9]

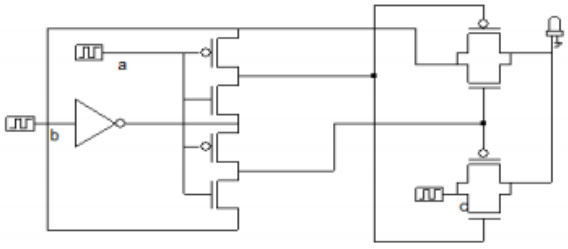

Fig. 10Carry Function Circuit [9]

J.Low Power Dynamic Full Adder Cell Based on Majority Function

full adder cell is based on Majority Function. The Majority Function is a logic circuit that performs a Majority vote to determine the output of the circuit[10].Although conventional dynamic style suffers from the excessive power dissipation, this new design enjoys low power and high performance.This is shown in Fig.11.

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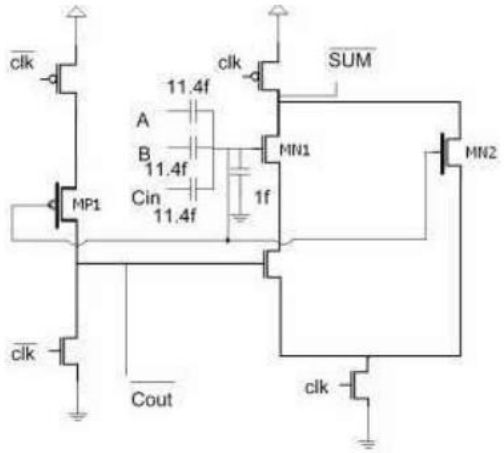

Fig. 11full adder based on Majority function [10]

K.16T FULL ADDER

The circuit consists of low power XOR and XNOR gates, pass transistors and transmission gates [11]. The adder offers higher speed and lower power consumption than other implementations of the full adder.16-T full adder is shown in Fig .12.the average power and Average Delay are low for 16T Full Adder.

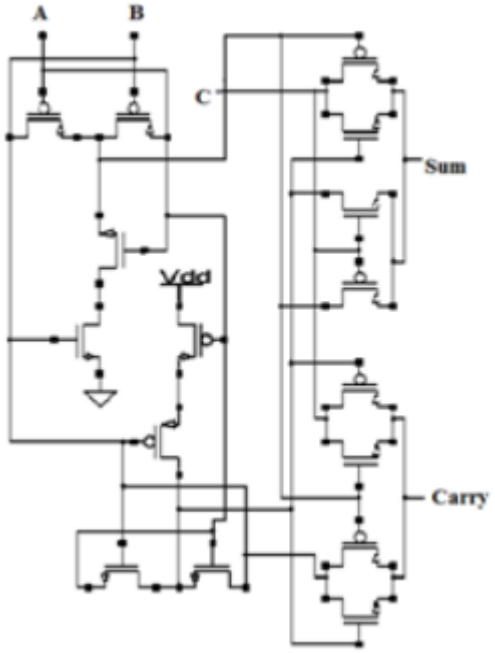

Fig. 12 full adder with 16T [11]

L.Full Adder Cell by Combining Common Digital Gates and Majority Function

The proposed Full-adders include two three-inputNAND and NOR gates [12]. The two adders differ in the designing of these gates.This is shown in Fig.13

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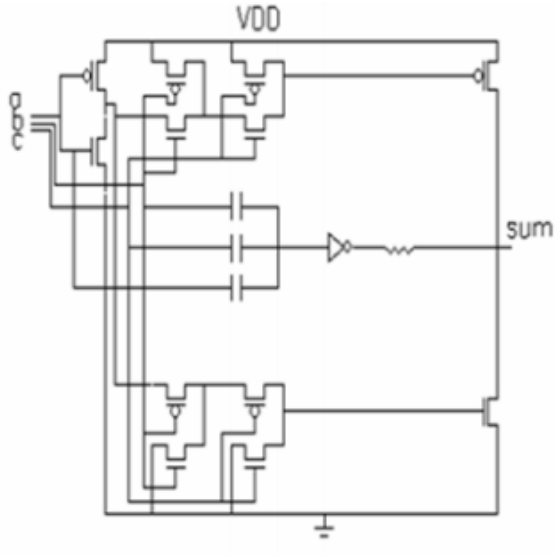

Fig. 13Full adder cell with PT gates [12]

M.An energy efficient full adder cell for low voltage

This full adder works based on majority function and MOS capacitors. because of the simple structure of the proposed design and reduced transistor counts, this full adder is very low power[13].This is shown in Fig.14.

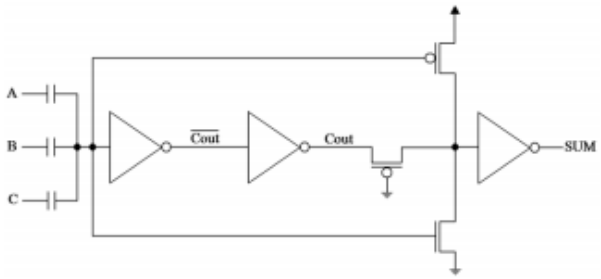

Fig. 14energy efficient full adder cell for low voltage [13]

N.Performance/Power/Area Efficient, Reliable Full Adder Design

In this section hybrid full adder topology based on D3L design philosophy is introduced [14]. The design brings together the speed advantages of dynamic design with the reliability and robustness of static CMOS design. The proposed adder is found to perform up to 2 times as fast as competing designs, while providing second highest noise margins amongst all the adders. The circuit is found to be one of the most reliable when included in buildingbigger circuits.This is shown in Fig.15 .

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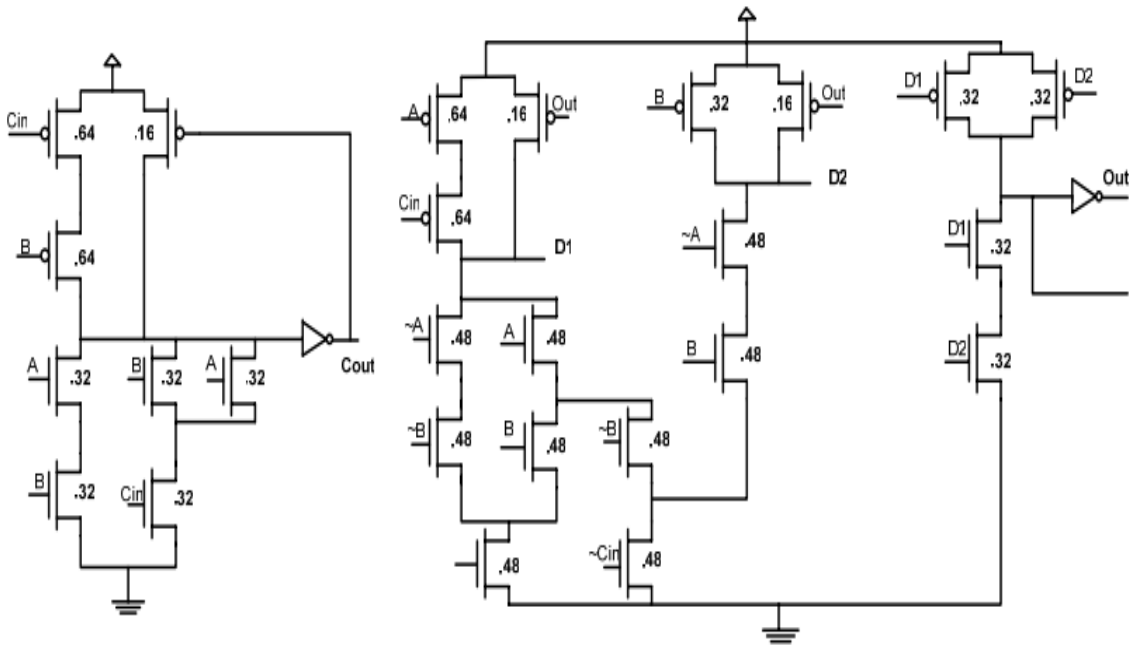

Fig. 15Hybrid D3L Full Adder Circuit [14]

O.High-Performance CMOS 1 Bit Full-Adder Cell

In this section we introduce a low complexity full adder design featuring higher computing speed, lower operating voltage, and lower energy consumption [15]. it uses the low power designs of the XOR and AND gates pass transistors and transmission gates, simulation results compar-ing the conventional cell to the standard implementation show its superiority diff erent circuit structures and input patterns are used for simulation. Energy saving up to 40% is achieved in addition.This is shown in Fig.16.

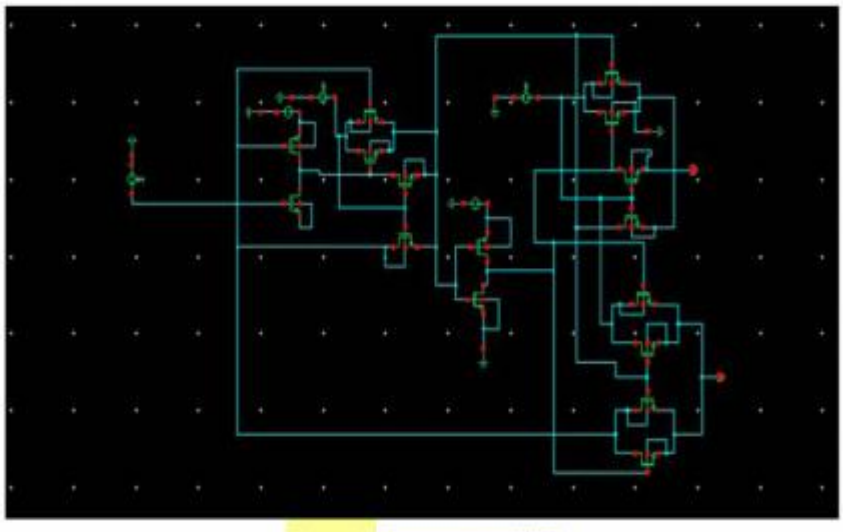

Fig. 16High-Performance CMOS 1 Bit Full-Adder Cell [15]

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The results of the comparative study are shown in table II.

Table II.comparison of previous full adders

Adders	power	delay	Power delay product(PDP)	Supply voltage	technology
Low voltage high performance hybrid full adder[1]	4.938 µW	38.54 ps	190.310 aj	1.2V	90nm
A Novel Quaternary Full Adder Cell Based on Nanotechnology [3]	7.5374 µw	112.76 ps	8.4959 fj	0.9 V	32nm
Ultra high speed full adders[4]	1.8724 µw	98.496 ps	1.8442 fj	0.8 V	0.18µm
9 transistor 1-bit full adder [6]	1.8 µw	-------	0.8 fj	0.25 V	32nm
Full Adder Cell with the GDI Technique Based on 0.18µm CMOS Technology [7]	0.78 µw	50 ns	39 aj	1.8 V	0.18µm
Low Power Dynamic Full Adder Cell Based on Majority Function[10]	1.1855 µw	0.1663 ns	0.1971 fj	1.8 V	0.18µm
16T FULL ADDER[11]	0.154 µw	0.0607 ns	0.935 fj	-------	0.18µm
Full Adder Cell by Combining Common Digital Gates and Majority Function [12]	4.14 w	4.36 s	1.81 j	1.8 V	0.18µm
An energy efficient full adder cell for low voltage [13]	4.065 µw	0.158 ns	0.6423 fj	1.8 V	0.18µm
Performance/Power/Area Efficient, Reliable Full Adder Design [14]	15.132 µw	80.04 ps	--------	1.2V	0.13 µm
High-Performance CMOS 1 Bit Full-Adder Cell [15]	70.21 w	97.53 ps	2.03 fj	1.8 V	----------

IV.CONCLUSION

In this paper, several types of full adder cell designs have been surveyed from the most recent published research paper. The comparison of full adder cells with each other in term of power, delay, supply voltage and is presented. Different logics are used in this paper to build the full adder to reduce the power, delay, power delay product and transistor count. A widely comparison to the state of the art designs cited in the VLSI literature illustrates a significant improvement in terms of power dissipation and PowerDelay product (PDP) parameter.

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