ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 1, January 2016

A High Speed Low Power CMOS Comparator for Pipeline ADC in 180nm Technology

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ABSTRACT: This paper describes the design of CMOS comparator for low power and high speed application of pipeline ADC in 180nm technology. This paper illustrates the comparison between the proposed comparator and the existing comparator. This comparator incorporates the back to back connected inverters (i.e latch) and a fully differential amplifier. This comparator has a low static power consumption and has a high operating speed of MHz's. This comparator requires only one clock cycle to trigger its transition from one phase to another. The comparator is designed and its functionality is verified in the cadence design environment. It is implemented in 180nm technology.

KEYWORDS: Differential Amplifier, Latch, buffers, Dynamic comparator.

I. INTRODUCTION

ADC is a key component of analog and digital interface system. The pipeline ADC is a promising topology for high speed data conversion with compact area and efficient power dissipation. The Pipelined ADC s are widely used in areas of wireless communications, digital subscriber line analog front ends, CCD imaging digitizers, Studio Cameras, ultra sound monitors and many other high speed applications. It is used in pipeline stages to increase the power efficiency since they consume no DC current. Pipelined ADCs find their use in high speed and moderate resolutions applications. The comparator used in pipeline ADC is a dynamic latch based comparator. The comparator has a n channel differential pair with back to back connected inverters as load. The given comparator has very low offsets of the order of few tens of mill volts at maximum. The Comparator consumes static power of only few hundred nano-watts and operates at frequencies of well above 100MHz. The track-and-latch-stage reduces the total number of gain stages even when good resolution is needed.

This paper describes the design and implementation of dynamic track and latch comparator for its further implication in pipelined ADC. It involves the fully differential amplifier which nullifies noise at the input of the ADC. It also involves the latch circuitry which stores the differential output during the phases of the dynamic latch comparator. The basic principle of operation to use the comparator principle to determine if a particular bit of binary number output need to turn on or not.

II. FULLY DIFFERENTIAL AMPLIFIER

A differential amplifier is a circuit that can accept two input signals and amplify the difference between those input signals. It provides high voltage gain and high common mode rejection ratio. It requires very low input bias current, very low offset voltage and very high input.

The differential amplifier has been shown in figure 2. MOSFET M1 and M2 from fig2 formed differential amplifier pair. MOSFET M5 is a current sink which provides bias current to the amplifier. MOSFET M3 and M4 together form a current mirror .Assuming that all transistors are in saturation region. The Bulk of all transistors connected to their sources. The current flowing through transistor M5 is divided into two equal parts and flows through M1, M3 and M2, M4 respectively. Transistor M3, M4 connects to the VDD supply, whereas transistor M5 connected to VSS.

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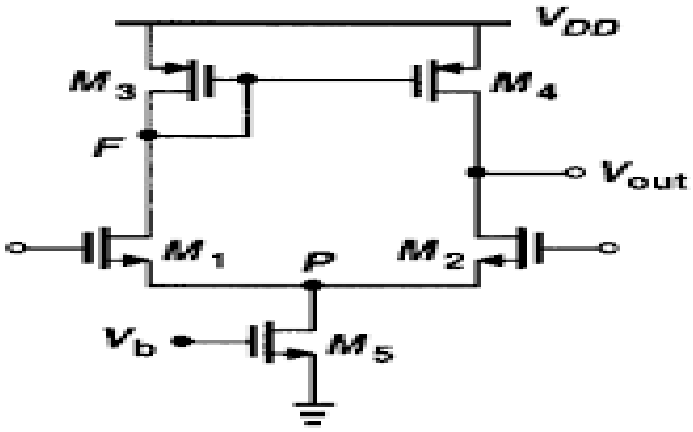

Fig 2: Fully Differential Pair Amplifier

The differential amplifier output can be described as

$$V_{out} = A(V_{in+} - V_{in-})$$

where A is the gain of the amplifier. [1]

III. DYNAMIC TRACK AND LATCH COMPARATOR

This comparator consists of two cross-coupled inverters controlled by a latch signal. When latch is low, V_{out+} and V_{out-} will be pulled to high voltage, the output of comparator would be locked. When latch is high, the comparator come into being a couple of two reversers that are connected end to end. The comparator during the phase1 regenerates recursively the output based on the unbalanced differential inputs and the RS latch takes in new value. The comparator during the phase2 gives a low at its output always and the RS latch remains unchanged.

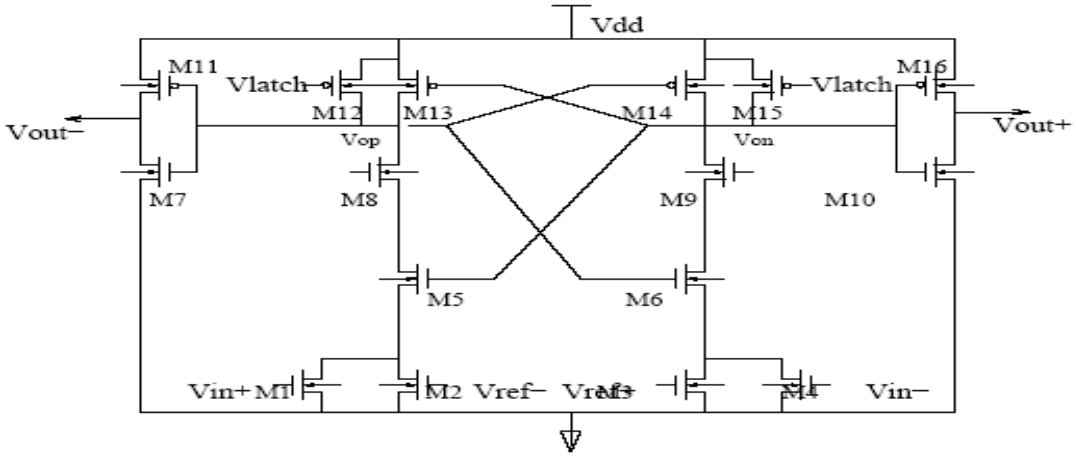

Fig 3: Dynamic Track and Latch Comparator

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IV. SIMULATION RESULTS

The simulation of the schematic in fig 3 is done in cadence tools environment. The simulation of the dynamic Track and latch circuit is done on the test bench of the schematic as shown in fig 4.The simulation result shown in fig5 depicts the transient response of dynamic track and latch circuit.

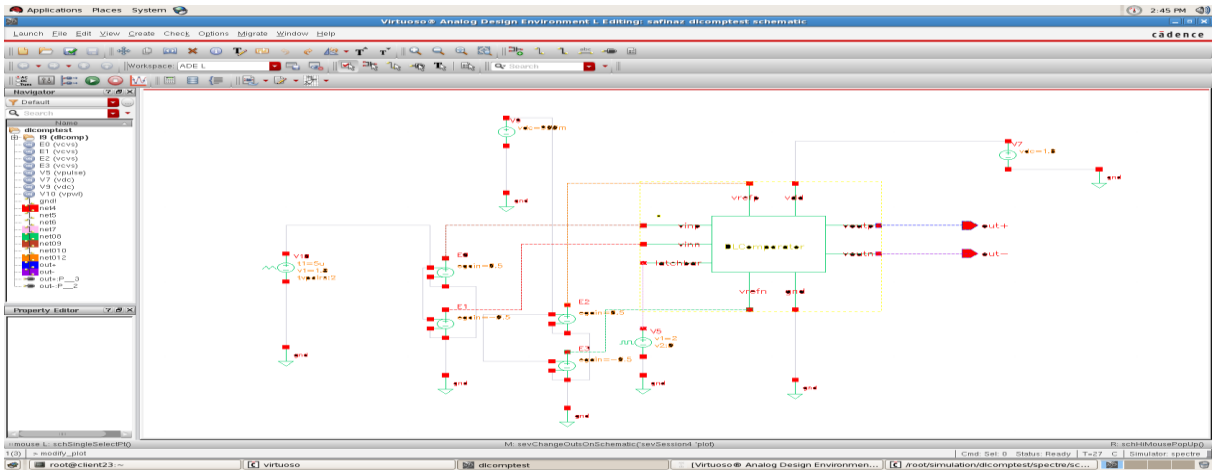

Fig 4: Dynamic Comparator test bench schematic

The two differential input signals when fed to the dynamic Track and Latch Comparator in the fig 5 the output gets pre-charged to high voltage 1v whenever the latch bar input is low. The comparator generates the compared output of both the signals with respect to the reference signals whenever the latch bar input is high [2].

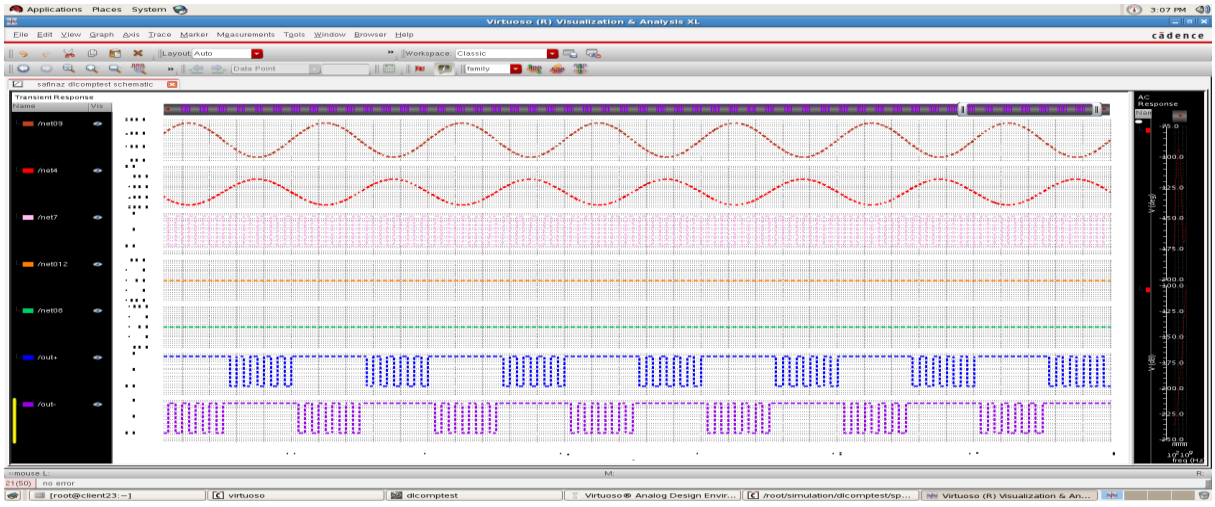

Fig 5: Transient Response of Dynamic Track and Latch comparator

The fig 6 shown below represents the comparator output operation in both the phases. When the V_{latch} is high, the upper pre-charging switches open and stop pre-charging, the lower NMOS discharging circuit starts its operation. The comparison is made by comparing the rate of discharging the output node(V_{on} & V_{op}).

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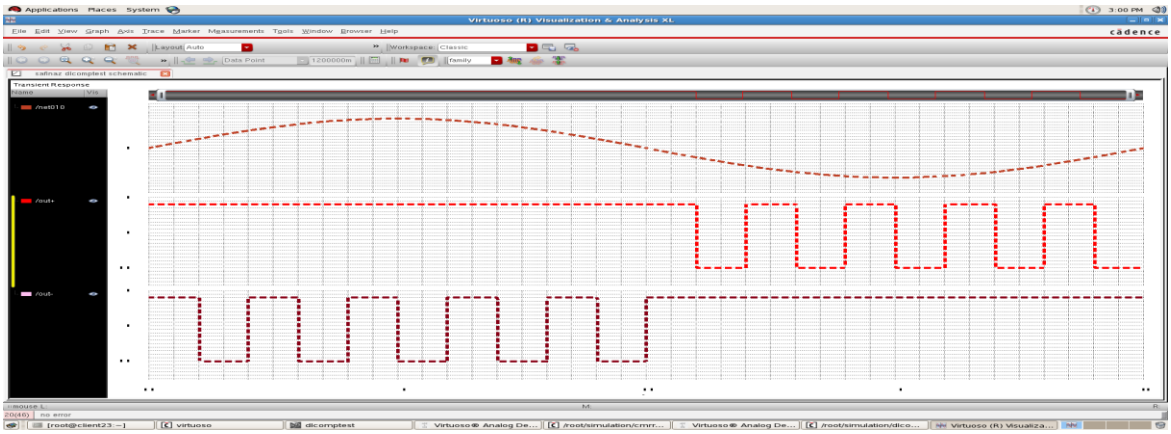

Fig 6: Comparator operation in both the phases of comparator.

The input sinusoidal signal of 500mV with 1MHz frequency when fed to the basic comparator which involves the Operational amplifier gives the square wave output as shown in fig 8.The test bench of the comparator shown in fig 7 gives the simulation result shown in fig8.

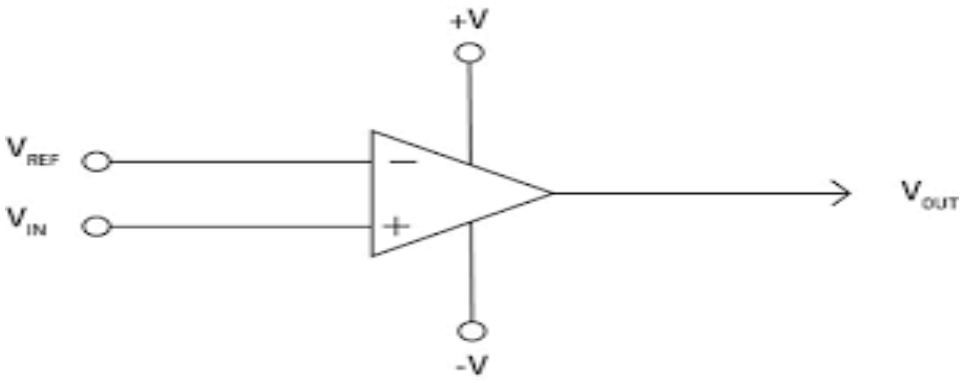

Fig 7: Basic Comparator using Operational Amplifier

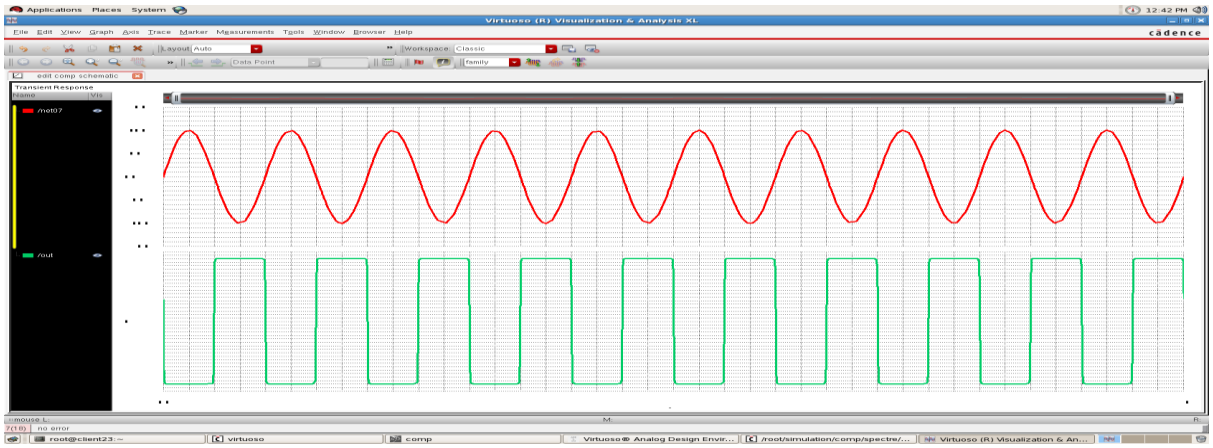

Fig 8: Comparator using Operational Amplifier Simulation

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The fig 9 illustrates the difference between the comparator and dynamic track and latch comparator. The Comparator involves the operational amplifier whereas the proposed comparator uses the track and latch circuit with fully differential amplifier. The proposed comparator works at higher operating speeds than the existing comparator which involves operational amplifier.

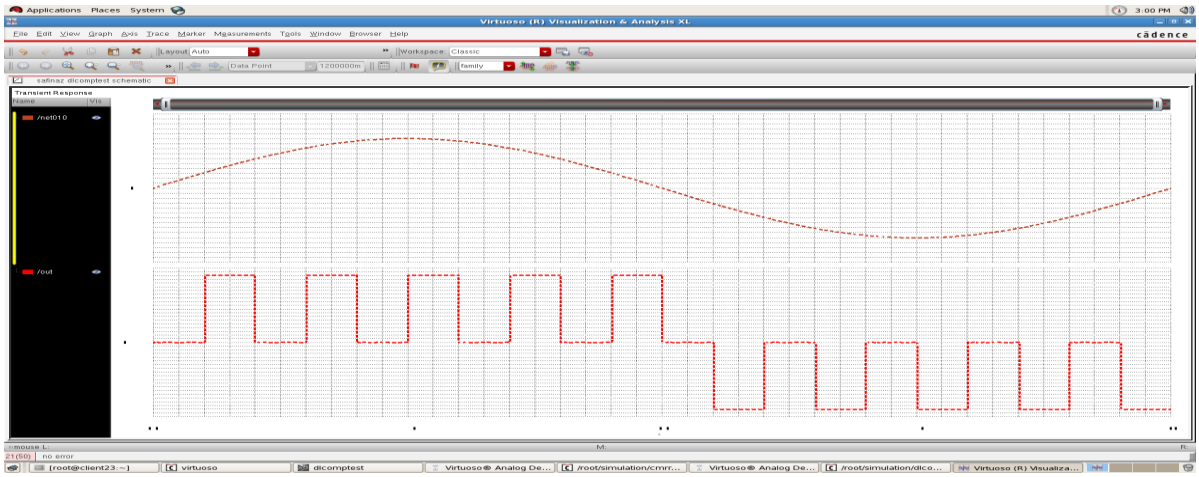

Fig 9: Proposed Comparator output

V.CONCLUSION

The design and implementation of dynamic track and latch comparator for use in pipeline ADC has been done in the cadence environment and the results are shown. The results obtained meet the expected functionality of the comparator. The paper has also presented the difference between the existing comparator and the proposed comparator with the computed results mentioned in the paper.

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