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A Solar-Wind Energy Source Interface with the Public Grid: Design and Implementation

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ABSTRACT: The challenges of interfacing the renewable energy sources with the public grid, are the higher injected power, inverter switches overheating, the misalignment switching instants of the inverter and synchronizing the inverter output with the public grid. This paper presents a complete design for a current link PWM for a renewable energy sources connected to the grid. A battery bank in parallel with a full wave rectifier are used for driving the inverter. An appropriate value of the DC link inductor has been calculated and implemented. A power MOSFTs CSI is designed and implemented. The proposed circuits provide an efficient electrical isolation between both digital and the power sides. The CSI has driven by a space vector PWM. Constraint of the CSI current continuity is hardware fulfilled using the inverter drive circuits. A temperature compensator has been designed for reducing the ON times of the PWM when the MOSFET temperature rises. Interface circuits for adapting both the DC link and the mains line voltages as well as the DC link current to the logic level have been designed and implemented.

KEYWORDS: SV-PWM, CSI, Synchronization, Microcontroller, Protection, Public Grid.

I. INTRODUCTION

Energy is vital input for sustainable development and economic growth for any country. Electrical energy is considered a most convenient form of energy sources in rural and urban areas. In many parts of the world there is growing awareness that renewable energy has an important role to play in the provision of social amenities such as potable water and electricity [1]. In the past few years the photovoltaic and wind power generation have been increased significantly. Both energy flow and operation characteristics of wind / PV hybrid power systems are analyzed to achieve its optimal and reliable operation [2]. A PV system that is independent of the grid typically consists of a battery bank and charge controller. This type of system, can be used to provide direct-current (DC) power, or with an inverter, can be used to supply power for alternating current (AC) loads. A PV system tied to the utility grid [3], typically consists of one or more PV modules connected to an inverter (or power conditioner) that inverts the system's DC output to an AC, which is compatible with the utility grid. One can include batteries in the system to provide reliable back-up power in case your utility experiences power outage [4]. The advances in semiconductor fabrication technology have made it possible to significantly improve not only voltage and current capabilities but also the switching speed. As far as efficiency is concerned, the static power converter is the best of class for most applications. Safe operation of such

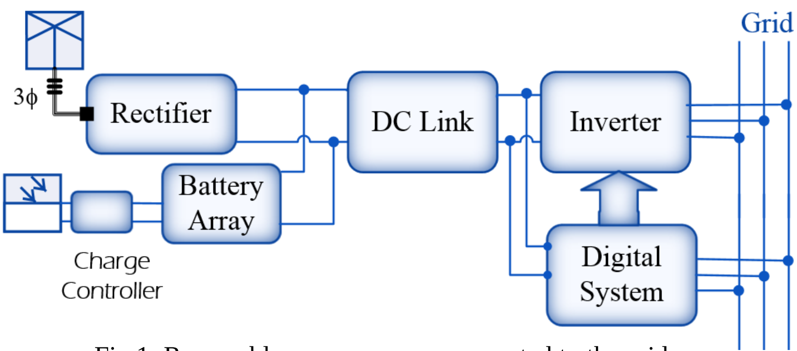

Fig.1: Renewable energy source connected to the grid

converters is one of the most important factors where the unpredicted digital hanging, over current, and then over heating of the converter components can simply happen [5]. Simplified block diagram of the proposed solar-wind

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energy converter connected to public grid is shown in F.g:1. In this work we will further refer to the output points of the battery bank and the rectifier as the DC link**.** In addition to the coupling inductor of the DC link, the proposed interface configured from two main stages, the inverter switches with their gate drive circuits including thermal compensation, power supply of the digital system. The second stage is the digital system of fig.1. Exploring the interface stages are presented in the next paragraphs:

II. FULLY CONTROLLED INVERTER OF THE PPROPOSED INTERFACE

Either the battery bank or the uncontrolled diodes rectifiers are often supplies the inverter with an uncontrolled voltage according to the output of the solar cell or the wind turbine respectively. Advantages of the proposed scheme are the high power factor of the electric generator and low cost of such rectifiers as well as the high reliability [6]. In this work a 3-phase current link SV-PWM inverter is presented by [7]. A 2kW, 10A and 220V rated values of the inverter has been designed and experimentally tested. A simple block diagram of the current link inverter is shown in Fig.2. The stages of the inverter circuits are designed and discussed as follows:

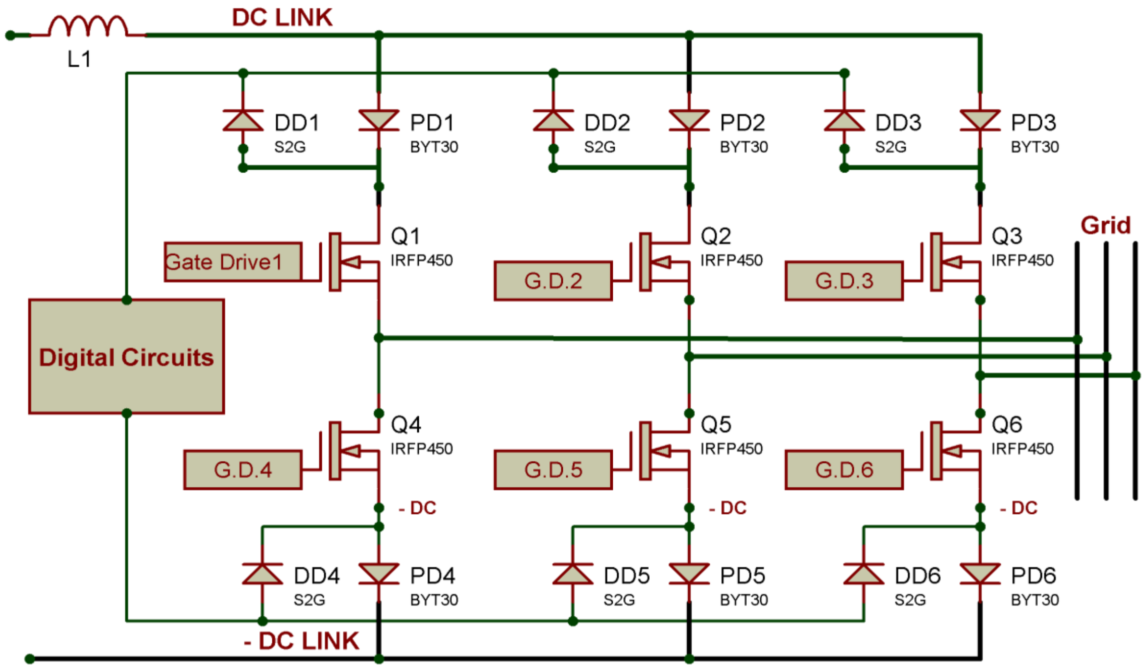

Fig.2: Simplified diagram of the proposed interface

a. DC Filter (Inductor)

The inductor of the DC link is used to limit the current ripple and to maintain the DC current almost constant during each cell time of the PWM inverter. The inductance value of the inductor can be estimated according to the allowable peak to peak current ripple $I_{r,pp}$ through the inductor, the voltage of the DC link, and the switching frequency of the PWM inverter. The inductor of the DC link has been designed based on the allowable peak-to-peak current ripple $I_{r,pp}$ and the maximum rms current $I_{MAX,rms}$ through it, the voltage of the DC link and the switching frequency of the inverter. The rated values of the proposed converter are *10 A rms*, *311V DC* voltage and *4.5 kHz* switching frequency of the inverter. The permissible ripple current peak-to-peak is 10% of the rated rms current $I_{,rms}$. The required inductor value for an acceptable current ripple is then given by:

$$L_1 = \frac{\Psi}{I_{r,PP}} \tag{3}$$

Where the Ψ is the linkage flux of L_{dc}, given by:

$$\Psi = V_{dc}\delta \approx 16.172\, V.ms \tag{4}$$

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where δ is the ON time of the PWM. An allowable ripple current 1A for instance, yields an L_{dc} of 16.172mH. The maximum energy E can be stored in the inductor is then:

$$E = \frac{1}{2} L_{dc} I_{PP}^2 = 0.808 \quad J \tag{5}$$

The size and the shape of the inductor are chosen based on the E value.

b. Six DC supplies for the gate drive circuits

Using the inverter DC link, six DC supplies have been provided in the gate drive circuits. Each DC supply is built using three series resistors in series with a diode, zener diode, and a capacitor as shown on the upper side of Fig.3. This circuit provides a stable DC voltage along the range of 100V up to 400V of the DC link. Compared to the classical DC

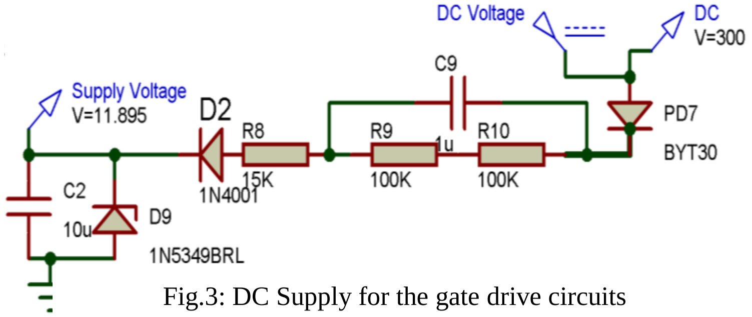

Fig.3: DC Supply for the gate drive circuits

supplies (consisting of a step-down transformer, a full wave rectifier, a smoothing capacitor and a 78xx regulator), the proposed DC supplies are more efficient ,small sized, and lower cost. Furthermore, in order to perform the experimental tests in a safe way on the gate drive circuits an additional (temporary) connection for the DC supply is provided 48V terminal in Fig.4.

c. Isolation circuits

The drive circuits interface the digital control with the power sides of the inverter. For such circuits an appropriate isolation between the two (digital and power) levels should be provided . The isolation can be accomplished using either pulse transformers or opto-couplers. Although the pulse transformers provide a quite good galvanic separation,

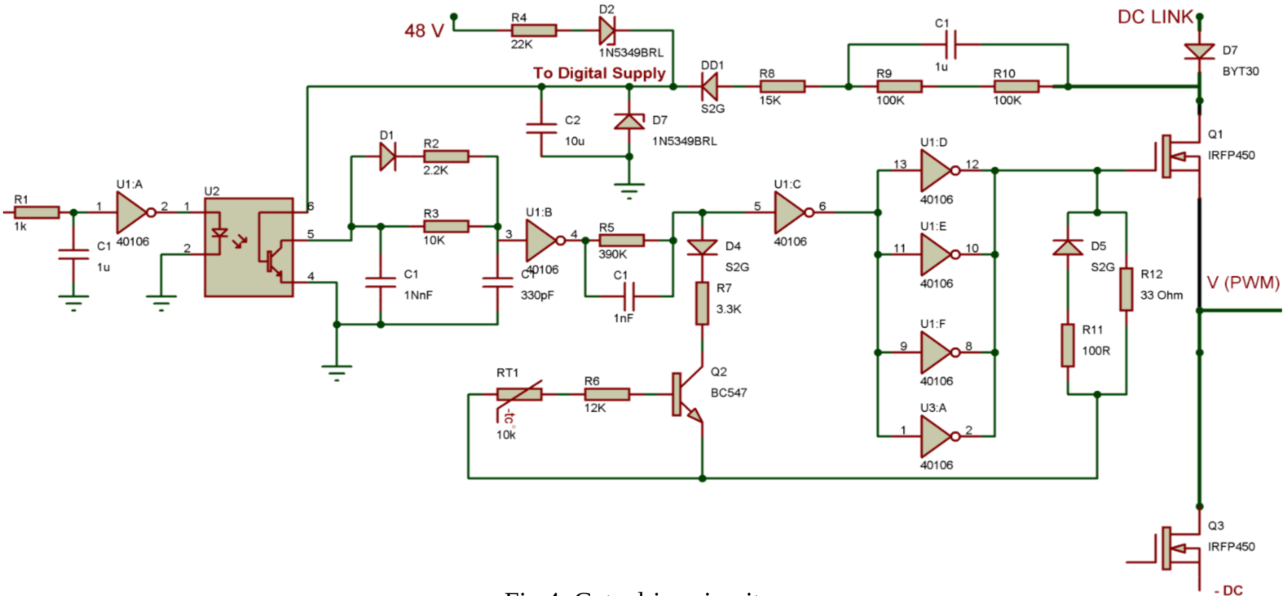

Fig.4: Gate drive circuits

the large size and the relatively high price of such transformers are reasons to consider an alternative. For a high

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switching speed, small size and I/O compatibility with the integrated circuits, a photon-coupled isolator 4N35 is chosen. For an efficient operation of the 4N35 opto-coupler, a buffer (40106-Schmitt Triggers) driven by a 1 kHz low pass filter is used at its input as shown in fig.4.

d. Gate firing circuits

The current and voltage levels of the output signals of the opto-couplers are not sufficient to drive the high power switches. Gate drive (aid) circuits are therefore required. For the CSI, six gate drive circuits (one per switch) have been designed as shown in fig.4:

e. DC link current continuity circuits

Generating the PWM signals using the available digital system such as microcontrollers are not always introduce the proper values of the overlap times in which any two consecutive switches are simultaneously ON. A simple and low cost concept for providing this overlap times is implemented by using a low pass filter with a fast ON slow OFF response as shown in Fig. 5, and a gate current controlled circuits with a slow ON fast OFF response of Fig. 6.

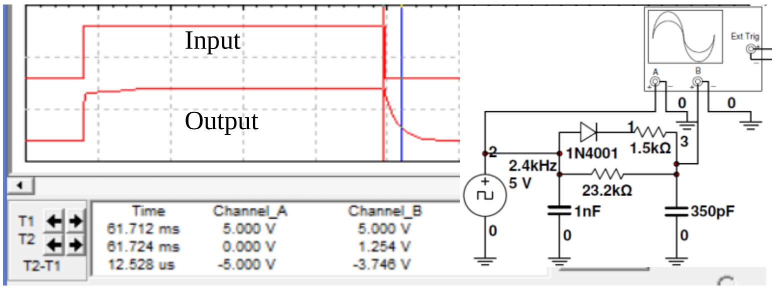

Fig.5: Fast ON Slow OFF circuit

According to the switching frequency of the PWM the resistors and the capacitors values are determined for providing the appropriate overlap times.

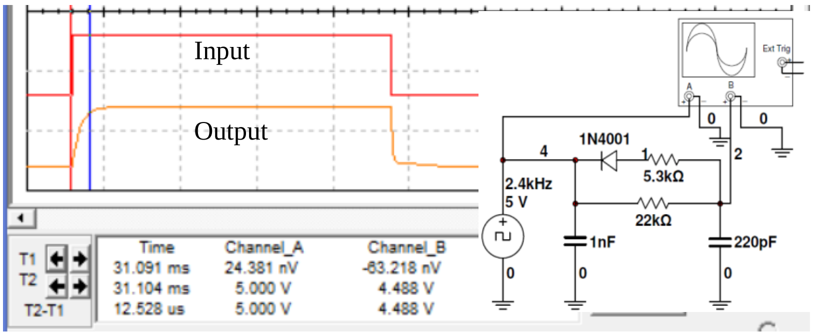

Fig.6: Slow ON Fast OFF circuit

f. Efficient operation

For a high drive capability and thus an efficient operation of the inverter power switch (MOSFET), four schmitt triggers in parallel are used in each of the gate’s drive circuits as shown in Fig.4.

g. Temperature compensation of the inverter switches

The semiconductors, temperature compensation is essential for efficient and safe inverter operation. The MOSFET temperature compensator consists of a capacitor and a Negative Temperature Coefficient (NTC) resistor in a base-emitter circuit of a common emitter transistor of Fig.4. A rise of the ambient or/and the MOSFET temperature results in a reduction of the ON times of the PWM. This is to limit the power transfer during the undesired high temperature of the inverter switches.

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h. Inverter switches

Different types of high power semiconductor switches are available nowadays. The selection of the inverter switches in general is based on the power ratings (voltage and current), the witching speed, base/gate drive requirements, and the price. For instance, for a 2kW power rating (small power range) current link PWM, the power MOSFET looks the most adequate choice. In this work, six N-channel 500V, 14A power MOSFETs (IRFP450) are used for the inverter circuit. The ON resistance R_{DS} of this MOSFET is about 0.4 Ω. In the current source inverter a high power diode in series with the MOSFET is used for blocking the reverse current and also to avoid a mains short circuit. Six BYT30 -30A/1000V power diodes are used in series with the inverter switches (diode per switch).

III. GLUE CIRCUITS

In the proposed system a glue circuits is a part of the digital system of Fig.1, consists of three stages, first is to feedback the rescaled mains voltages to the digital system. Second, is interfacing the voltage of the DC link to the digital system and the third stage is to read the current of the DC link to the digital system.

a. Interface circuits for the mains line voltages

In this work a digital synchronization of the line currents of the inverter with the line voltages of the mains is implemented. A simple attenuator with offset level control are designed and implemented as in Fig.7, to interface the mains line voltages and the A/D converter.

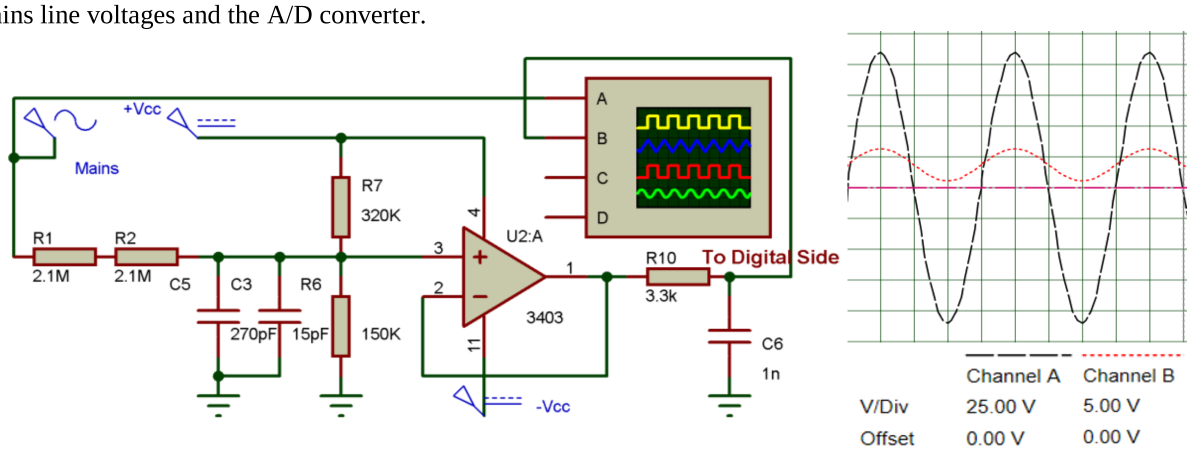

Fig.7: AC attenuator

b. Interface circuits for the voltage of the DC link

The desirable value of the modulation index is determined based on the available power in the DC link. For interfacing the voltage of the DC link and the A/D converter, a simple voltage attenuator is used. The implemented circuit diagram

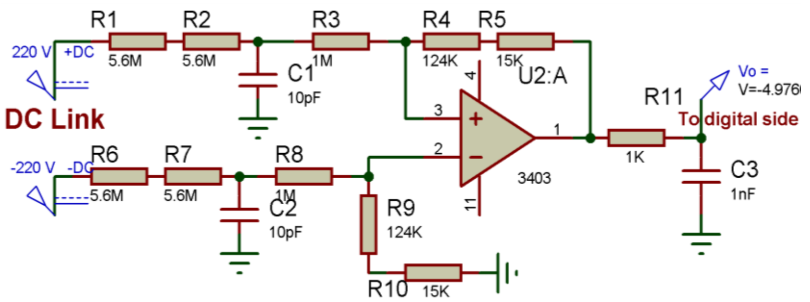

Fig.8: The DC link voltage attenuator

for the attenuator is shown in Fig.8. The system uses the attenuator output voltage in addition to the output of the next current sensor to digitally set the proper modulation index of the PWM pattern through the A/D converter. This output voltage is also used to protect the DC link against the over range of operation of the inverter.

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c. Interface circuits for the current of the DC link

The LA 55-P current transducer is used for converting the currents of the DC link to the equivalent DC voltages. These voltages are added to the output voltages of the DC attenuator of the DC link to decide the injected power to the grid..

d. System Protection

A system protection against the temperature rise is provided in the gate drive circuits as well as the protection against the temperature rise a protection against the over-voltage on the DC link is provided. In this work a hardware-protection based system is preferred instead of the software-based system. An unexpected hanging of the microprocessor can therefore be avoided. For this purpose a dissipater to absorb the over-voltage higher than 311V for short times (0.5seconds) is designed and implemented.

e. AC filter (capacitor filter)

For absorbing the rapid changes in the output current of the inverter an AC capacitor filter is used. For an allowable voltage ripple $V_{r,pp}$ the required capacitor value is given by:

$$C_Y = \frac{1}{2} T_{Cell} \frac{I_{av}}{V_{r,pp}} \tag{6}$$

where the highest voltage ripple appears when the firing signal of the inverter is almost square wave. With T_{cell} =222μs, $I_{av}=I_{dc}/2$ = 5A and $V_{r,pp}$=40V, the required C_{Δ}= 4.6μF. Here the AC filter is built using three 4.7μF delta connected capacitors .

IV. EXPERIMENTAL RESULTS

The whole system has been design and laboratory examined for the different proposed stages. The SAB80C517A microcontroller has been used for the digital realization of the symmetrical cell time PWM_CSI technique. The desired switching pattern has been obtained via a single Programmable Array Logic PAL chip. An HP E1429A/B-200MSa/s 2-channels digitizer system has been used for measuring and depicting the obtained results. The output line voltage for Y-

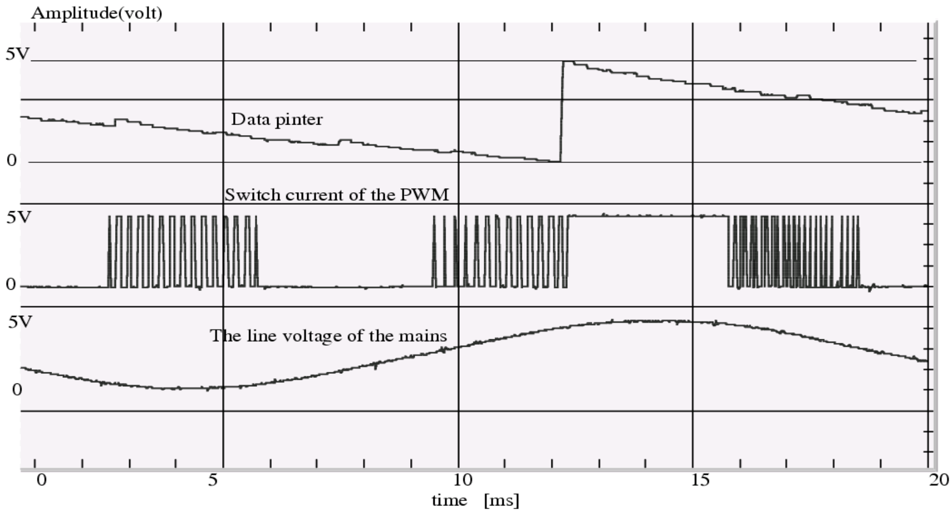

Fig.10: Data pointer (frequency controller), switch current and the line voltage of the glow circuits

connected load resistance at a modulation index of 0.5, the influence of the output capacitor filter is clearly displayed in the waveform especially at middle of the modulation index. Some of the output waveforms of the drive circuits are depicted in fig.10, 11 and 12. Phase counter (data pointer) output of Fig.10 is digitally obtained using the microprocessor counter, displayed via the implemented Digital to analog converter.

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The line voltage of the 5V-pp is obtained by using the attenuator circuits. The switch space vector PWM is directly

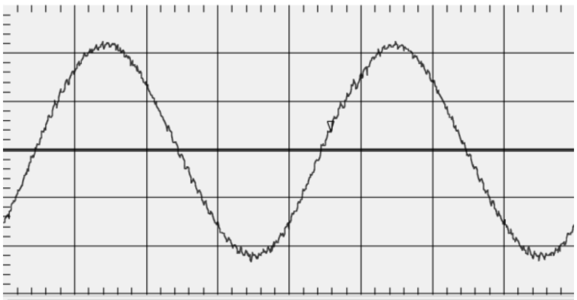

Fig.11: Output line voltage with capacitor filter

measured at the gate of the power MOSFET. The output line voltage of the Y-connected load resistance is shown in Fig.11. Synchronization of the extracted line current with line voltage of the grid is displayed in Fig.12.

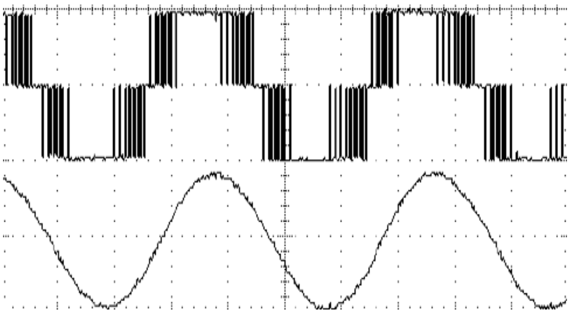

Fig.12: The synchronized inverter line current and the grid line voltage

V. CONCLUSIONS

A complete design for the renewable current link PWM connected to the grid is presented. A full wave rectifier is used for the AC/DC conversion. An appropriate value of the DC link inductor has been calculated and implemented. Power MOSFET CSI (drive and circuits) is designed and implemented. The digital and the power sides of the inverter are isolated using the opto-coupler. The CSI constraint (current continuity) is hardware fulfilled using the inverter drive circuits. Temperature compensator has been designed for reducing the ON times of the PWM when the MOSFET temperature rises. Interface circuits for adapting the mains line voltages, current and voltage of the DC link to the logic level have been designed. The different stages of the inverter are designed for an efficient operation. The inverter circuits are protected against over-voltage of the DC link using a dissipator. Some of the experimental results of the designed circuits are presented and fully satisfying the desired operation requirements.

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BIOGRAPHY

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